3.3V CMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74LVCH646A

FEATURES:
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP, 0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of − 40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH646A:
- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:
- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVCH646A device consists of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data is stored in one register and B data can be stored in the other register. When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.
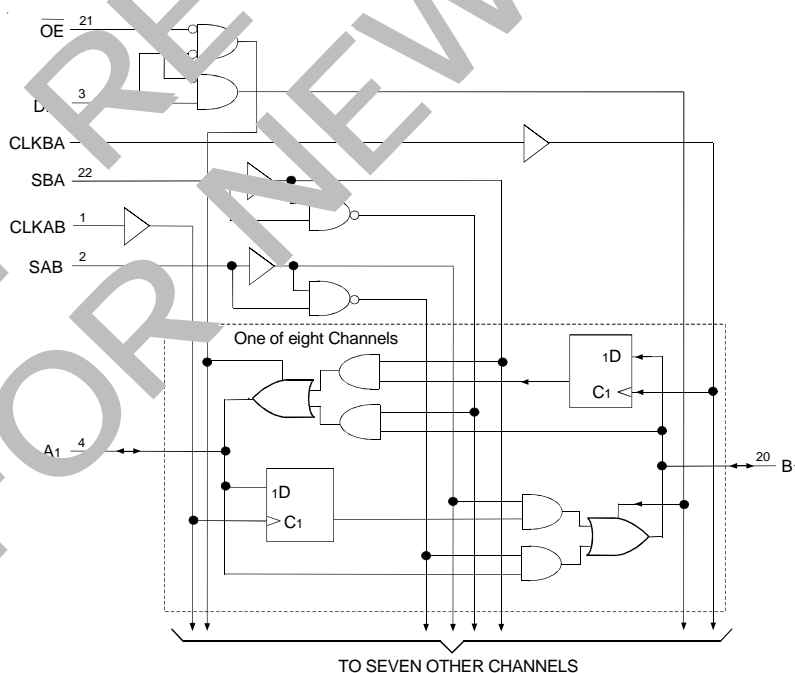
The LVCH646A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
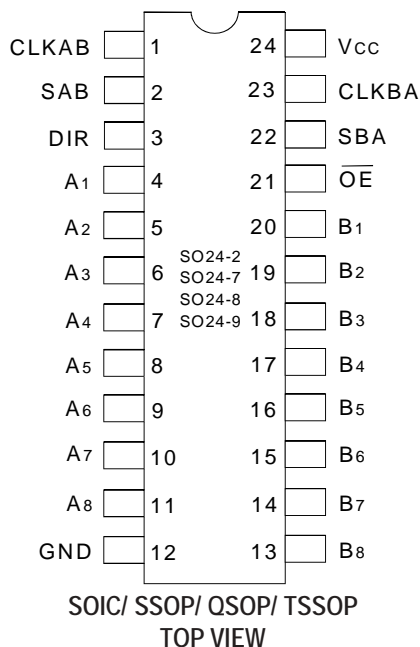
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVCH646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

TO SEVEN OTHER CHANNELS

EXTENDED COMMERCIAL TEMPERATURE RANGE

OCTOBER 1999

DSC-4499/-

PIN CONFIGURATION

CLKAB	1	24	V$_{CC}$
SAB	2	23	CLKBA
DIR	3	22	SBA
A$_1$	4	21	$\overline{OE}$
A$_2$	5	20	B$_1$
A$_3$	6	19	B$_2$
A$_4$	7	18	B$_3$
A$_5$	8	17	B$_4$
A$_6$	9	16	B$_5$
A$_7$	10	15	B$_6$
A$_8$	11	14	B$_7$
GND	12	13	B$_8$

SO24-2
SO24-7
SO24-8
SO24-9

SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
Ax	Data Register A Inputs [1] Data Register B Outputs
Bx	Data Register B Inputs [1] Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
$\overline{OE}$	Output-enable Input
DIR	Direction-control Input

NOTE:
1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Description	Max.	Unit
V$_{TERM}$	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T$_{STG}$	Storage Temperature	– 65 to +150	°C
I$_{OUT}$	DC Output Current	– 50 to +50	mA
I$_{IK}$ I$_{OK}$	Continuous Clamp Current, V$_I$ < 0 or V$_O$ < 0	– 50	mA
I$_{CC}$ I$_{SS}$	Continuous Current through each V$_{CC}$ or GND	±100	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
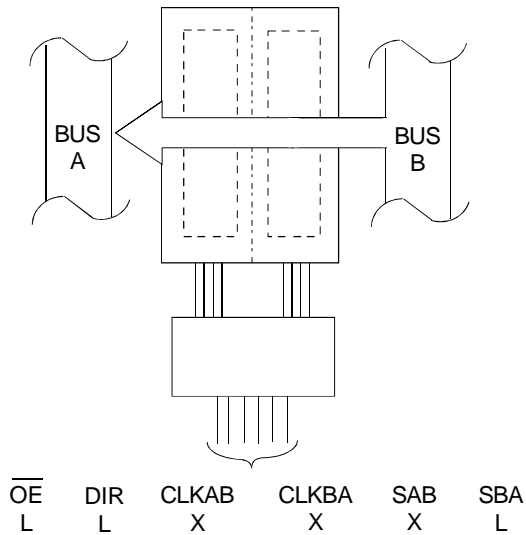
CAPACITANCE (T$_A$ = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 0V	4.5	6	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 0V	5.5	8	pF
C$_{I/O}$	I/O Port Capacitance	V$_{IN}$ = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

FUNCTION TABLE [1]

Inputs						Data I/O		
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	Operation or Function
X	X	↑	X	X	X	Input	Unspecified[2]	Store A, B unspecified[2]
X	X	X	↑	X	X	Unspecified[2]	Input	Store B, A unspecified[2]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real Time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled; i.e., data at the bus pins willl be stored on every LOW-to-HIGH transition on the clock inputs.

$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A

$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X
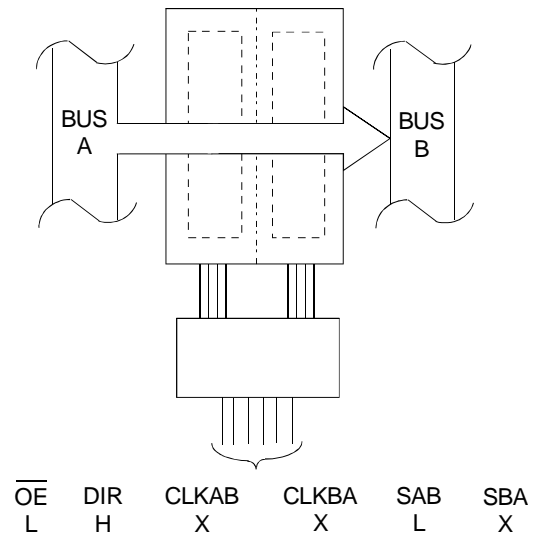
REAL-TIME TRANSFER
BUS A TO BUS B

$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X
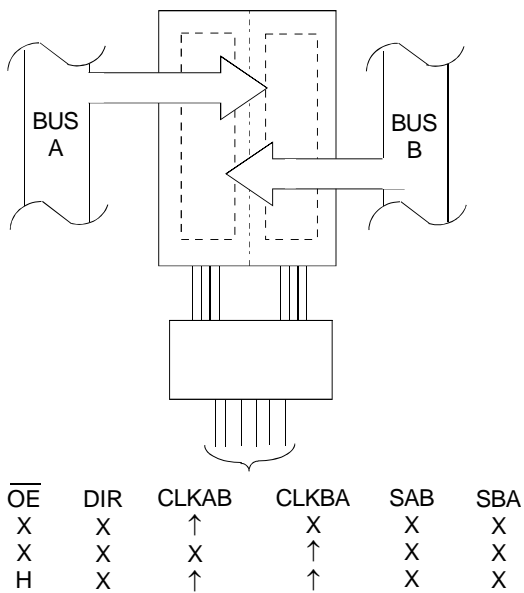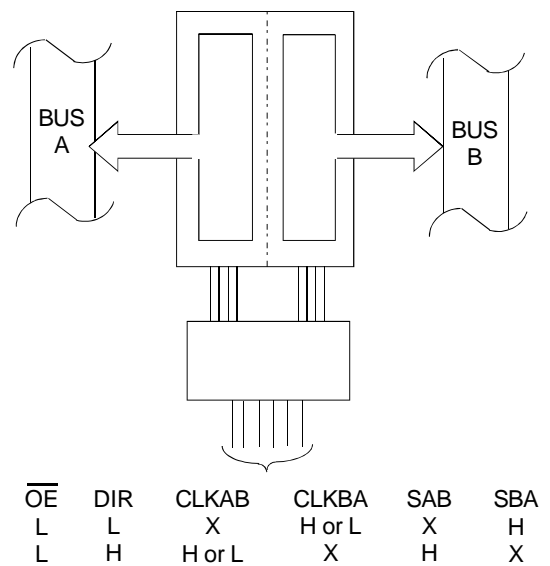
TRANSFER STORED DATA
TO A AND/OR B[1]

NOTE:
1. LVCH646A cannot transfer data to A bus and B bus simultaneously.

3

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = – 40°C To +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
I_{CCZ}			3.6 ≤ V_{IN} ≤ 5.5V[2]	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

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NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = − 0.1mA	V_{CC} − 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = − 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = − 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = − 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = − 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power dissipation capacitance per transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	75	pF
C_{PD}	Power dissipation capacitance per transceiver Outputs disabled		9	pF

SWITCHING CHARACTERISTICS [1]

Symbol	Parameter	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		—	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax or Bx to Bx or Ax	—	—	—	7.9	1.4	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to Ax or Bx	—	—	—	8.8	1.3	8.4	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Ax or Bx	—	—	—	9.9	1.4	8.6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Ax	—	—	—	10.2	1	8.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Ax	—	—	—	8.9	1	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to Bx	—	—	—	10.4	1.2	8.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to Bx	—	—	—	8.7	1.1	7.9	ns
t_W	Pulse Duration	—	—	3.3	—	3.3	—	ns
t_{SU}	Setup Time, data before CLK↑	—	—	1.6	—	1.5	—	ns
t_H	Hold Time, data after CLK↑	—	—	1.7	—	1.7	—	ns
$t_{SK(o)}$	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = − 40°C to + 85°C.
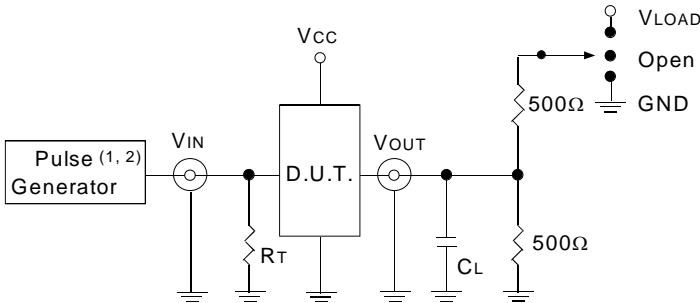2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$ = 3.3V ±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$ = 2.5V ±0.2V	Unit
V_{LOAD}	6	6	2 x V_{CC}	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	V_{CC} / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS

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DEFINITIONS:
C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - tsk (x)
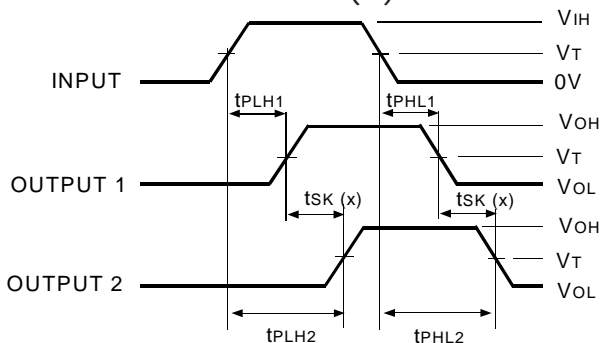
$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
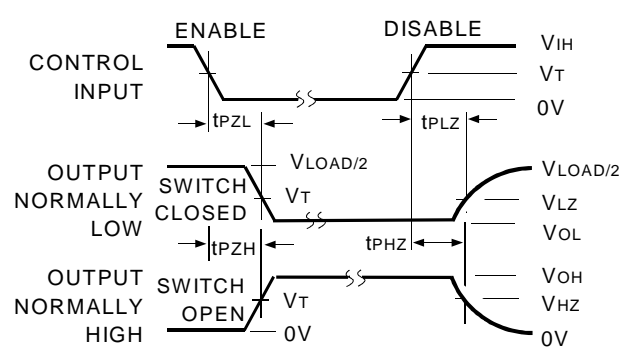
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NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY
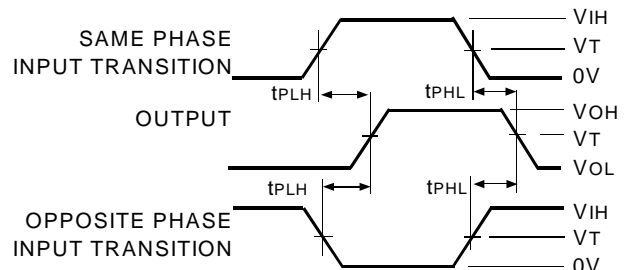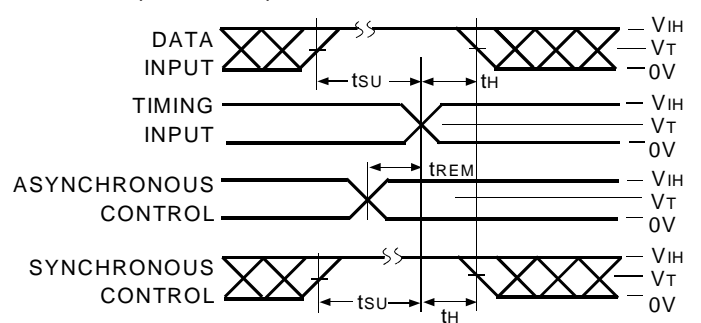

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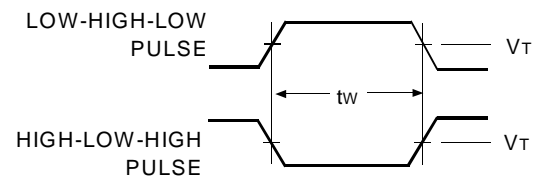## ENABLE AND DISABLE TIMES

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NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES

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PULSE WIDTH

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ORDERING INFORMATION

IDT _____XX_____ LVC ___X___ ___XXXX___ ___XX___
   Temp. Range   Bus-Hold Device Type Package

SO	Small Outline IC (gull wing) (SO24-2)
PY	Shrink Small Outline Package (SO24-7)
Q	Quarter Size Small Outline Package (SO24-8)
PG	Thin Shrink Small Outline Package (SO24-9)
646A	Octal Bus Transceiver and Register with 3-State Outputs, ±24mA
H	Bus-hold
74	−40°C to +85°C