256/512/1K/2K/4K x 9-bit First-In/First-Out (FIFO)

L8C200/201 L8C202/203/204

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- High Speed — to15 ns Access Time
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Empty and Full Warning Flags
- Auto Retransmit Capability
- Plug Compatible with IDT720x, Cypress CY7C4x, and Samsung KM75C0x
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin CerDIP
  - 32-pin Plastic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The L8C200, L8C201, L8C202, L8C203, and L8C204 are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C200 – 256 x 9-bit
L8C201 – 512 x 9-bit
L8C202 – 1024 x 9-bit
L8C203 – 2048 x 9-bit
L8C204 – 4096 x 9-bit

Each memory utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty flags are provided to prevent data overflow and underflow. Three additional pins are also provided to allow for unlimited expansion in both word size and depth. Depth Expansion does not result in a flow-through penalty. The parts are hooked up with the data and control signals in parallel. The active device is determined by the Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals which are daisy chained from device to device.

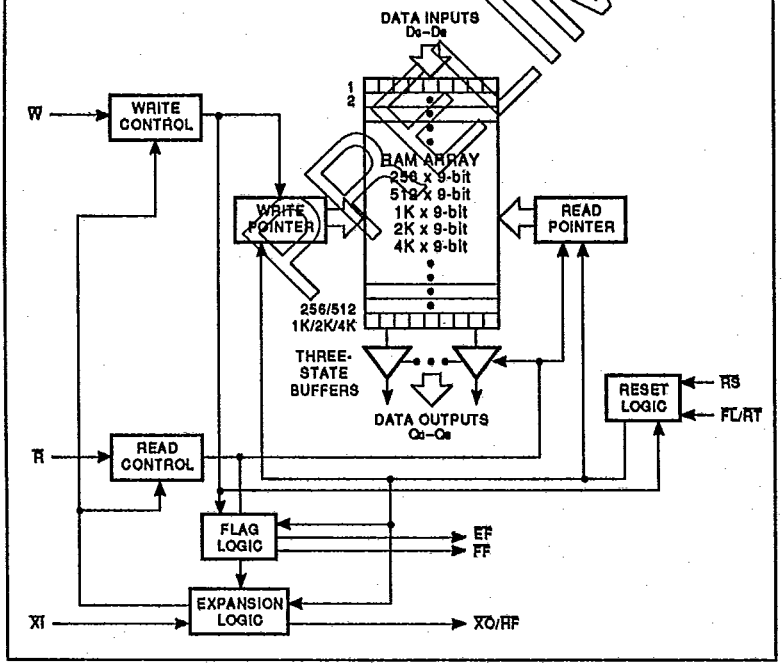
The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The nine data outputs go to the high impedance state when $\overline{R}$ is HIGH. A Retransmit ($\overline{RT}$) capability allows for reset of the read pointer when $\overline{RT}$ is pulsed LOW, allowing for retransmission of data from the beginning. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data. A Half Full ($\overline{HF}$) output flag is available in the single device and width expansion modes. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

The FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

The FIFOs are designed for those applications requiring asychronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Latchup and static discharge protection is provided on-chip. The FIFOs can withstand an injection current of up to 200 mA on any pin without damage.

L8C200/201/202/203/204 Block Diagram



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T-46-35

Maximum Ratings *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	–0.5 V to +7.0 V
DC input voltage	–3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (Vcc)
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	–55°C to +125°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = –2.0 mA, Vcc = Min.	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA, Vcc = Min.			0.4	V
VIH	Input High Voltage		2.2		Vcc + 0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Leakage Current	GND ≤ VIN ≤ Vcc	–10		+10	µA
IOZ	Output Leakage Current	$\overline{R}$ ≥ VIH, GND ≤ VOUT ≤ Vcc	–10		+10	µA
IOS	Output Short Current	VOUT = GND, Vcc = Max (Note 4)			–150	mA
ICC2	Vcc Current, Standby	All Inputs = VIH MIN (Note 7)			35	mA
ICC3	Vcc Current, Powerdown	All Inputs = Vcc (Note 13)			20	mA
CIN	Input Capacitance	Ambient Temp = 25°C, Vcc = 4.5 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 8)			7	pF

			L8C200/201/202/203/204-					
Symbol	Parameter	Test Condition (MHz)→	15	20	25	35	50	Unit
ICC1	Vcc Current, Active	Vcc = Max., IOUT = 0 mA (Notes 5, 6)	100	100	90	90	80	mA
Fs	Shift Frequency		40	33	25	20	15	MHz

PRELIMINARY

SIGNAL DESCRIPTIONS

INPUTS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown (i.e., t_{WHSH} before the rising edge of $\overline{RS}$) and should not change until t_{SHWL} after the rising edge of $\overline{RS}$. Hall-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold time must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RHFH}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operating has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WHEH} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The FIFOs can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than the full memory has been written between resets. Retransmit will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

DATA INPUTS (D_0–D_8)

Data input signals for 9-bit wide data. Data has setup and hold time requirements with respect to the rising edge of $\overline{W}$.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 256 writes for the L8C200, 512 writes for the LCF201, 1024 wites for the L8C202, 2048 wites for the L8C203, and 4096 writes for the L8C204.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device Mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then deasserted by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0–Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read enable ($\overline{R}$) is in a high state or the device is empty.

PRELIMINARY

3

OPERATING MODES

SINGLE DEVICE MODE

A single FIFO may be used when the application requirements are for the number of words in a single device. The FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is the active function of the combination pin $\overline{XO}/\overline{HF}$.

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be detected from any one device. Any word width can be attained by adding additional FIFOs. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. **Do not connect any output signals together.**

DEPTH EXPANSION (DAISY CHAIN) MODE

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. Any depth can be attained by adding additional FIFOs. The FIFOs operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device with the last device connecting back to the first.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing FIFOs. Care must be taken to assure that the appropriate flag is monitored by each system, i.e., $\overline{FF}$ is monitored on the device when $\overline{W}$ is used; $\overline{EF}$ is monitored on the device when $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode, the FIFO permits the reading of a single word after writing one word data into an empty FIFO. The data is enabled on the bus in ($t_{WHEH} + t_{RLQV}$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{AHQZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag). However, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode, the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer. The user must be aware that there is no minimum value for t_{RLEL} and t_{WLFL}. These pulses may be slight during some operating conditions and lot variations.

PRELIMINARY

T-46-35

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLRL	Read Cycle Time	65		45		35		30		25	
tRLQV	Read Low to Output Valid (Access Time)		50		35		25		20		15
tRHRL	Read High to Read Low (Notes 9, 10)	15		10		10		10		8	
tRLRH	Read Low to End of Read Cycle (Notes 9, 10)	50		35		25		20		15	
tRLQZ	Read Low to Output Low Z (Note 2)	10		5		5		5		3	
tRHQV	Read High to Output Valid	5		5		5		5		5	
tRHQZ	Read High to Output High Z (Note 15)		30		20		10		10		10
tWLWL	Write Cycle Time (Note 10)	65		45		35		30		25	
tWLWH	Write Low to Write High (Notes 9, 10)	50		35		25		20		15	
tWHWL	Write High to End of Write Cycle (Notes 9, 10)	15		10		10		10		8	
tDVWH	Data Valid to Write High (Notes 9, 10)	30		18		15		15		10	
tWHDX	Write High to Data Change (Notes 9, 10)	5		0		0		0		0	
tSLSH	Reset Cycle Time (Notes 10, 11)	50		35		25		20		15	
tSLWL	Reset Low to Write Low (Notes 10, 11)	65		45		35		30		25	
tWHSH	Write High to Reset High (Notes 10, 11)	50		35		25		20		15	
tRHSH	Read High to Reset High (Notes 10, 11)	50		35		25		20		15	
tSHWL	Reset High to Write Low (Notes 10, 11)	15		10		10		10		8	
tSLEL	Reset Low to Empty Flag Low		65		45		35		30		25
tSLHH	Reset Low to Half-Full Flag High		65		45		35		30		25
tSLFH	Reset Low to Full Flag High		65		45		35		30		25

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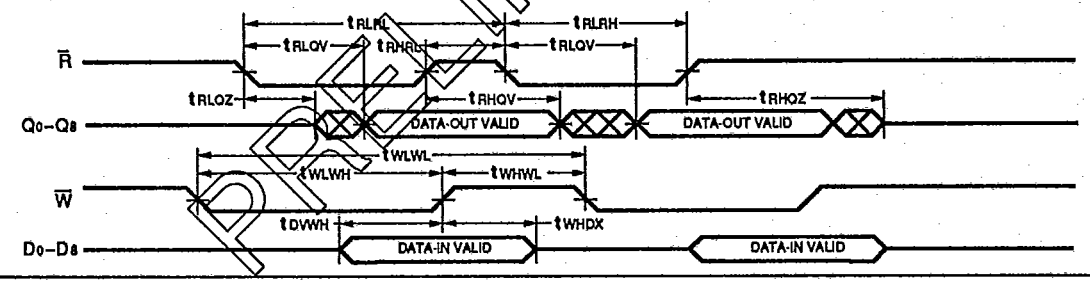
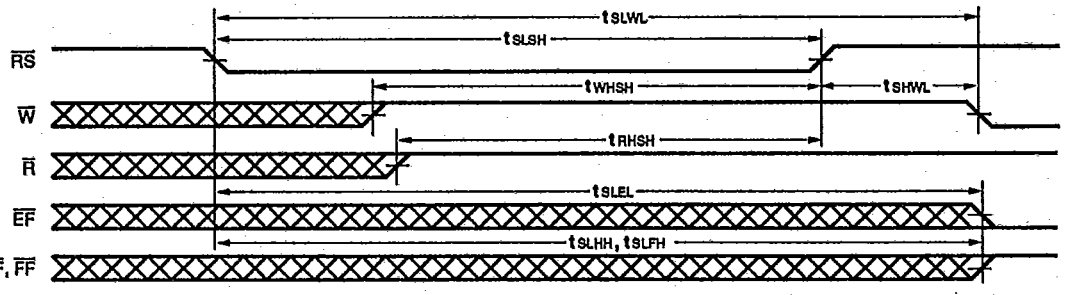
ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING



PRELIMINARY

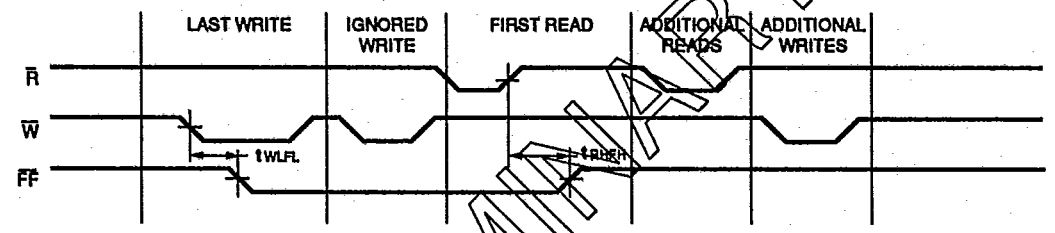
T-46-35

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

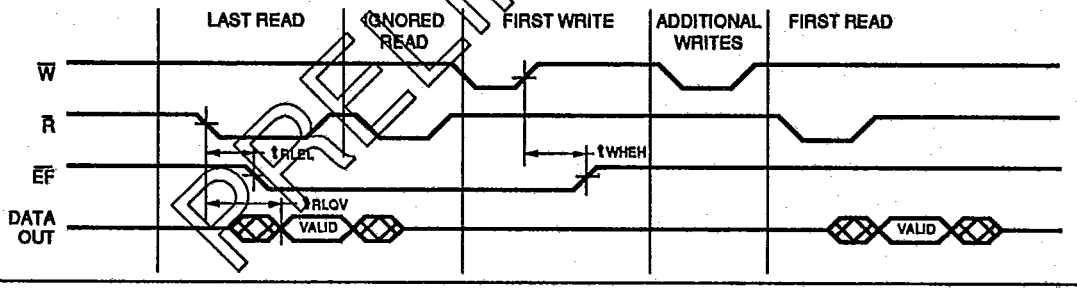
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLQV	Read Low to Output Valid		50		35		25		20		15
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tTLAL	Retransmit Cycle Time	65		45		35		30		25	
tTLTH	Retransmit Low to End of Retransmit Cycle (Notes 9, 10, 11)	50		35		25		20		15	
tAHTH	Read/Write High to Retransmit High (Notes 9, 10, 11)	50		35		25		20		15	
tTHAL	Retransmit High to Read/Write Low (Note 10)	15		10		10		10		8	

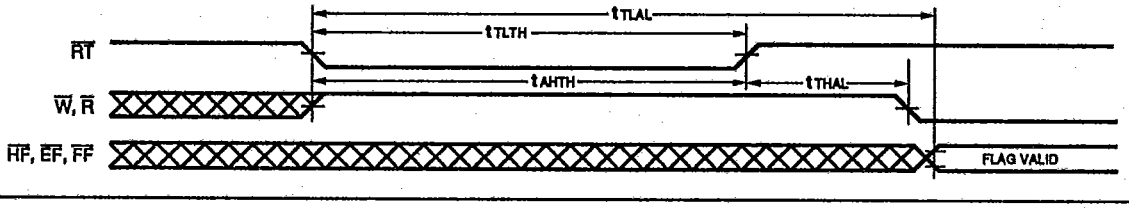
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT



PRELIMINARY

T-46-35

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRHFH	Read High to Full Flag High		45		30		25		25		25
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tRHHH	Read High to Half-Full Flag High		65		45		35		30		25
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLHL	Write Low to Half-Full Flag Low		65		45		35		30		25
tFHWH	Write Pulse Width After Full Flag High (Note 10)	50		35		25		20		15	

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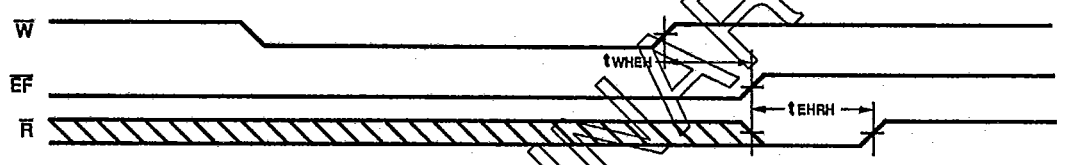
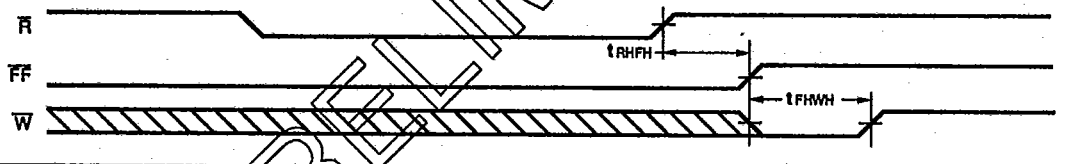
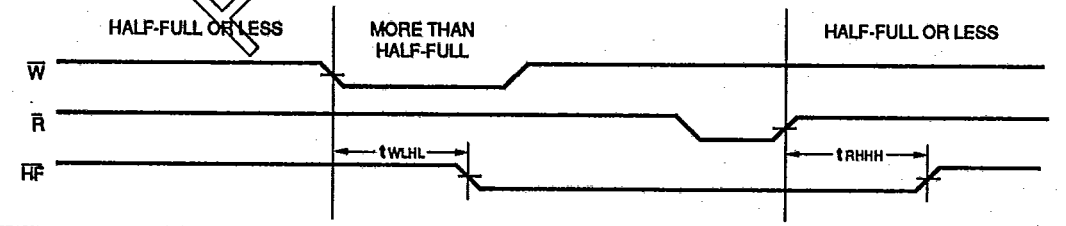
EMPTY FLAG TIMING



FULL FLAG TIMING



HALF-FULL FLAG TIMING



PRELIMINARY

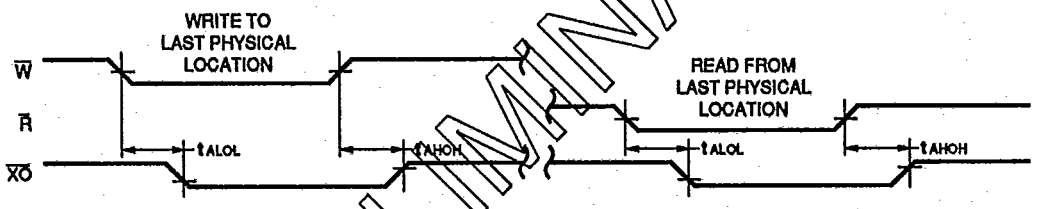
T-46-35

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

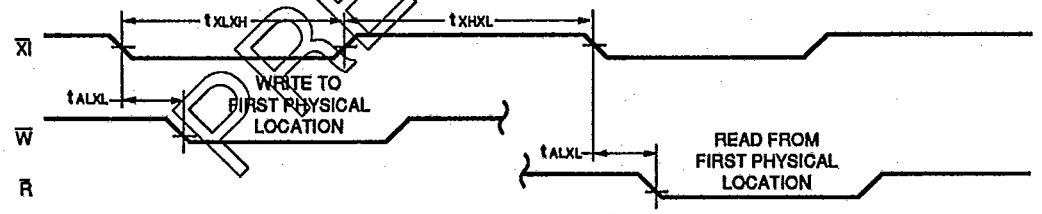
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tALOL	Read/Write to Expansion Out Low (Note 12)		50		35		25		20		15
tAHOH	Read/Write to Expansion Out High (Note 12)		50		35		25		20		15
tXLXH	Expansion In Pulse Width (Notes 10, 12)	50		35		25		20		15	
tXHXL	Expansion In High to Expansion In Low (Notes 10, 12)		10		10		10		10		10
tALXL	Read/Write Low to Expansion In Low (Notes 10, 12)	15		10		10		10		10	

EXPANSION OUT



EXPANSION IN



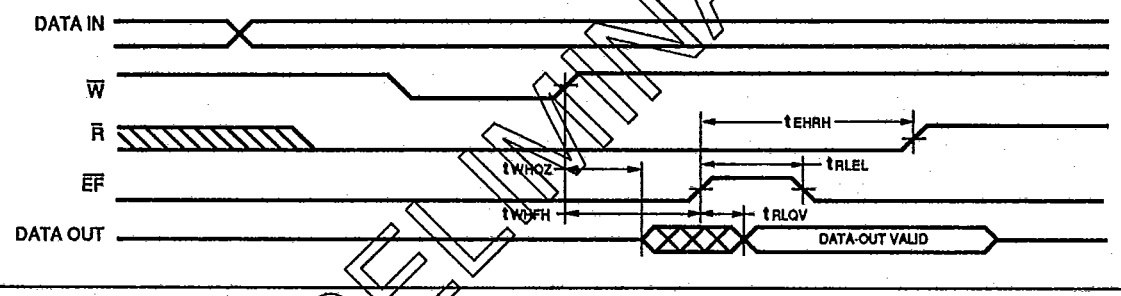
PRELIMINARY

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

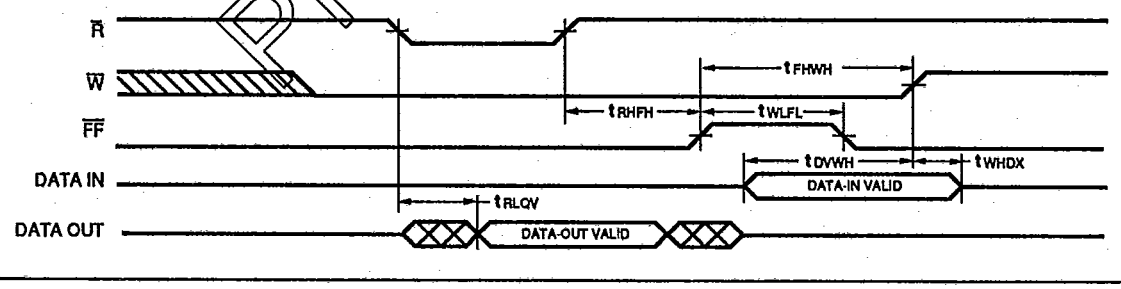
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tWHEH	Write High to Empty Flag High	45		30		25		25		25	
tRLQV	Read Low to Output Valid		50		35		25		20		15
tWHQZ	Write High to Output Low Z (Notes 14, 15)	15		10		5		5		3	
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tFHWH	Write Pulse Width After Full Flag High	50		35		25		20		15	
tDVWH	Data Valid to Write High	30		18		15		15		10	
tWHDX	Write High to Data Change	5		0		0		0		0	

READ DATA FLOW-THROUGH MODE



WRITE DATA FLOW-THROUGH MODE



PRELIMINARY

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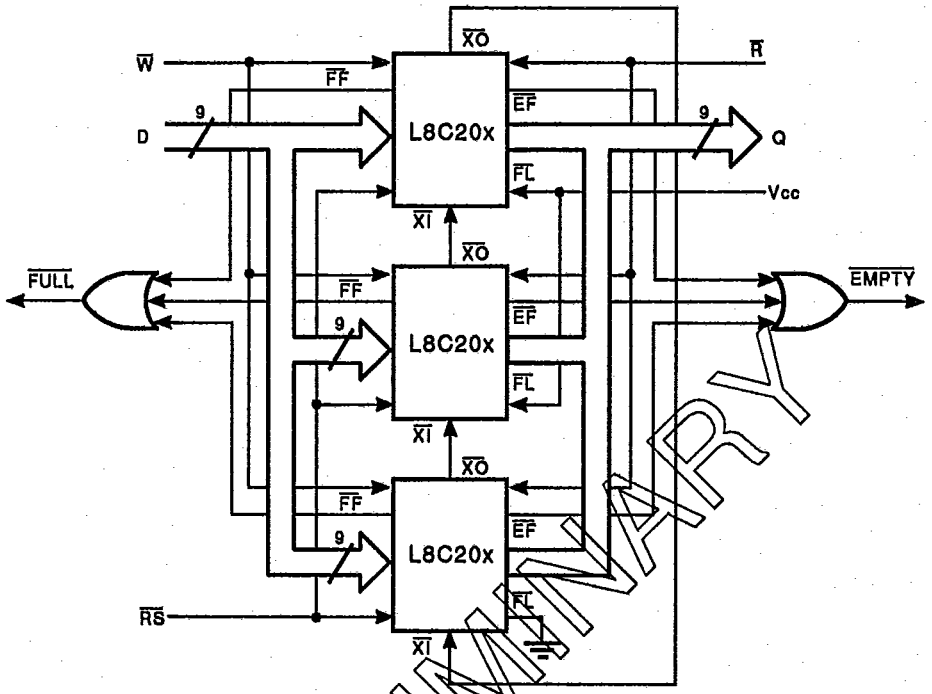
T-46-35

FIFO Memory (Depth Expansion) Block Diagram



PRELIMINARY

Table 1. Reset and Retransmit (Single Device Configuration/Width Expansion Mode)

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS		
	$\overline{RS}$	$\overline{RT}$	XI	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X

Table 2. Reset and First Load Truth Table (Depth Expansion/Compound Expansion Mode)

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS	
	$\overline{RS}$	$\overline{RT}$	XI	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Others	0	1	(1)	Location Zero Disabled	Location Zero Disabled	0	1
Read/Write	1	(2)	(1)	X	X	X	X

(1) See Depth Expansion Block Diagram above.
(2) Unchanged.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. Tested with outputs open in the worst static input control signal combination (i.e., $\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{FL}$, and $\overline{RS}$).

8. These parameters are guaranteed but not 100% tested.

9. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RLRH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. When cascading devices, the reset pulse width must be increased to equal $t_{SLSH} + t_{SLHH}$.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. Tested with output open and $\overline{RS} = \overline{FL} = \overline{XI} = \overline{R} = \overline{W} = VCC$.

14. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

15. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

16. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

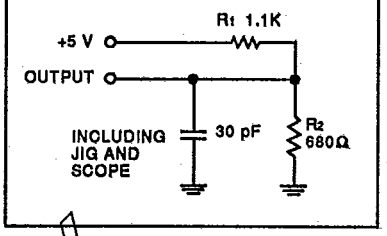


FIGURE 1b.

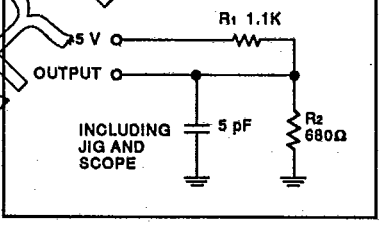
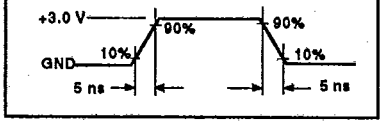


FIGURE 2.

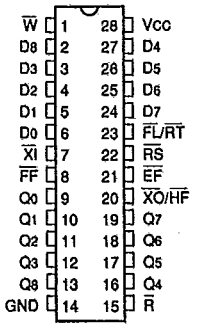


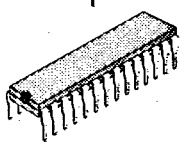
PRELIMINARY

3

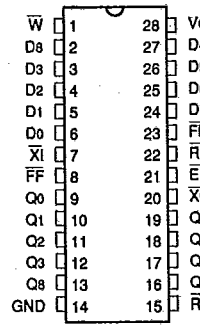
ORDERING INFORMATION

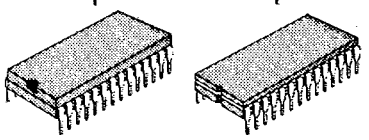
28-pin (0.3" wide)



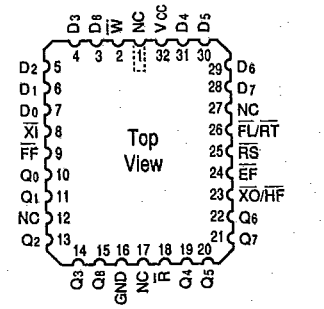


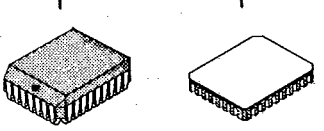
28-pin (0.6" wide)





32-pin





Speed	Plastic DIP (P10)		Plastic DIP (P9)	CerDIP (C6)	Plastic Leaded Chip Carrier (J6)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening					
50 ns 35 ns 25 ns 20 ns 15 ns	L8C200PC – 50 L8C201PC – 35 L8C202PC – 25 L8C203PC – 20 or L8C204PC – 15		L8C200NC – 50 L8C201NC – 35 L8C202NC – 25 L8C203NC – 20 or L8C204NC – 15	L8C200CC – 50 L8C201CC – 35 L8C202CC – 25 L8C203CC – 20 or L8C204CC – 15	L8C200JC – 50 L8C201JC – 35 L8C202JC – 25 L8C203JC – 20 or L8C204JC – 15	L8C200KC – 50 L8C201KC – 35 L8C202KC – 25 L8C203KC – 20 or L8C204KC – 15
	–55°C to +125°C — Commercial Screening					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CM – 50 L8C201CM – 35 L8C202CM – 25 L8C203CM – 20 or L8C204CM		L8C200KM – 50 L8C201KM – 35 L8C202KM – 25 L8C203KM – 20 or L8C204KM
	–55°C to +125°C — Extended Screening					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CME – 50 L8C201CME – 35 L8C202CME – 25 L8C203CME – 20 or L8C204CME		L8C200KME – 50 L8C201KME – 35 L8C202KME – 25 L8C203KME – 20 or L8C204KME
	–55°C to +125°C — MIL-STD-883 Compliant					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CMB – 50 L8C201CMB – 35 L8C202CMB – 25 L8C203CMB – 20 or L8C204CMB		L8C200KMB – 50 L8C201KMB – 35 L8C202KMB – 25 L8C203KMB – 20 or L8C204KMB

PRELIMINARY