Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

Separate Data Inputs and Outputs

IDT 71981S/L
IDT 71982S/L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT71981/2S
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
  - IDT71981/2L
    Active: 300mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, 28-pin SOIC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

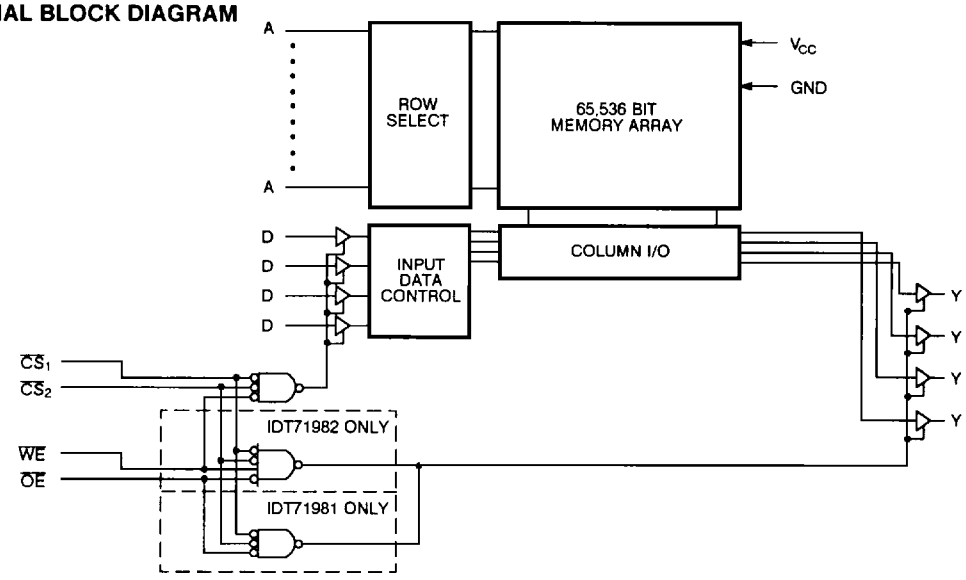
Access times as fast as 15ns are available with typical power consumption of only 300mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}_1$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30µW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71981/IDT71982 are packaged in either space-saving 28-pin, 400 mil hermetic DIPs, 28-pin 300 mil plastic DIP, 28-pin SOIC or 28-pin leadless chip carriers, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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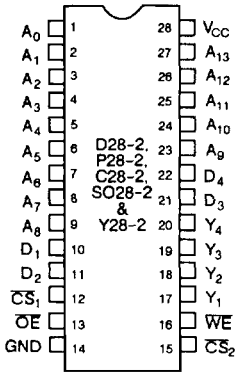
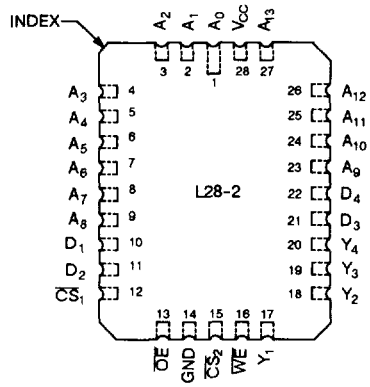
PIN CONFIGURATIONS

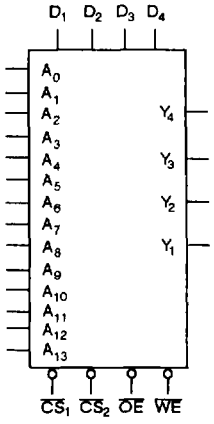


DIP/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{13}	Address Inputs	D_1-D_4	$DATA_{IN}$
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects	Y_1-Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71981/2S MIN.	IDT71981/2S TYP.(1)	IDT71981/2S MAX.	IDT71981/2L MIN.	IDT71981/2L TYP.(1)	IDT71981/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	71981/2S15 COM'L.	71981/2S15 MIL.	71981/2 S19/20 COM'L.	71981/2 S19/20 MIL.	71981/2S25 71981/2L25 COM'L.	71981/2S25 71981/2L25 MIL.	71981/2S30/35 71981/2L30/35 COM'L.	71981/2S30/35 71981/2L30/35 MIL.	71981/2S45/55(3) 71981/2L45/55(3) COM'L.	71981/2S45/55(3) 71981/2L45/55(3) MIL.	71981/2S70 71981/2L70 COM'L.	71981/2S70 71981/2L70 MIL.	71981/2S85 71981/2L85 COM'L.	71981/2S85 71981/2L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	135	155	125	140	125	140	–	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IL}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

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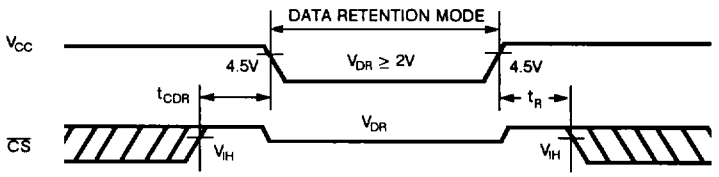
LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

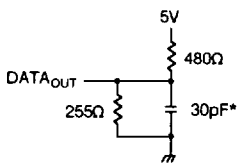


Figure 1. Output Load

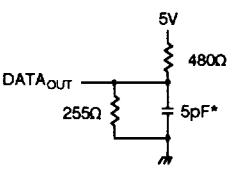


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

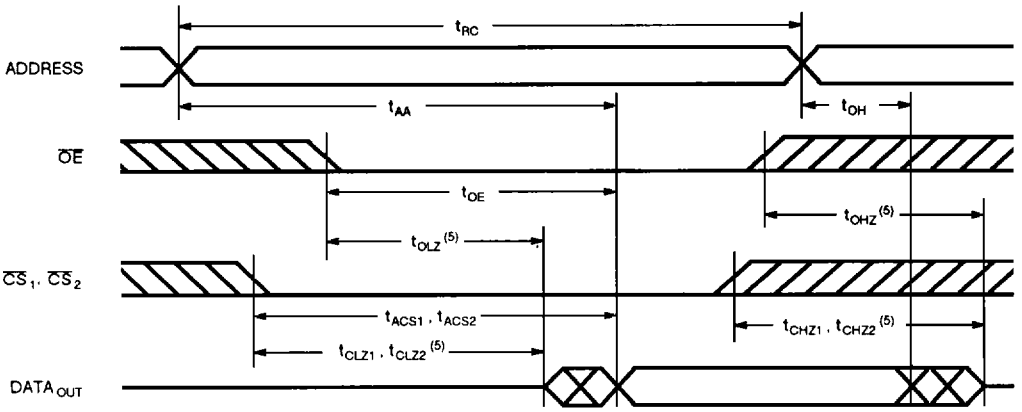
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71981/2S15[1] /19/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/19/20	–	25/29	–	35/45	–	55	–	70	–	85	ns
$t_{ACS1, 2}$	Chip Select-1, 2 Access Time[3]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{CLZ1, 2}$	Chip Select-1, 2 to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	8/9/9	–	11/18	–	20/25	–	35	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ1, 2}$	Chip Select-1, 2 to Output in High Z[4]	–	7/8/8	–	10/12	–	14	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output In High Z[4]	–	7/8/8	–	9/12	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[4]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns

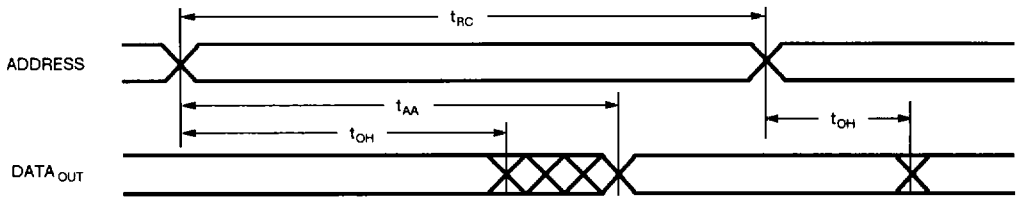
NOTES:

1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

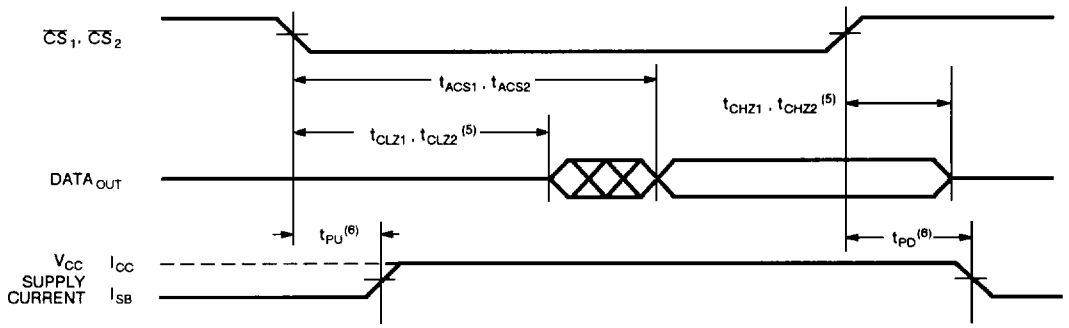
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$, and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.
6. This parameter is guaranteed but not tested.

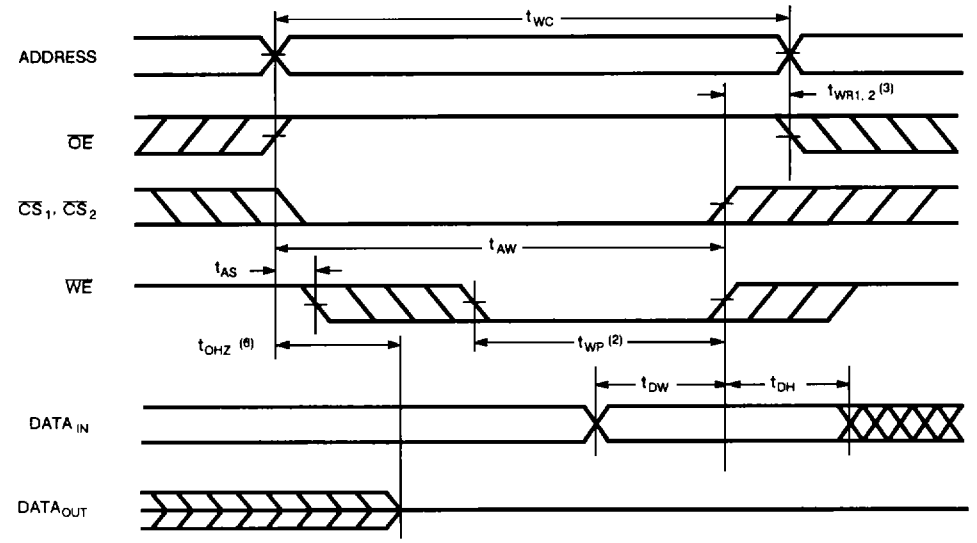
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71981/2S15[1] /19/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17/17	–	20/22	–	30/40	–	50	–	60	–	75	–	ns
$t_{CW1,2}$	Chip Select to End of Write	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
$t_{WR1,2}$	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z [3,5]	–	5/6/6	–	7/10	–	10/15	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	8/10/10	–	13	–	15/20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [3,5]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid [3,4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns
t_{WY}	Write Enable to Output Valid [3,4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns

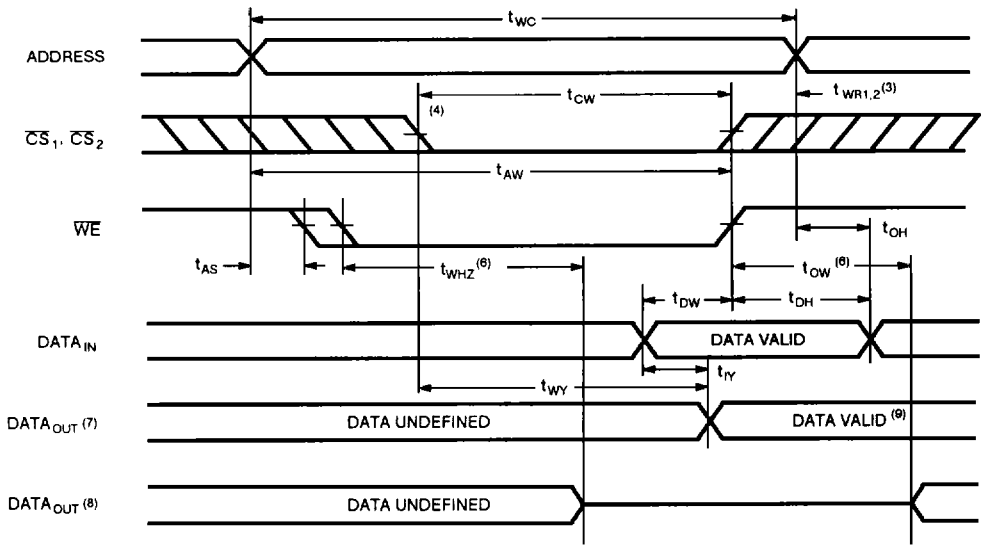
NOTES:

1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

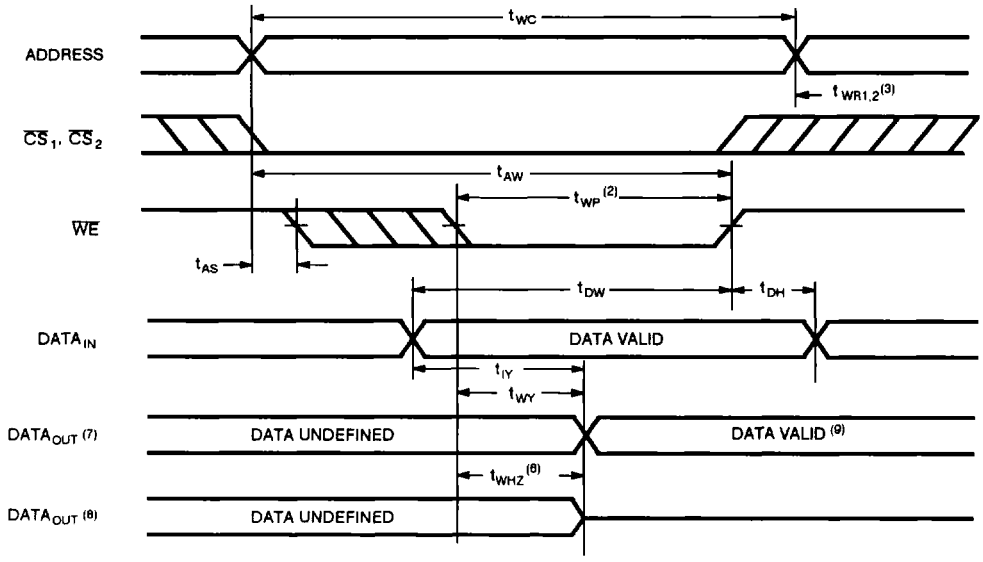
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) [1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) [1, 5]



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW) [1, 5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}_1$, or $\overline{CS}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a low $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}_1$ and or $\overline{CS}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT}$ = $DATA_{IN}$

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write (1)	L	L	L	L	D_{IN}	Active
Write (1)	L	L	L	H	High Z	Active
Write (2)	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

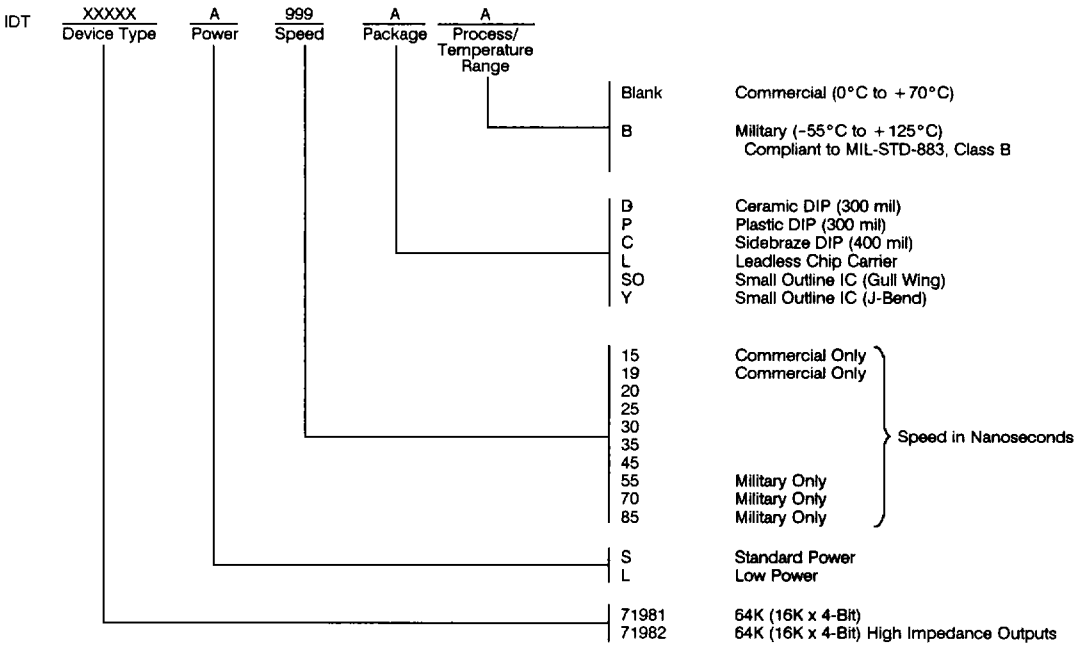
NOTES:
1. For IDT71981 only.
2. For IDT71982 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION



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