



HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT74FCT823AT/BT/CT/DT

FEATURES:

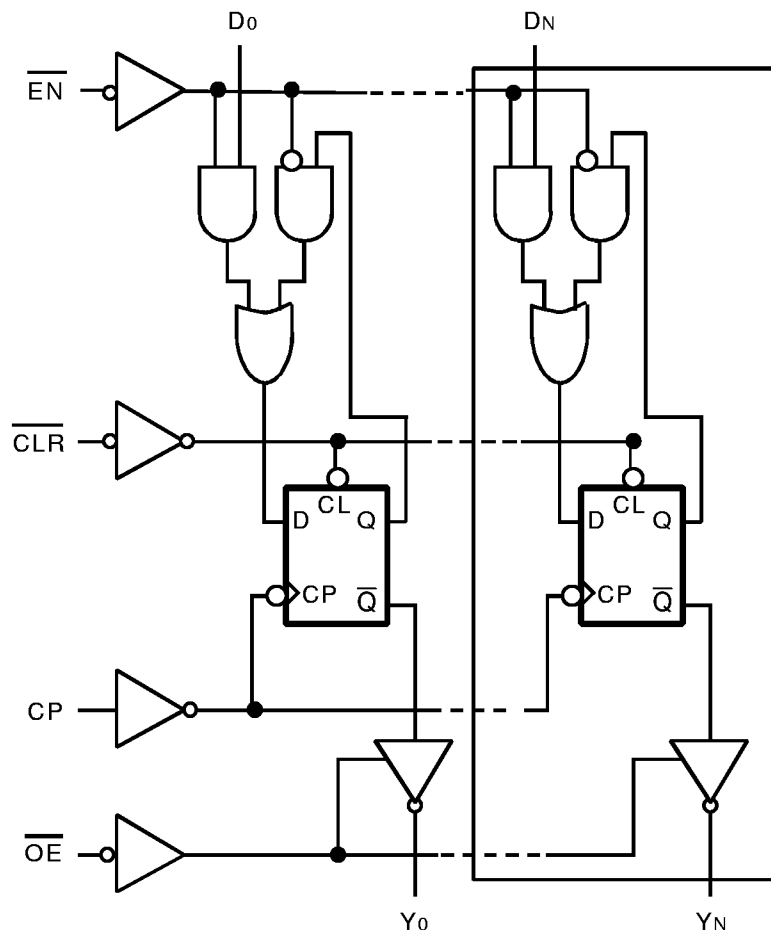
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- Extended commercial range of -40°C to $+85^\circ\text{C}$
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Available in PDIP, SOIC, SSOP, and QSOP packages
- A, B, C and D speed grades
- High drive outputs (-15mA IOH, 48mA IOL)
- Power off disable outputs permit "live insertion"

DESCRIPTION:

The FCT823T series is built using an advanced dual metal CMOS technology. The FCT823T series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT823T are 9-bit wide buffered registers with Clock Enable ($\overline{\text{EN}}$) and Clear ($\overline{\text{CLR}}$) – ideal for parity bus interfacing in high-performance microprogrammed systems.

The FCT823T high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

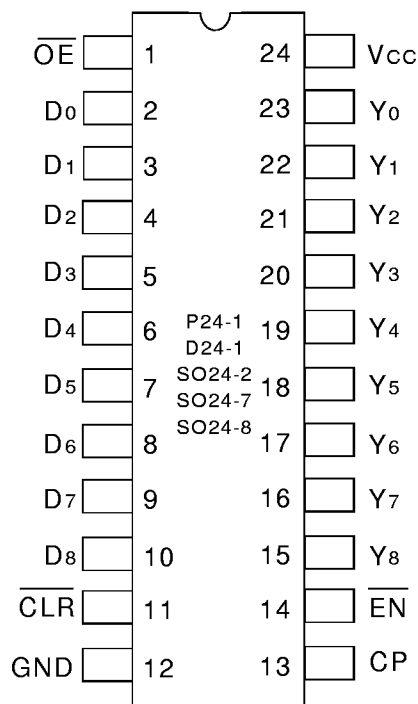
FUNCTIONAL BLOCK DIAGRAM



COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1999

PIN CONFIGURATION



PDIP/ SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-65 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Names	I/O	Description
D _i	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	When the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q _i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y _i	O	The register 3-state outputs.
$\overline{\text{EN}}$	I	Clock Enable. When the clock enable is LOW, data on the D _i input is transferred to the Q _i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q _i outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y _i outputs are in the high-impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y _i outputs.

FUNCTION TABLE (1)

Inputs					Internal/Outputs		Function
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D _i	CP	Q _i	Y _i	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

- H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ $V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	
I_{OZH}	High Impedance Output Current (3-State Output Pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$ $V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_H	Input Hysteresis	—	—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	-60	-120	-225	mA	
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$	—	—	± 1	μA	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE} = \overline{EN} = GND$ One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	1.5	3.5	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2	5.5	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE} = \overline{EN} = GND$ Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	3.8	7.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6	16.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

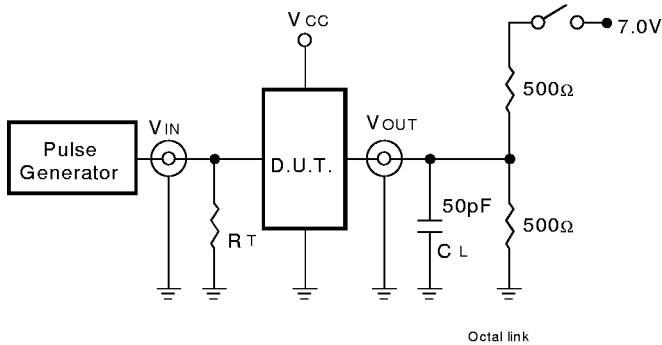
Symbol	Parameter	Condition ⁽¹⁾	FCT823AT		FCT823BT		FCT823CT		FCT823DT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Y _i ($\overline{OE} = \text{LOW}$)	CL = 50pF RL = 500Ω	1.5	10	1.5	7.5	1.5	6	1.5	5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	20	1.5	15	1.5	12.5	1.5	8.5	
tsu	Set-up Time HIGH or LOW Di to CP	CL = 50pF RL = 500Ω	4	—	3	—	3	—	2	—	ns
tH	Hold Time HIGH or LOW Di to CP		2	—	1.5	—	1.5	—	1	—	ns
tsu	Set-up Time HIGH or LOW \overline{EN} to CP		4	—	3	—	3	—	3	—	ns
tH	Hold Time HIGH or LOW \overline{EN} to CP		2	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, \overline{CLR} to Y _i		1.5	14	1.5	9	1.5	8	1.5	5	ns
tREM	Recovery Time \overline{CLR} to CP		6	—	6	—	6	—	3	—	ns
tw	Clock Pulse Width HIGH or LOW		7	—	6	—	6	—	3	—	ns
tw	\overline{CLR} Pulse Width LOW		6	—	6	—	6	—	3	—	ns
tPZH tPZL	Output Enable Time \overline{OE} to Y _i	CL = 50pF RL = 500Ω	1.5	12	1.5	8	1.5	7	1.5	4.8	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23	1.5	15	1.5	12.5	1.5	9	
tPHZ tPLZ	Output Disable Time \overline{OE} to Y _i	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7	1.5	6.5	1.5	6	1.5	4	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	7.5	1.5	6.5	1.5	4	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

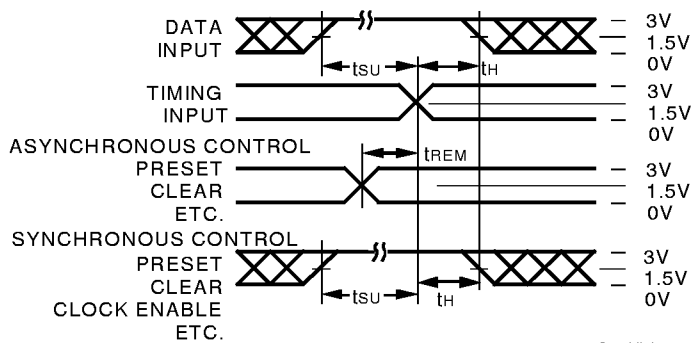
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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

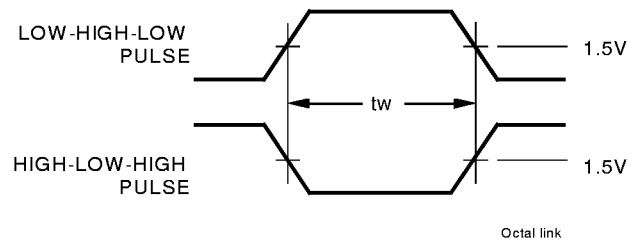
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



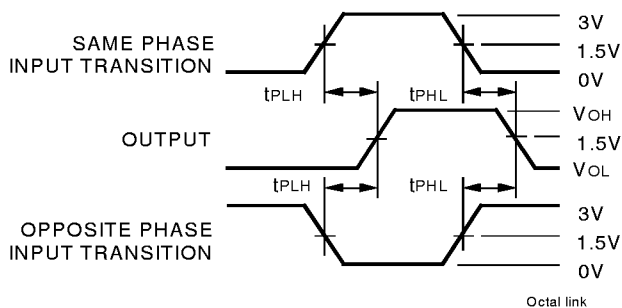
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PULSE WIDTH



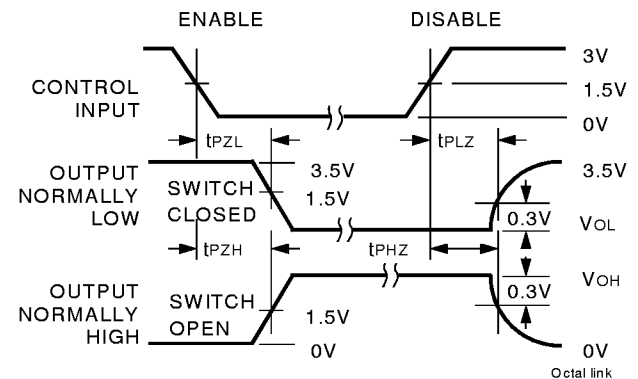
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

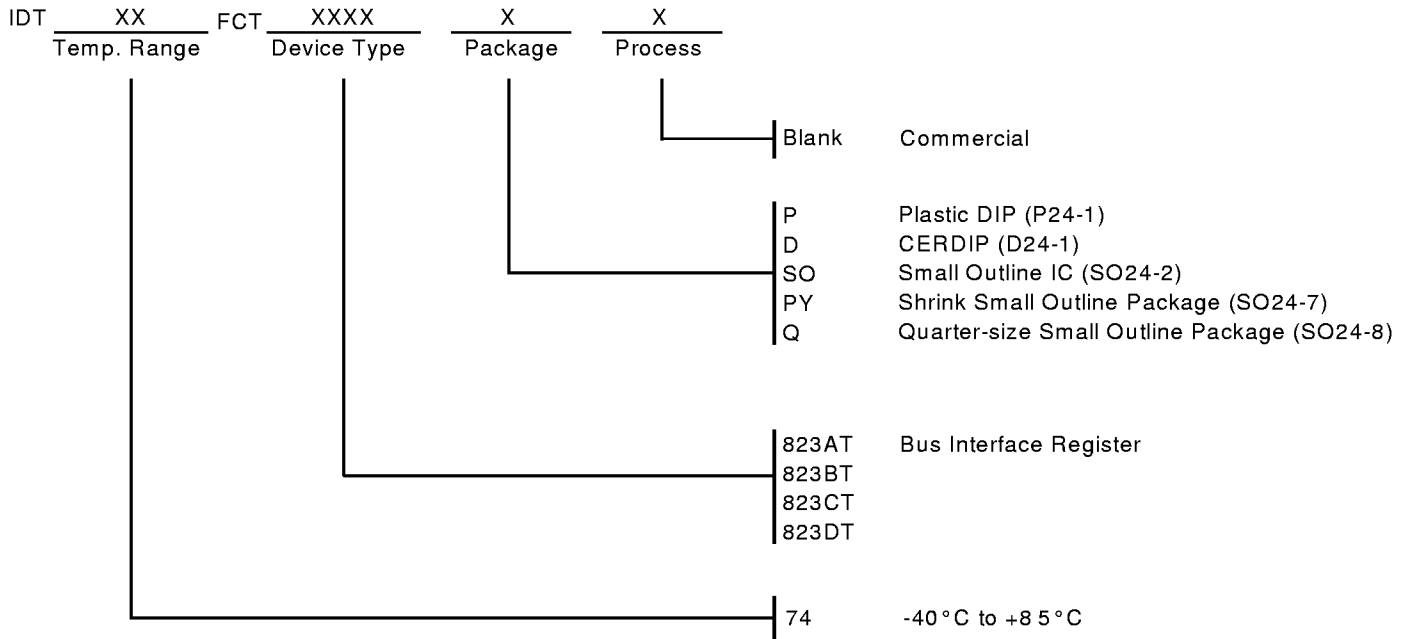


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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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