

February 1998

Fast CMOS 16-Bit Bidirectional Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **$V_{CC} = 5V \pm 10\%$**
- **Hysteresis on All Inputs**
- **CD74FCT16245T**
 - **High Output Drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$**
 - **Power Off Disable Outputs Permit "Live Insertion"**
 - **Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$**
- **CD74FCT162245T**
 - **Balanced Output Drivers: $\pm 24mA$**
 - **Reduced System Switching Noise**
 - **Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$**
- **CD74FCT162H245T**
 - **Bus Hold Retains Last Active Bus State During Three-State**
 - **Eliminates the Need for External Pull-up Resistors**

Description

These devices are 16-bit bidirectional transceivers designed for asynchronous two-way communication between data buses. The direction control input pin (χ_{DIR}) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74FCT16245T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers. The CD74FCT162245T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H245T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

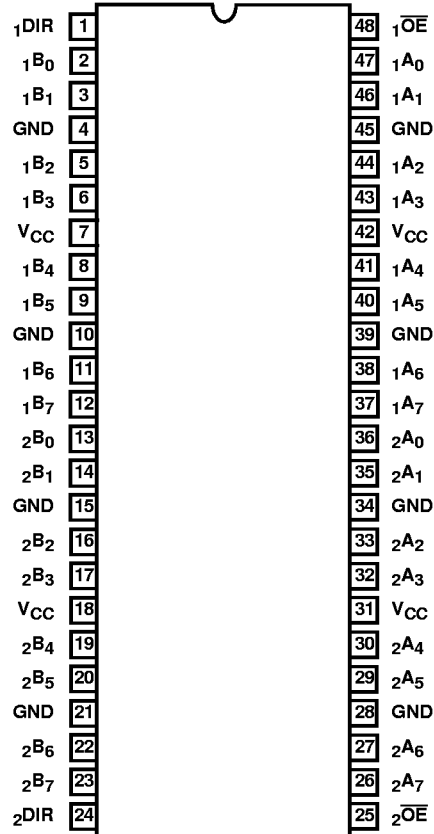
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16245ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162H245ATMT	-40 to 85	48 Ld TSSOP	M56.240P
CD74FCT162H245ATSM	-40 to 85	48 Ld SSOP	M56.300P
CD74FCT162H245CTMT	-40 to 85	48 Ld TSSOP	M56.240P
CD74FCT162H245CTSM	-40 to 85	48 Ld SSOP	M56.300P
CD74FCT162H245DTMT	-40 to 85	48 Ld TSSOP	M56.240P
CD74FCT162H245DTSM	-40 to 85	48 Ld SSOP	M56.300P
CD74FCT162H245ETMT	-40 to 85	48 Ld TSSOP	M56.240P
CD74FCT162H245ETSM	-40 to 85	48 Ld SSOP	M56.300P
CD74FCT162H245TSM	-40 to 85	48 Ld SSOP	M56.300P
CD74FCT162H245TMT	-40 to 85	48 Ld TSSOP	M56.240P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

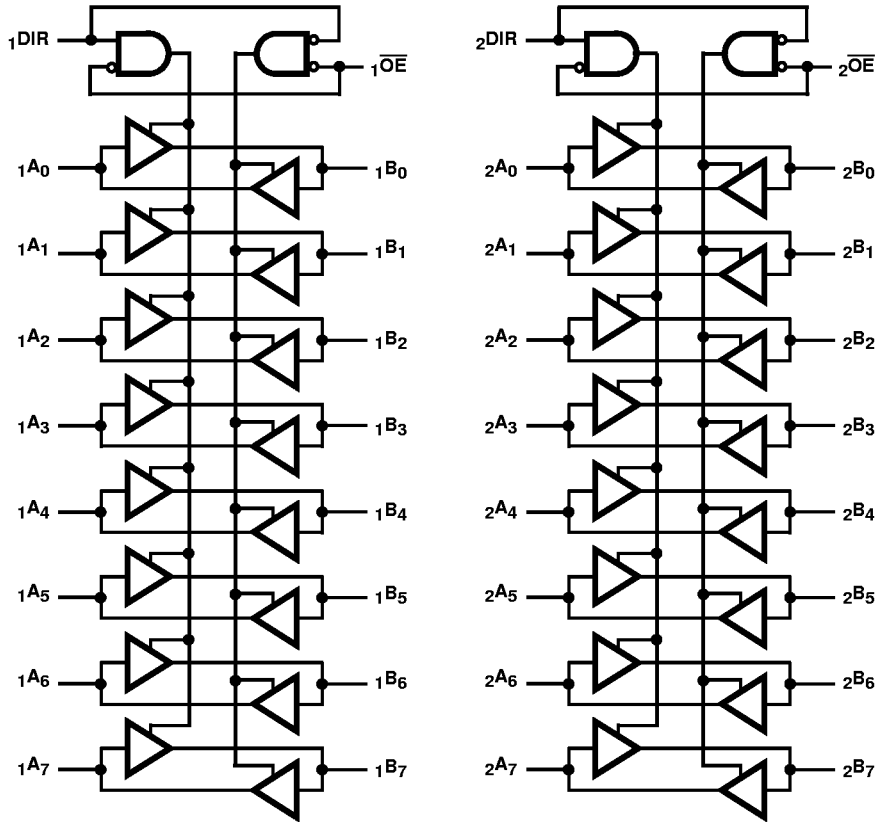
CD74FCT16245T, CD74FCT162245T, CD74FCT162H245T

Pinout

CD74FCT16245T, CD74FCT162245T, CD74FCT162H245T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
\overline{xOE}	$xDIR$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{xOE}	Three-State Output Enable Inputs (Active LOW)
$xDIR$	Direction Control Input
xAx	Side A Inputs or Three-State Outputs (Note 2)
xBx	Side B Inputs or Three-State Outputs (Note 2)
GND	Ground
V_{CC}	Power

NOTE:

- 2. For the CD74FCT162H245T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

CD74FCT16245T, CD74FCT162245T, CD74FCT162H245T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
 TSSOP Package 94
 SSOP Package 76
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10%						
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level	2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level	-	-	0.8	V
Input HIGH Current	I _{IH}	Standard Input (Note 7) V _{CC} = Max			1	μA
Input HIGH Current	I _{IH}	Standard I/O (Note 7) V _{CC} = Max			1	μA
Input HIGH Current	I _{IH}	Bus Hold Input (Note 8) V _{CC} = Max			±100	μA
Input HIGH Current	I _{IH}	Bus Hold I/O (Note 8) V _{CC} = Max			±100	μA
Input LOW Current	I _{IL}	Standard Input (Note 7) V _{CC} = Min			-1	μA
Input LOW Current	I _{IL}	Standard I/O (Note 7) V _{CC} = Min			-1	μA
Input LOW Current	I _{IL}	Bus Hold Input (Note 8) V _{CC} = Min			±100	μA
Input LOW Current	I _{IL}	Bus Hold I/O (Note 8) V _{CC} = Min			±100	μA
Bus Hold Sustain Current	I _{BHH}	Bus Hold Input (Note 8) V _{CC} = Min	V _{IN} = 2.0V	-50	-	μA
	I _{BHL}		V _{IN} = 0.8V	50	-	μA
High Impedance Output Current (Three-State) (Note 9)	I _{OZH}	V _{CC} = Max			1	μA
	I _{OZL}	V _{CC} = Max			-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA	-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 6), V _{OUT} = GND	-80	-140	-200	mA
Output Drive Current	I _O	V _{CC} = Max (Note 6), V _{OUT} = 2.5V	-50	-	-180	mA
Input Hysteresis	V _H		-	100	-	mV

CD74FCT16245T, CD74FCT162245T, CD74FCT162H245T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
CD74FCT16245T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0mA	2.5	3.5	-	V
			I _{OH} = -15.0mA	2.4	3.5	-	V
			I _{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I _{OFF}	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	-	-	±100	μA	
CD74FCT162245T, CD74FCT162H245T, OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I _{ODL}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6)	-	60	115	150	mA
Output HIGH Current	I _{ODH}	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6)	-60	-115	-150	mA	
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C _{IN}	V _{IN} = 0V	-	4.5	6	pF	
Output Capacitance (Note 10)	C _{OUT}	V _{OUT} = 0V	-	5.5	8	pF	
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I _{CCD}	V _{CC} = Max, Outputs Open χ _{OE} = χ _{DIR} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	60	100	μA/ MHz
Total Power Supply Current (Note 14)	I _C	V _{CC} = Max, Outputs Open f _I = 10MHz, 50% Duty Cycle χ _{OE} = χ _{DIR} = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	0.6	1.5 (Note 13)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	0.9	2.3 (Note 13)	mA
		V _{CC} = Max, Outputs Open f _I = 2.5MHz 50% Duty Cycle χ _{OE} = χ _{DIR} = GND 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	2.4	4.5 (Note 13)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	6.4	16.5 (Note 13)	mA

CD74FCT16245T, CD74FCT162245T, CD74FCT162H245T

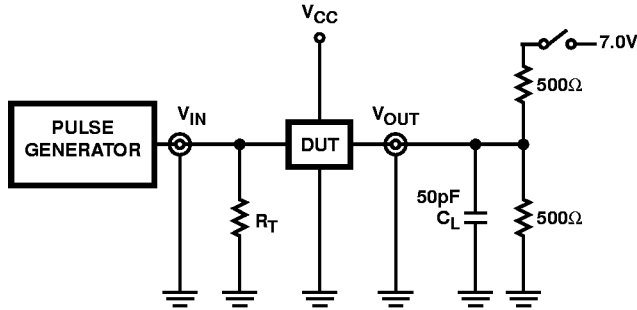
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 16) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	1.5	3.2	ns
Output Enable Time $\chi\overline{OE}$ to A or B	t_{PZH} , t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.4	ns
Output Disable Time (Note 17) $\chi\overline{OE}$ to A or B	t_{PHZ} , t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Enable Time χDIR to A or B (Note 17)	t_{PZH} , t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.8	ns
Output Disable Time χDIR to A or B (Note 17)	t_{PHZ} , t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Skew (Note 18)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading, except as noted.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
8. Pins with Bus Hold are identified in the pin description.
9. This specification does not apply to bidirectional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



NOTE:

19. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$; $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

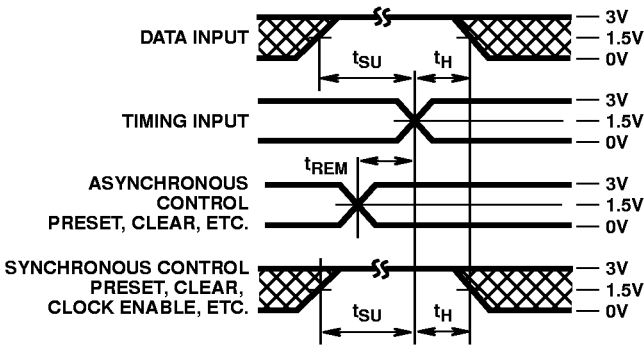


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

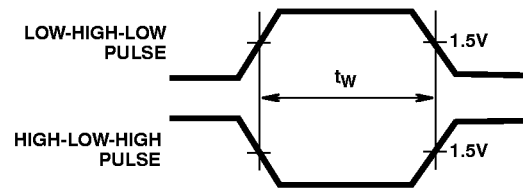


FIGURE 3. PULSE WIDTH

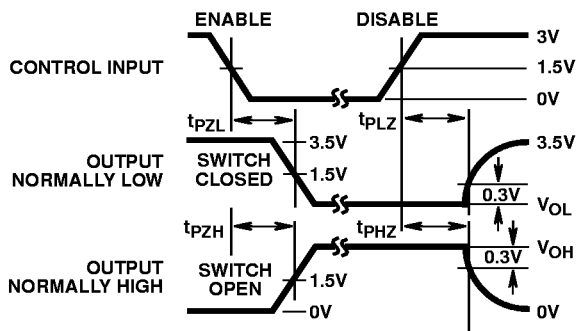


FIGURE 4. ENABLE AND DISABLE TIMING

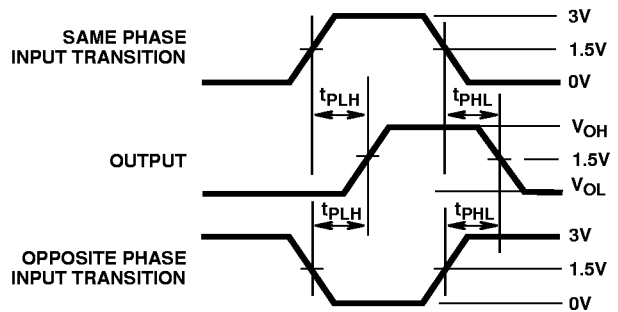


FIGURE 5. PROPAGATION DELAY