



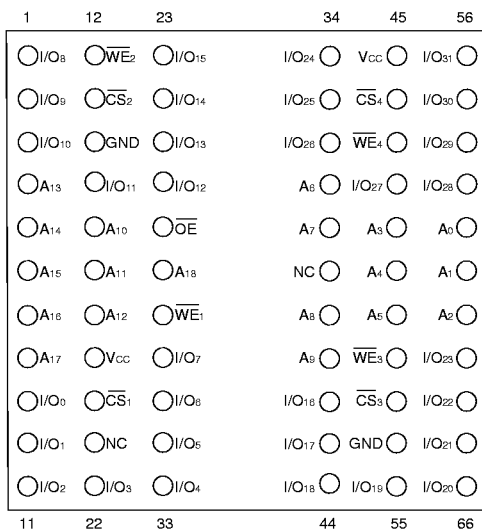
512Kx32 SRAM MODULE, SMD 5962-94611 PRELIMINARY*

FEATURES

- Access Times of 17, 20, 25, 35, 45, 55ns
- Packaging
 - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400).
 - 66 pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402).
 - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502), Package to be developed.
 - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square (Package 509) 4.57mm (0.180 inch) height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32-XH1X - 13 grams typical
 - WS512K32-XH2X - 13 grams typical
 - WS512K32-XG2TX - 13 grams typical
 - WS512K32-XG4TX - 20 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH1X AND WS512K32N-XH2X



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
\overline{WE}_{1-4}	Write Enables
\overline{CS}_{1-4}	Chip Selects
\overline{OE}	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

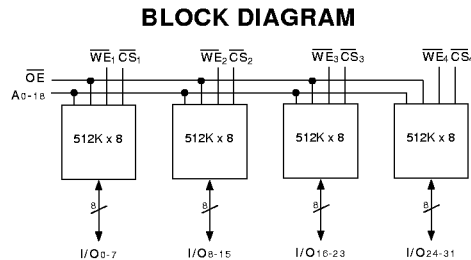




FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4TX

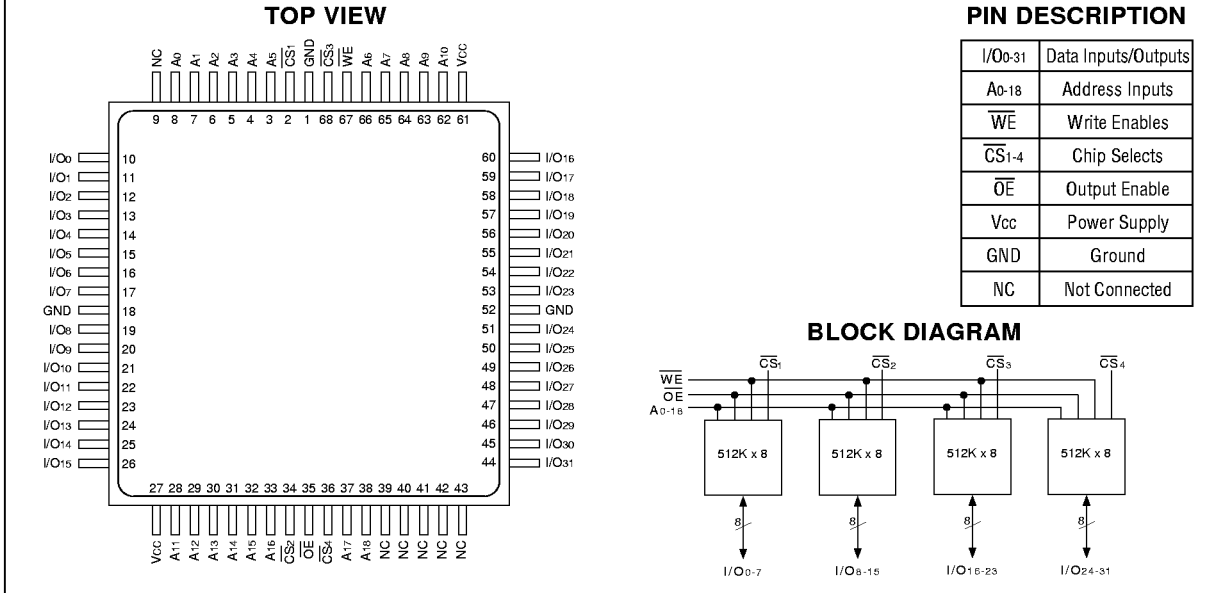
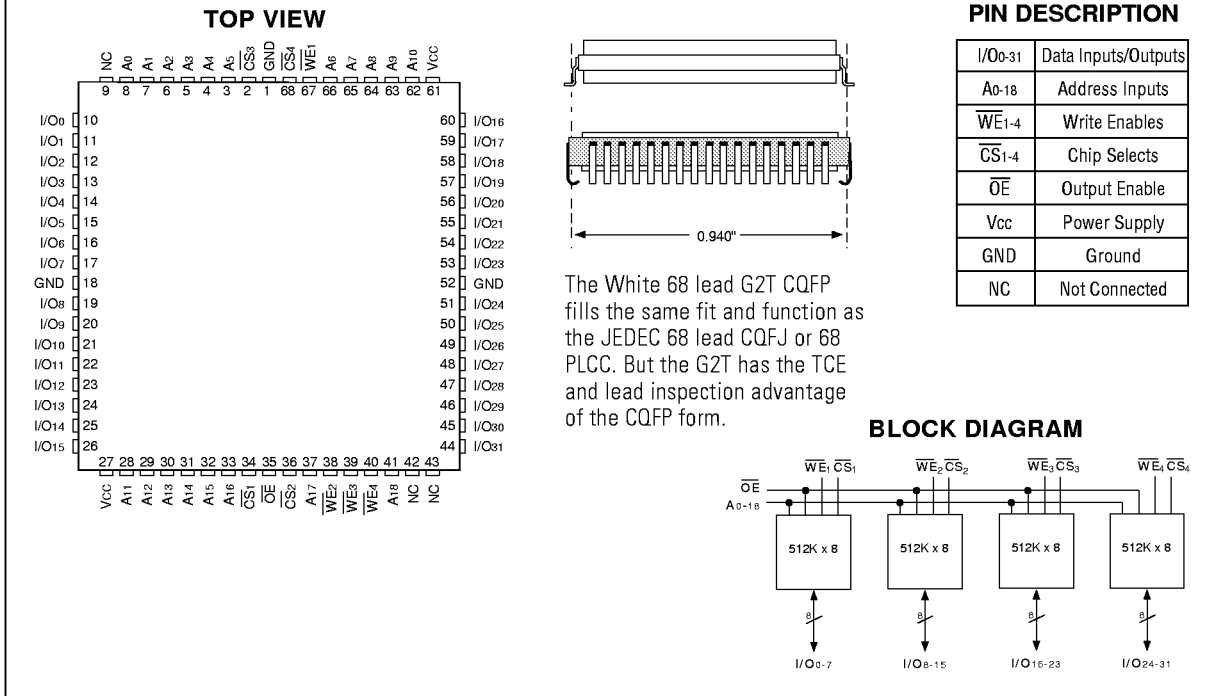


FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2TX



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{stg}	-65	+150	°C
Signal Voltage Relative to GND	V _g	-0.5	V _{cc} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{cc}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{cc}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{cc} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T _A	-55	+125	°C

TRUTH TABLE

\overline{CS}	\overline{OE}	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
\overline{WE} 1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2T			20	
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{cc} = 5.0V, V_{ss} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units		
			Min	Max	
Input Leakage Current	I _{LI}	V _{cc} = 5.5, V _{IN} = GND to V _{cc}		10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{cc}		10	μA
Operating Supply Current x 32 Mode	I _{CC x 32}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{cc} = 5.5		540	mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{cc} = 5.5		60	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA for 17 - 35ns, I _{OL} = 2.1mA for 45 - 55ns, V _{cc} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA for 17 - 35ns, I _{OH} = -1.0mA for 45 - 55ns, V _{cc} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{cc} - 0.3V, V_{IL} = 0.3V**DATA RETENTION CHARACTERISTICS**(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units			
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{cc} - 0.2V$	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{cc} = 3V		3.2	28*	mA

* Also available in Low Power version, please call factory for information.



AC CHARACTERISTICS

(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Table with 14 columns: Parameter, Symbol, and two columns for temperature ranges (-17, -20, -25, -35, -45, -55) with Min and Max values, and a Units column. Rows include Read Cycle Time, Address Access Time, Output Hold from Address Change, Chip Select Access Time, Output Enable to Output Valid, Chip Select to Output in Low Z, Output Enable to Output in Low Z, Chip Disable to Output in High Z, and Output Disable to Output in High Z.

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

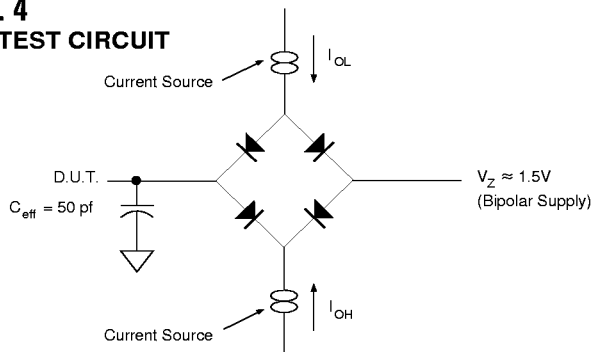
(Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Table with 14 columns: Parameter, Symbol, and two columns for temperature ranges (-17, -20, -25, -35, -45, -55) with Min and Max values, and a Units column. Rows include Write Cycle Time, Chip Select to End of Write, Address Valid to End of Write, Data Valid to End of Write, Write Pulse Width, Address Setup Time, Address Hold Time, Output Active from End of Write, Write Enable to Output in High Z, and Data Hold Time.

1. This parameter is guaranteed by design but not tested.

2. The Address Setup Time of minimum 2ns is for the G2 and H2 packages. tas minimum for G4 and G4T packages is 0ns.

FIG. 4 AC TEST CIRCUIT



AC TEST CONDITIONS

Table with 3 columns: Parameter, Typ, and Unit. Rows include Input Pulse Levels (VIL = 0, VIH = 3.0 V), Input Rise and Fall (5 ns), Input and Output Reference Level (1.5 V), and Output Timing Reference Level (1.5 V).

NOTES: Vz is programmable from -2V to +7V. IOL & IOH programmable from 0 to 16mA. Tester Impedance Z0 = 75 Ω. Vz is typically the midpoint of VOH and VOL. IOL & IOH are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.



FIG. 5
TIMING WAVEFORM - READ CYCLE

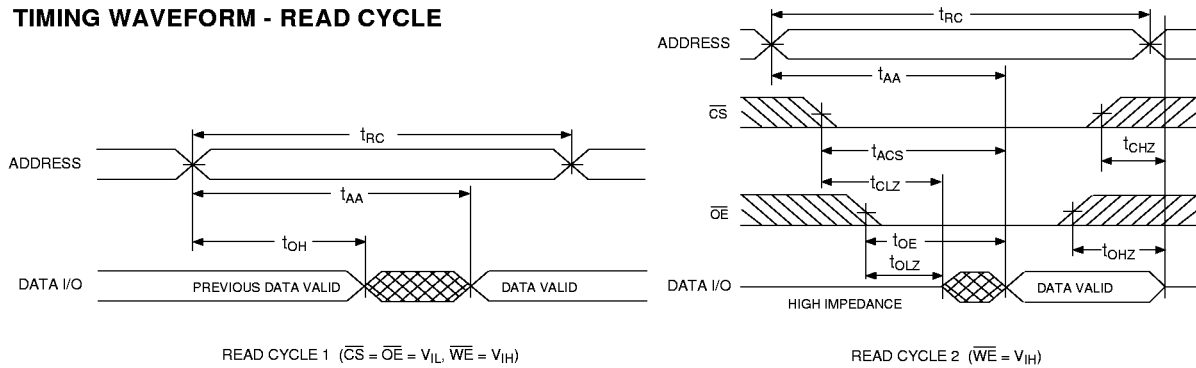


FIG. 6
WRITE CYCLE - \overline{WE} CONTROLLED

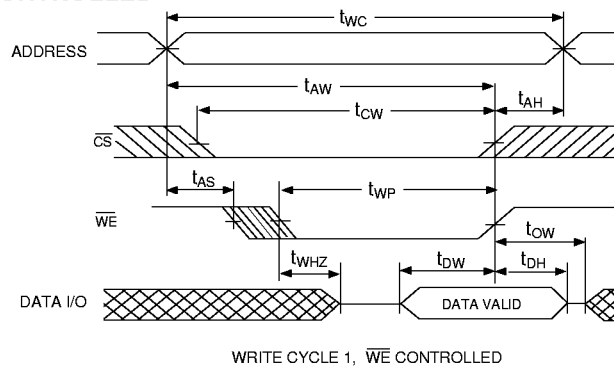
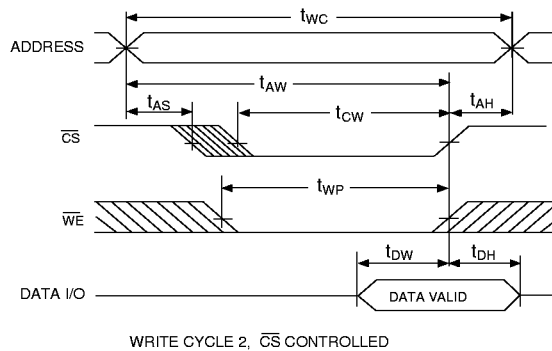
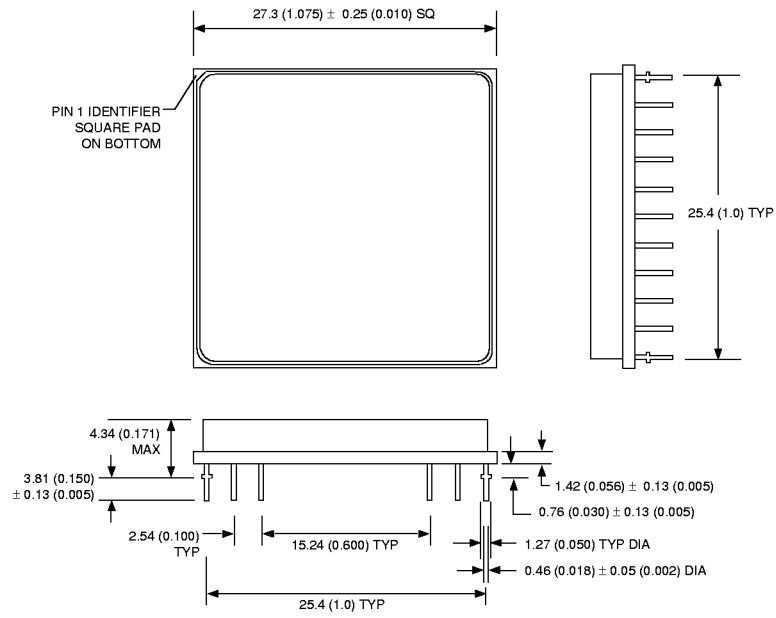


FIG. 7
WRITE CYCLE - \overline{CS} CONTROLLED



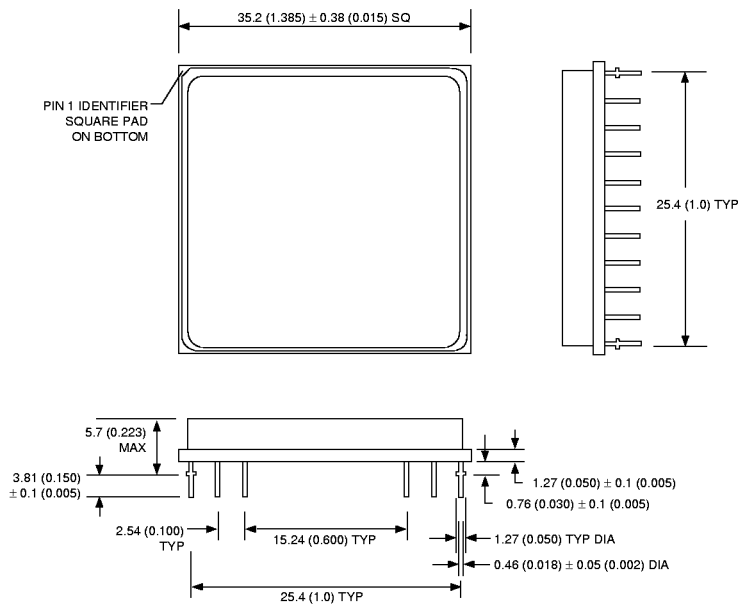


PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

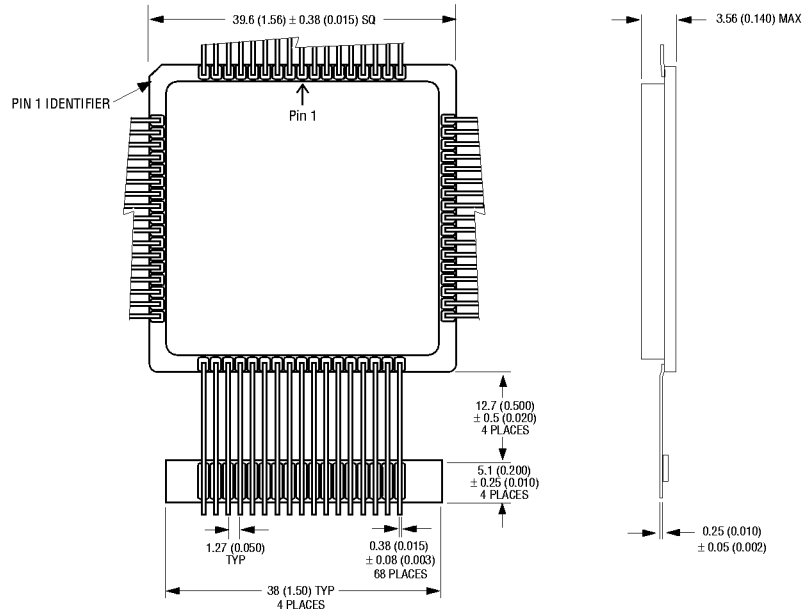
PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



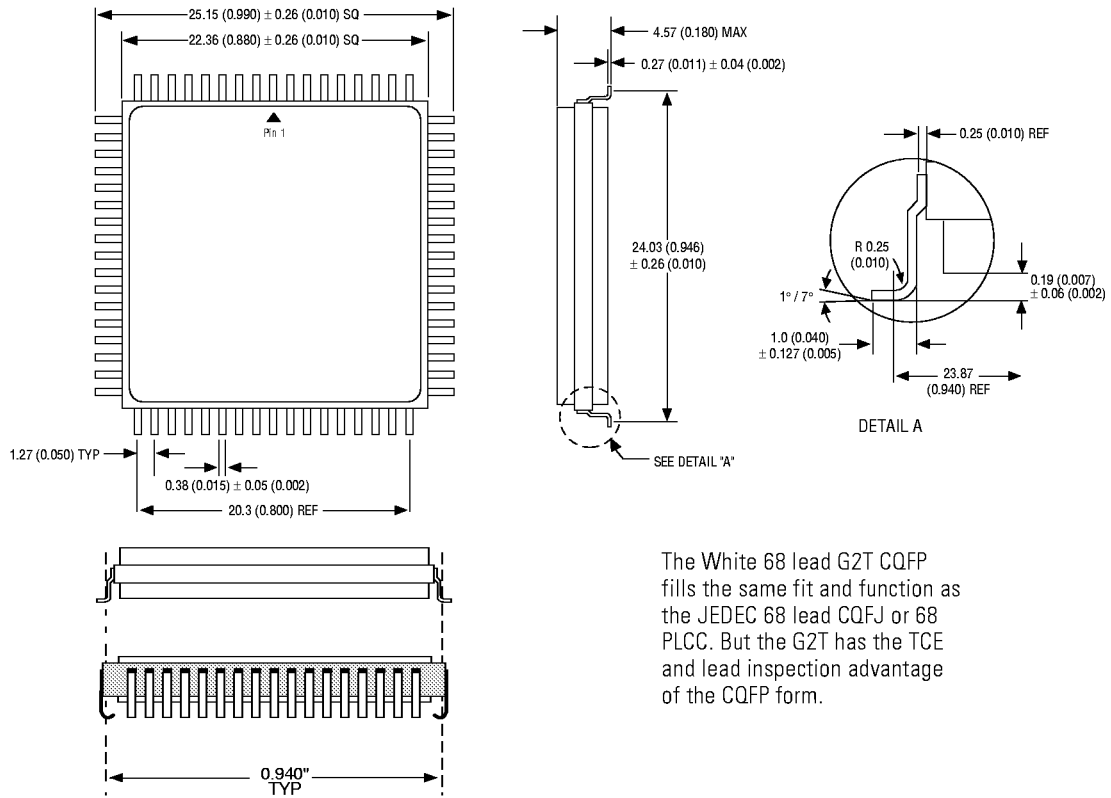
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 512K 32 X - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to 85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H1 = Ceramic Hex-In-line Package, HIP (Package 400)
- H2 = Ceramic Hex-In-line Package, HIP (Package 402)
- G2T = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 509)
- G4T = 40mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:

- N = No Connect at pin 21 and 39 in HIP for Upgrades

ORGANIZATION, 512Kx32

- User configurable as 1Mx16 or 2Mx8

SRAM

WHITE MICROELECTRONICS



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	55ns	66 pin HIP (H2)	5962-94611 05HXX
512K x 32 SRAM Module	45ns	66 pin HIP (H2)	5962-94611 06HXX
512K x 32 SRAM Module	35ns	66 pin HIP (H2)	5962-94611 07HXX
512K x 32 SRAM Module	25ns	66 pin HIP (H2)	5962-94611 08HXX
512K x 32 SRAM Module	20ns	66 pin HIP (H2)	5962-94611 09HXX
512K x 32 SRAM Module	17ns	66 pin HIP (H2)	5962-94611 10HXX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP/J (G2T)	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP/J (G2T)	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP/J (G2T)	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP/J (G2T)	5962-94611 08HMX
512K x 32 SRAM Module	20ns	68 lead CQFP/J (G2T)	5962-94611 09HMX
512K x 32 SRAM Module	17ns	68 lead CQFP/J (G2T)	5962-94611 10HMX