

PRELIMINARY

# MITSUBISHI LSIs M5M418160CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

## FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418160CXX-5,-5S	50	13	25	13	90	810
M5M418160CXX-6,-6S	60	15	30	15	110	675
M5M418160CXX-7,-7S	70	20	35	20	130	585

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V  $\pm$ 10% supply
- Low stand-by power dissipation  
5.5mW (Max) ----- CMOS Input level
- Low operating power dissipation  
M5M418160Cxx-5,-5S ----- 990.0mW (Max)  
M5M418160Cxx-6,-6S ----- 825.0mW (Max)  
M5M418160Cxx-7,-7S ----- 715.0mW (Max)
- Fast-page mode, Read-modify-write, RAS-only refresh  
CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance  
All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A<sub>0</sub>-A<sub>9</sub>)  
\* : Applicable to self refresh version (M5M418160CJ,TP-5S,-6S,-7S : option) only

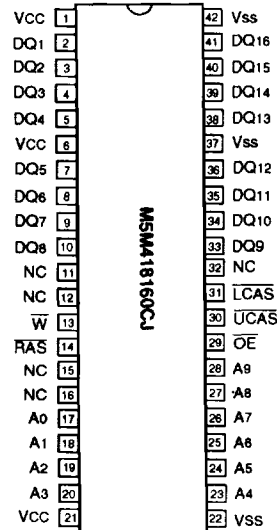
## APPLICATION

Main memory unit for computers, Microcomputer memory,  
Refresh memory for CRT

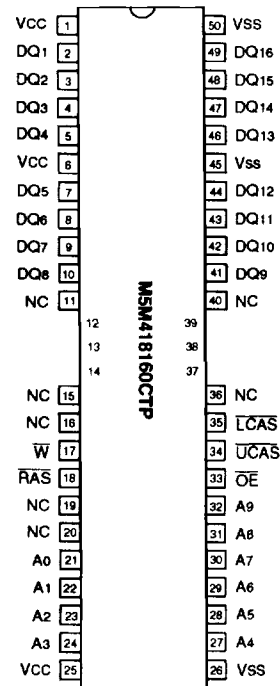
## PIN DESCRIPTION

Pin name	Function
A <sub>0</sub> -A <sub>9</sub>	Address inputs
DQ <sub>1</sub> -DQ <sub>16</sub>	Data inputs/outputs
RAS	Row address strobe input
UCAS	Upper byte control column address strobe input
LCAS	Lower byte control column address strobe input
$\bar{W}$	Write control input
$\bar{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

## PIN CONFIGURATION (TOP VIEW)



Outline 42P0N-A (400mil SOJ)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

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# M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S

## FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

### FUNCTION

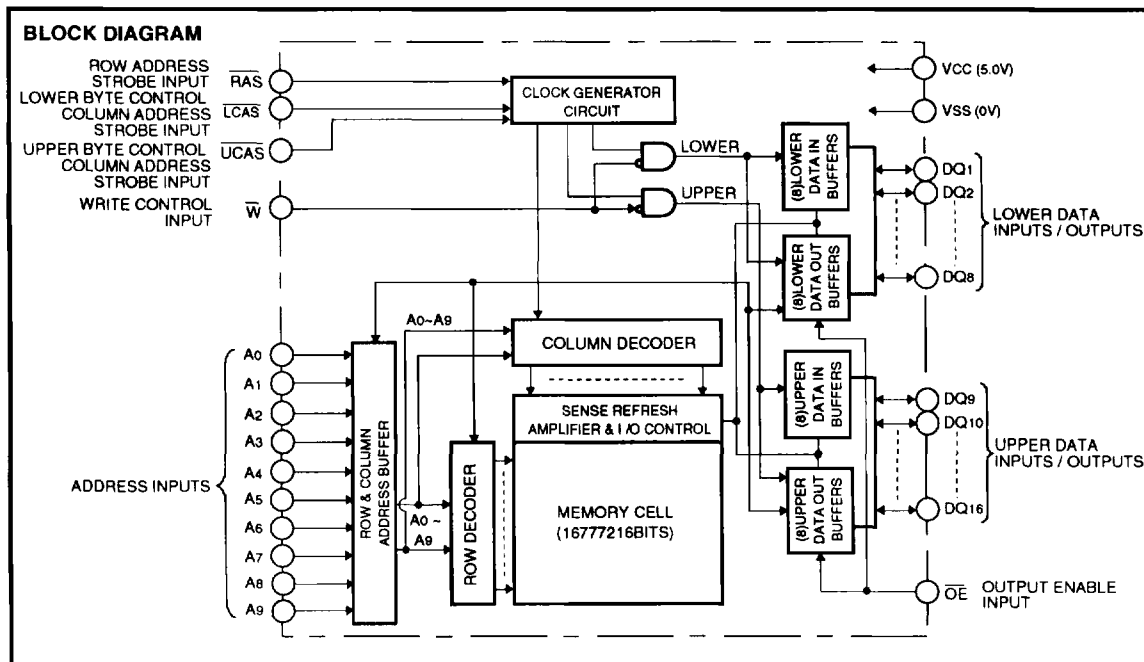
The M5M418160CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g.,

fast page mode,  $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	RAS	LCAS	UCAS	W	$\overline{\text{OE}}$	DQ1-DQ8	DQ9-DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



**PRELIMINARY**

Note: This is not a final specification.  
Some parameters may be subject to change without notice.

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to V <sub>ss</sub>	-1~7	V
V <sub>i</sub>	Input voltage		-1~7	V
V <sub>o</sub>	Output voltage		-1~7	V
I <sub>o</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25 °C	1000	mW
T <sub>opr</sub>	Operating temperature		0~70	°C
T <sub>stg</sub>	Storage temperature		-65~150	°C

**RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0~70°C, unless otherwise noted) (Note 1)**

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>cc</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>ss</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.4		6.0	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-1		0.8	V

Note 1: All voltage values are with respect to V<sub>ss</sub>.

**ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0~70°C, V<sub>cc</sub>=5.0V±10%, V<sub>ss</sub>=0V, unless otherwise noted) (Note 2)**

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-5mA	2.4		V <sub>cc</sub>	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =4.2mA	0		0.4	V	
I <sub>oz</sub>	Off-state output current	Q floating 0V ≤ V <sub>OUT</sub> ≤ 5.5V	-10		10	μA	
I <sub>i</sub>	Input current	0V ≤ V <sub>IN</sub> ≤ 6V, Other inputs pins=0V	-10		10	μA	
I <sub>CC1(AV)</sub>	Average supply current from V <sub>cc</sub> operating (Note 3,4,5)	M5M418160C-5, -5S	RAS, CAS cycling t <sub>RC</sub> =t <sub>WC</sub> =min. output open			180	mA
		M5M418160C-6, -6S				150	
		M5M418160C-7, -7S				130	
I <sub>CC2</sub>	Supply current from V <sub>cc</sub> , stand-by (Note 6)	RAS = CAS = V <sub>IH</sub> , output open			2	mA	
		RAS = CAS ≥ V <sub>cc</sub> - 0.2V output open			1 0.3*		
I <sub>CC3(AV)</sub>	Average supply current from V <sub>cc</sub> refreshing (Note 3,5)	M5M418160C-5, -5S	RAS cycling, CAS = V <sub>IH</sub> t <sub>RC</sub> =min. output open			180	mA
		M5M418160C-6, -6S				150	
		M5M418160C-7, -7S				130	
I <sub>CC4(AV)</sub>	Average supply current from V <sub>cc</sub> Fast-page-mode (Note 3,4,5)	M5M418160C-5, -5S	RAS = V <sub>IL</sub> , CAS cycling t <sub>PC</sub> =min. output open			80	mA
		M5M418160C-6, -6S				70	
		M5M418160C-7, -7S				65	
I <sub>CC8(AV)</sub>	Average supply current from V <sub>cc</sub> CAS before RAS refresh mode (Note 3)	M5M418160C-5, -5S	CAS before RAS refresh cycling t <sub>RC</sub> =min. output open			180	mA
		M5M418160C-6, -6S				150	
		M5M418160C-7, -7S				130	
I <sub>CC8(AV)*</sub>	Average supply current from V <sub>cc</sub> Extended-refresh cycle (Note 6)	M5M418160C (S)	Stand-by: RAS ≥ V <sub>cc</sub> - 0.2V CAS ≥ V <sub>cc</sub> - 0.2V or CAS ≤ 0.2V CAS before RAS refresh: RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling W ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V OE ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V A0 ~ A9 ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V DQ=open, t <sub>RC</sub> =125 μs, t <sub>RAS</sub> =t <sub>RASmin.</sub> ~ 1 μs			500	μA
I <sub>CC9(AV)*</sub>	Average supply current from V <sub>cc</sub> Self-refresh cycle	M5M418160C (S)	RAS = CAS ≤ 0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1</sub> (AV), I<sub>CC3</sub> (AV) and I<sub>CC4</sub> (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I<sub>CC1</sub> (AV) and I<sub>CC4</sub> (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS = V<sub>IL</sub> and LCAS/UCAS = V<sub>IH</sub>.



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Notice: This circuit is not guaranteed to operate at the maximum rated frequency. Some parameters may vary with frequency.

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**CAPACITANCE** (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI(A)	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			5	pF
CI(OE)	Input capacitance, OE input				7	pF
CI(W)	Input capacitance, write control input				7	pF
CI(RAS)	Input capacitance, RAS input				7	pF
CI(CAS)	Input capacitance, CAS input				7	pF
CI/O	Input/Output capacitance, data ports				7	pF

**SWITCHING CHARACTERISTICS** (Ta=0~70 °C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7,8)		13		15		20	ns
tRAC	Access time from RAS (Note 7,9)		50		60		70	ns
tAA	Column address access time (Note 7,10)		25		30		35	ns
tCPA	Access time from CAS precharge (Note 7,11)		30		35		40	ns
tOEA	Access time from OE (Note 7)		13		15		20	ns
tCLZ	Output low impedance time from CAS low (Note 7)	5		5		5		ns
tOFF	Output disable time after CAS high (Note 12)	0	13	0	15	0	15	ns
tOEZ	Output disable time after OE high (Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 16.4ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IoH=5mA) / VOL=0.4V(IoL=4.2mA) load 100pF. The reference levels for measuring of output signal are 2.4V(VOH) and 0.4V(VOL).

8: Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max).

9: Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).

11: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).

12: tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT ≤ |±10 μA|) and is not reference to VOH(min) or VOL(max).



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**TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)**

(Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tREF*	Refresh cycle time		128		128		128	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	10		10		10		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	10		10		10		ns
tRAD	Column address delay time from RAS low (Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	13		15		15		ns
tDZC	Delay time, data to CAS low (Note 18)	0		0		0		ns
tDZO	Delay time, data to OE low (Note 18)	0		0		0		ns
tCDD	Delay time, CAS high to data (Note 19)	13		15		15		ns
tODD	Delay time, OE high to data (Note 19)	13		15		15		ns
tT	Transition time (Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed  $t_T = 5ns$ .

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) = tRAH(min) + 2tT + tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.

17: tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.

18: Either tDZC or tDZO must be satisfied.

19: Either tCDD or tODD must be satisfied.

20: tT is measured between VIH(min) and VIL(max).

**Read and Refresh Cycles**

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	50		60		70		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 21)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 21)	10		10		10		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tOCH	CAS hold time after OE low	13		15		20		ns
tORH	RAS hold time after OE low	13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	50		60		70		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tWCS	Write setup time before CAS low (Note 23)	0		0		0		ns
tWCH	Write hold time after CAS low	8		10		15		ns
tCWL	CAS hold time after W low	13		15		20		ns
tRWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	10		15		15		ns
tOEH	OE hold time after W low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note22)	131		155		180		ns
tRAS	RAS low pulse width	91	10000	105	10000	120	10000	ns
tCAS	CAS low pulse width	54	10000	60	10000	70	10000	ns
tCSH	CAS hold time after RAS low	91		105		120		ns
tRSH	RAS hold time after CAS low	54		60		70		ns
tRCS	Read setup time before CAS low	0		0		0		ns
tCWD	Delay time, CAS low to W low (Note 23)	36		40		45		ns
tRWD	Delay time, RAS low to W low (Note 23)	73		85		95		ns
tAWD	Delay time, address to W low (Note 23)	48		55		60		ns
tCWL	CAS hold time after W low	13		15		20		ns
tRWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before W low	0		0		0		ns
tDH	Data hold time after W low	10		10		15		ns
tOEH	OE hold time after W low	13		15		15		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5t.

23: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min), tAWD ≥ tAWD(min) and tCPWD ≥ tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	RAS low pulse width for read write cycle (Note 25)	85	125000	100	125000	115	125000	ns
tCP	CAS high pulse width (Note 26)	8	12	10	15	10	15	ns
tCPRH	RAS hold time after CAS precharge	30		35		40		ns
tCPWD	Delay time, CAS precharge to W low (Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: tRAS(min) is specified as two cycles of CAS input are performed.

26: tCP(max) is specified as a reference point only.



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**CAS before RAS Refresh Cycle** (Note 27)

Symbol	Parameter	Limits						Unit
		M5M418160C-5,-5S		M5M418160C-6,-6S		M5M418160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		10		ns
tCHR	CAS hold time after RAS low	10		10		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

**SELF REFRESH SPECIFICATIONS**

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

**TIMING REQUIREMENTS** (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418160C-5S		M5M418160C-6S		M5M418160C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh RAS low pulse width	100		100		100		μs
tRPS	Self refresh RAS high precharge time	90		110		130		ns
tCHS	Self refresh RAS hold time	- 50		- 50		- 50		ns

**SELF REFRESH ENTRY & EXIT CONDITIONS**

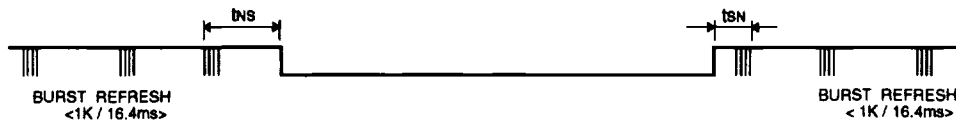
(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tns / tsn before / after self refresh, on the condition of tns ≤ 16.4ms and tsn ≤ 16.4ms.



(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tns / tsn before / after self refresh, on the condition of tns + tsn ≤ 16.4ms.



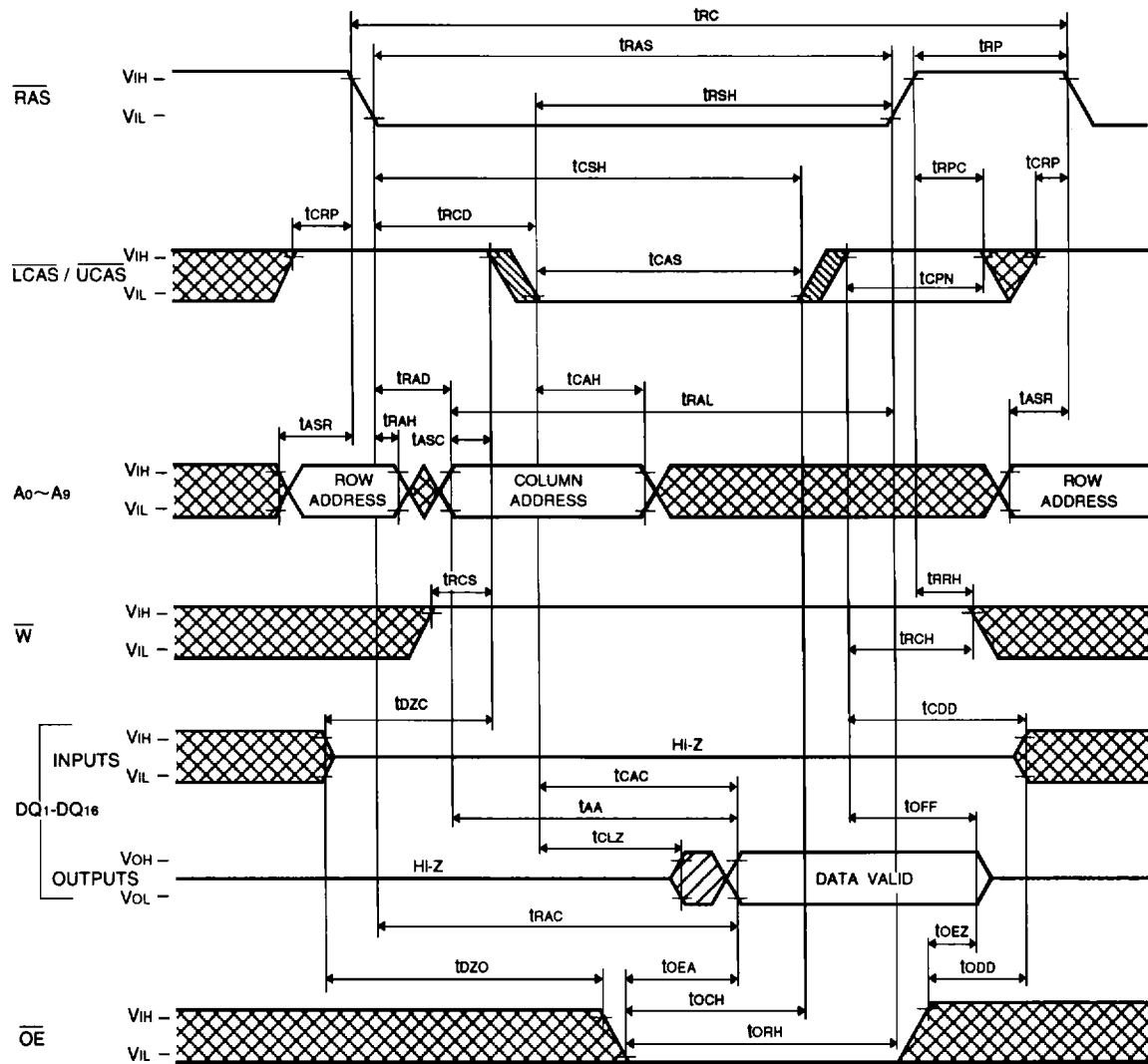
**PRELIMINARY**




**M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S**

Note: This is not a final specification.  
Some parameter limits are subject to change.

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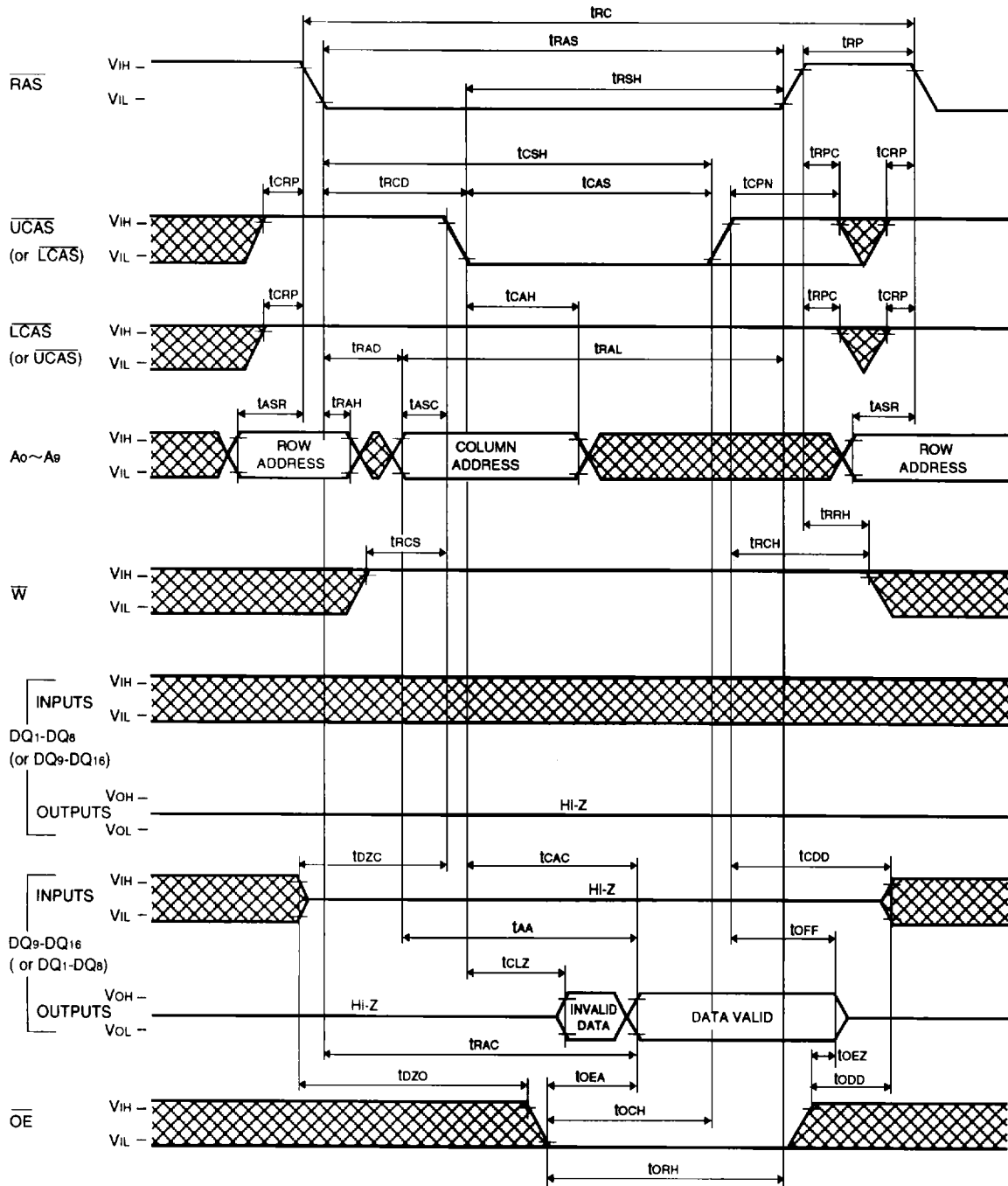
**Timing Diagrams (Note 28)**  
**Read Cycle**



- Note 28
-  Indicates the don't care input.  
 $V_{IH(min.)} \leq V_{IN} \leq V_{IH(max.)}$  or  $V_{IL(min.)} \leq V_{IN} \leq V_{IL(max.)}$
  -  Indicates the invalid output.
  -  Indicates the skew of the two inputs.



Upper / (Lower) Byte Read Cycle

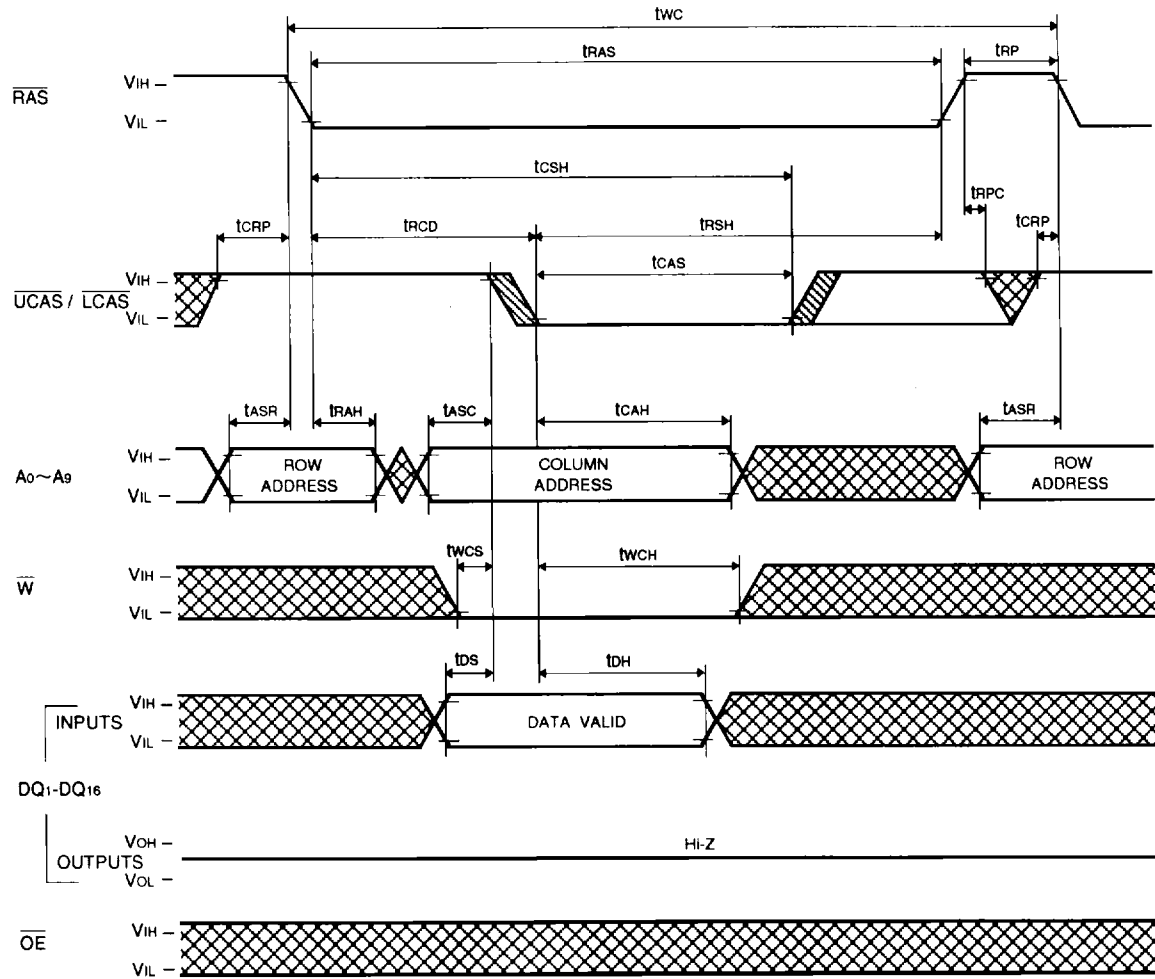


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M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

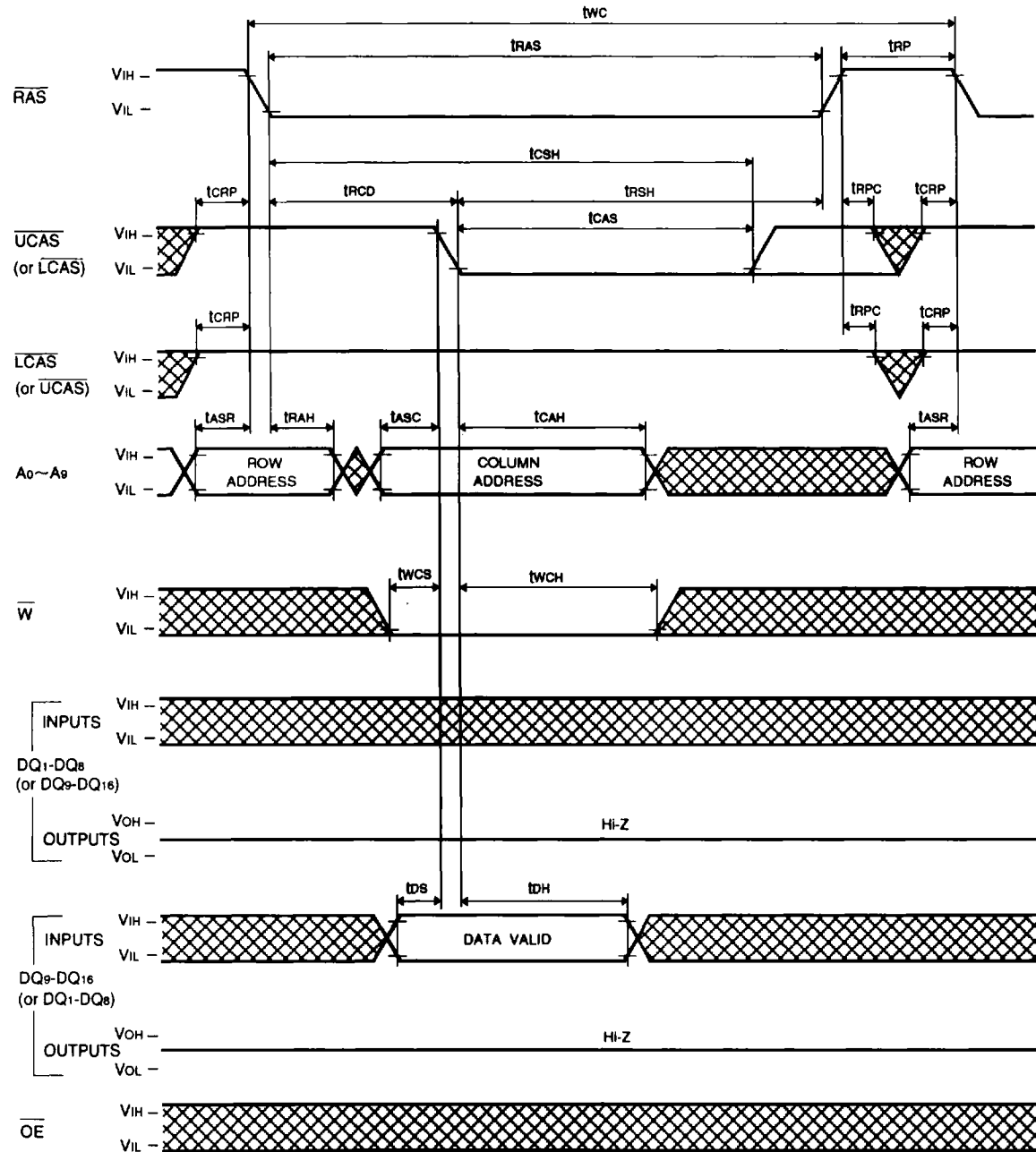
Write Cycle (Early write)



**PRELIMINARY**

Notice: This circuit is preliminary design.  
Some parameter limits are subject to change.

**Upper / (Lower) Byte Write Cycle (Early write)**



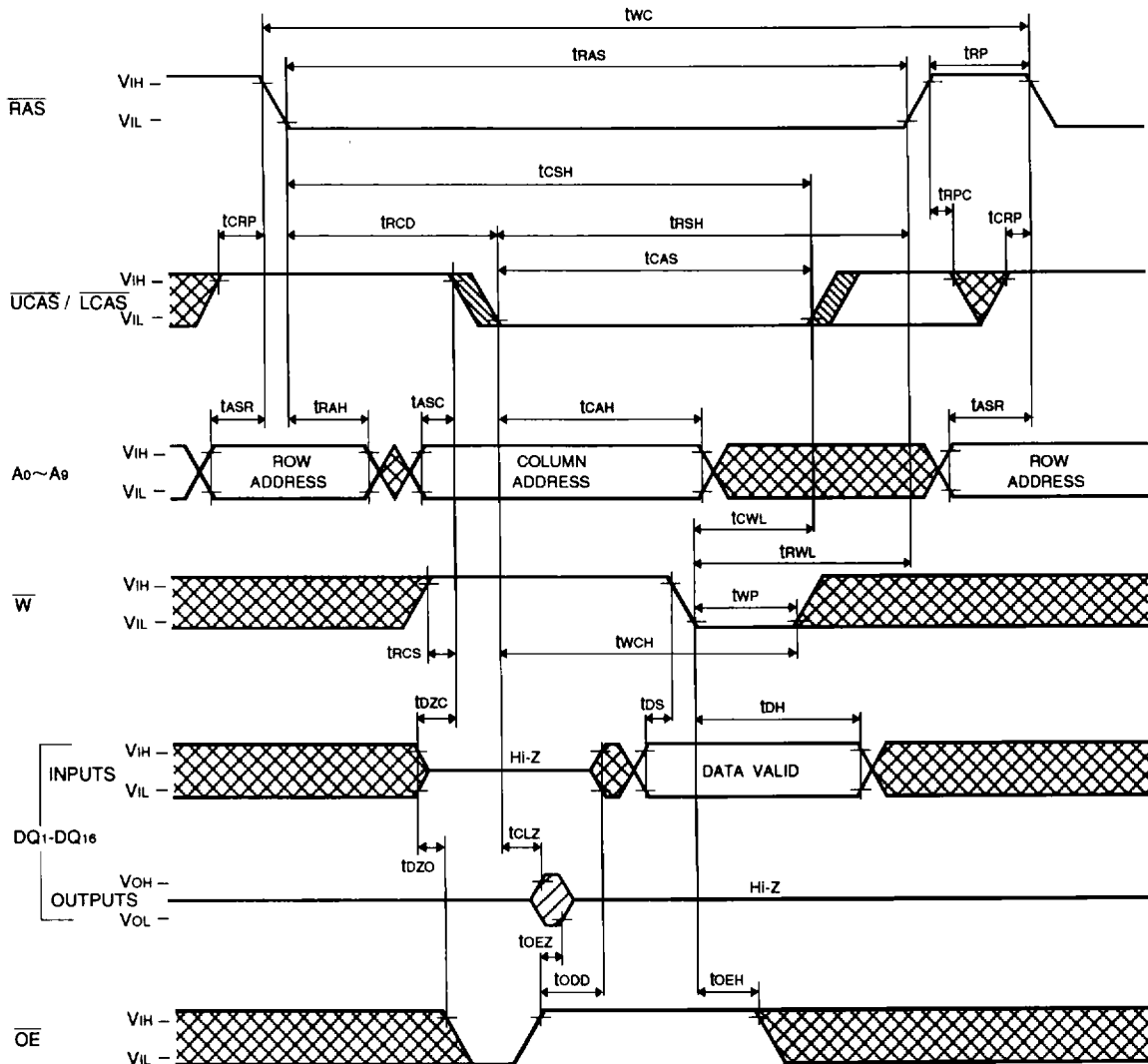
**PRELIMINARY**

**M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S**

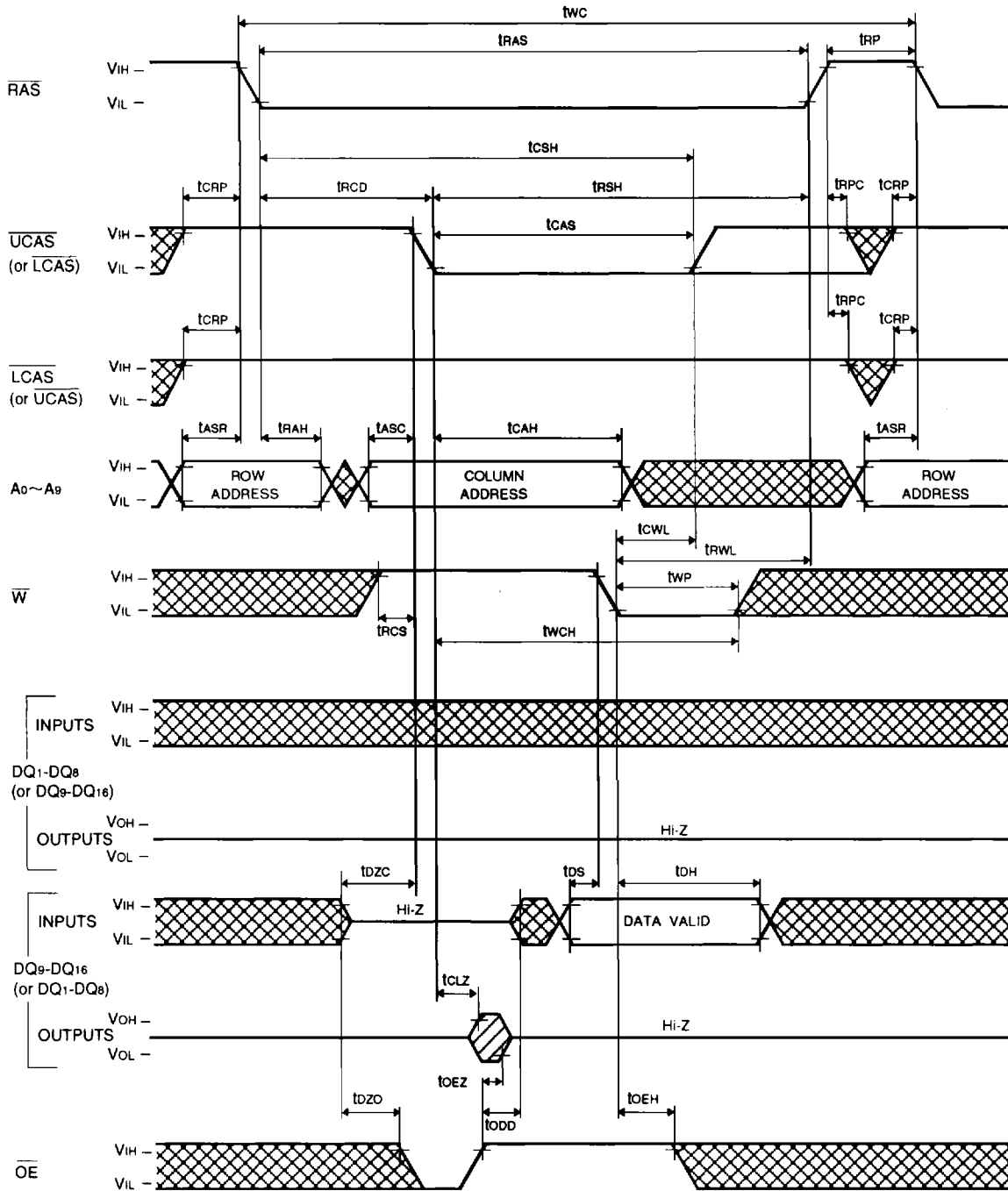
Note: The t<sub>1</sub> and t<sub>2</sub> test conditions are shown.  
Some parameter tests are subject to change.

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Write Cycle (Delayed write)**



Upper / (Lower) Byte Write Cycle (Delayed write)





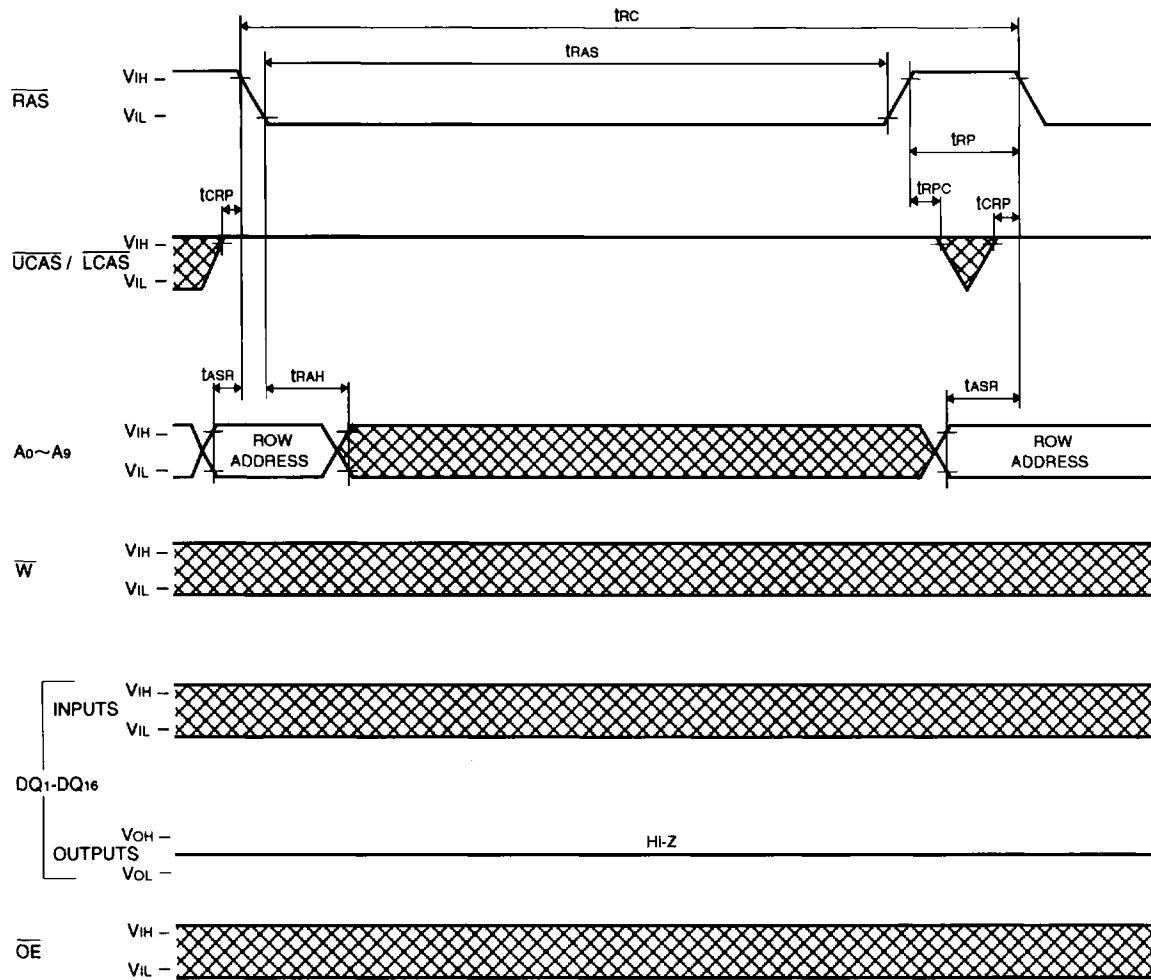


**PRELIMINARY**

Note: This is not a final specification.  
Some parameters listed are subject to change.

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**RAS-only Refresh Cycle**

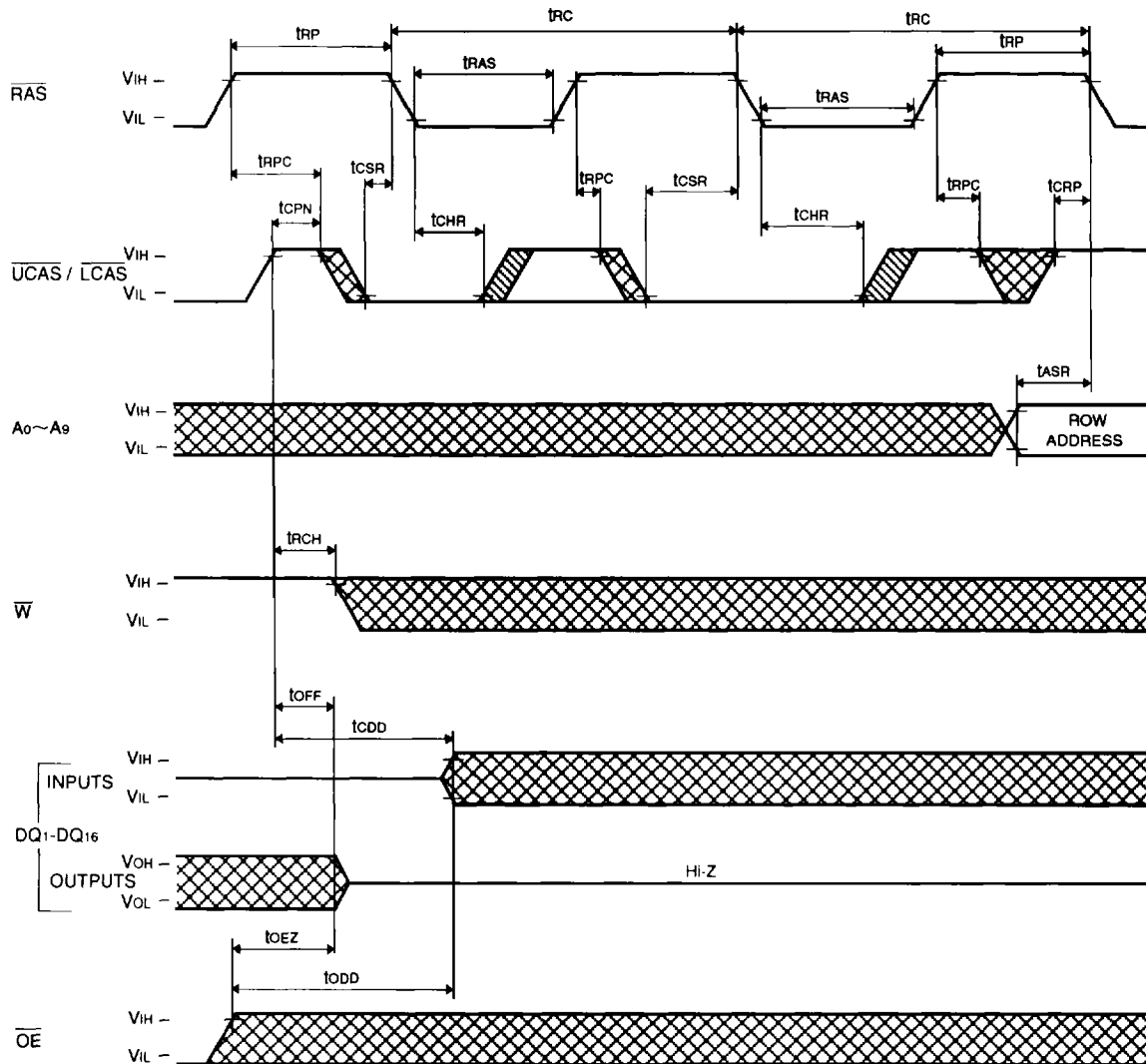




PRELIMINARY

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

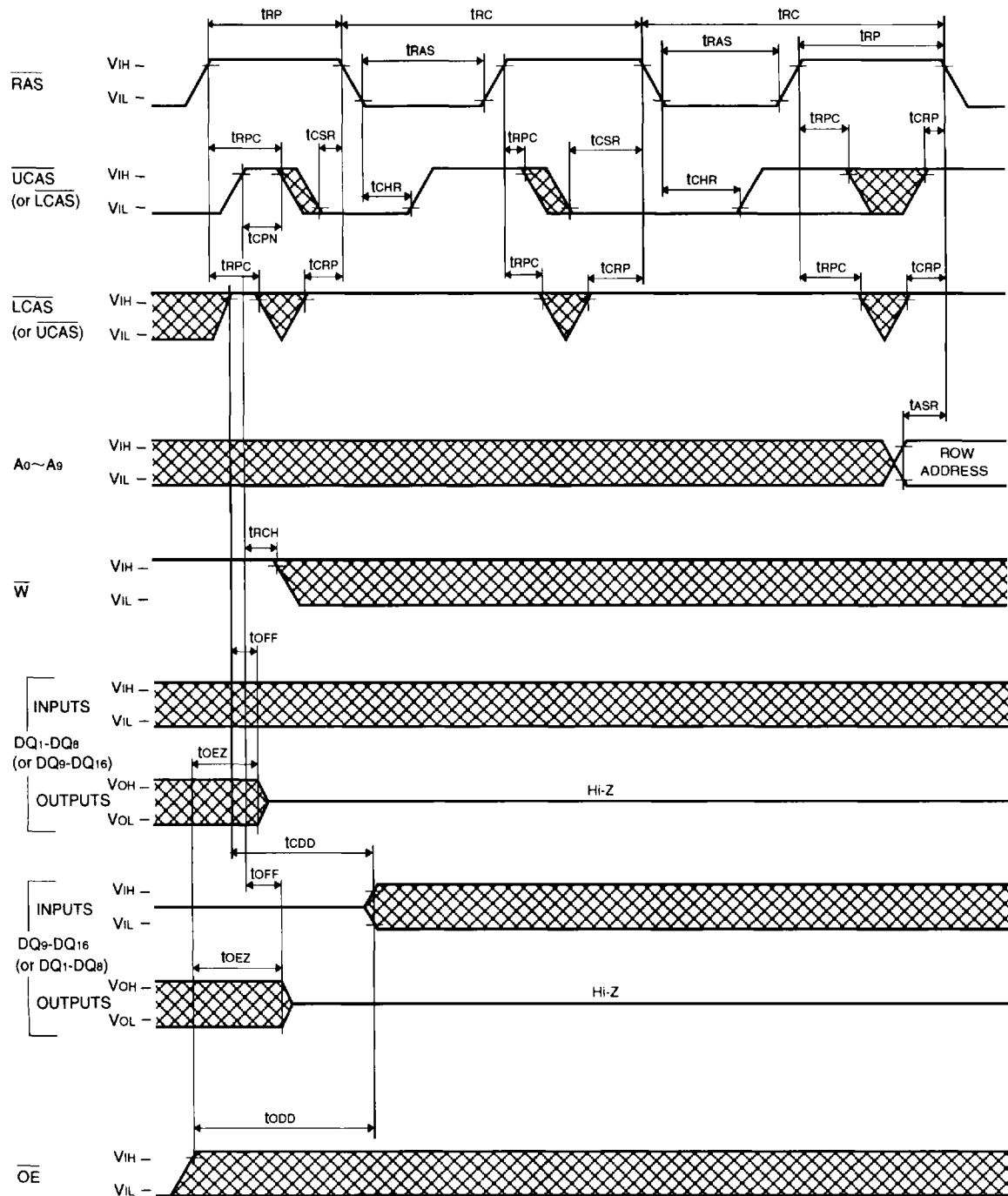
CAS before RAS Refresh Cycle, Extended Refresh Cycle\*



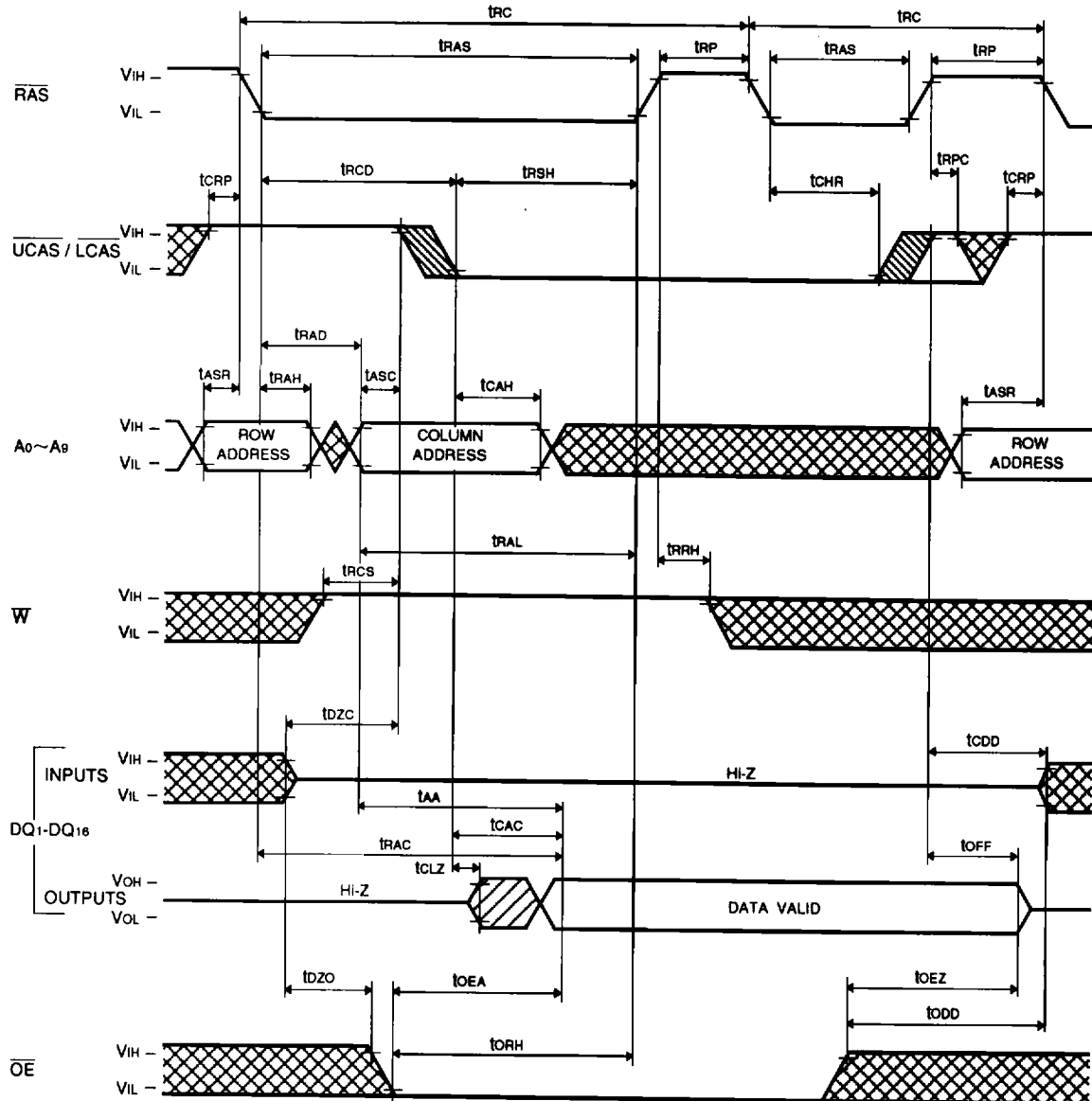
PRELIMINARY

**FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

Upper / (Lower) CAS before RAS Refresh Cycle, Extended Refresh Cycle \*



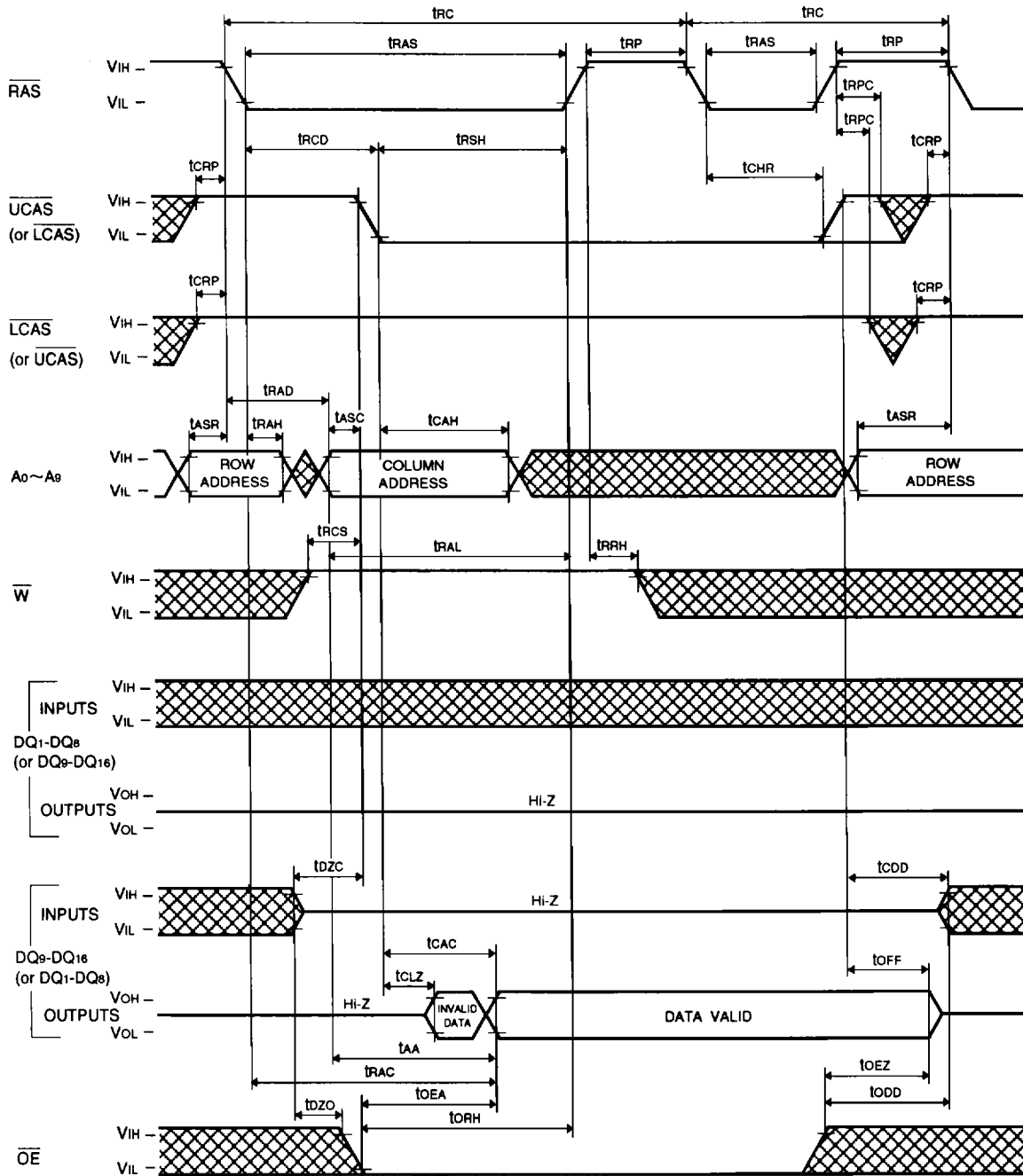
**Hidden Refresh Cycle (Read) (Note 29)**



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)



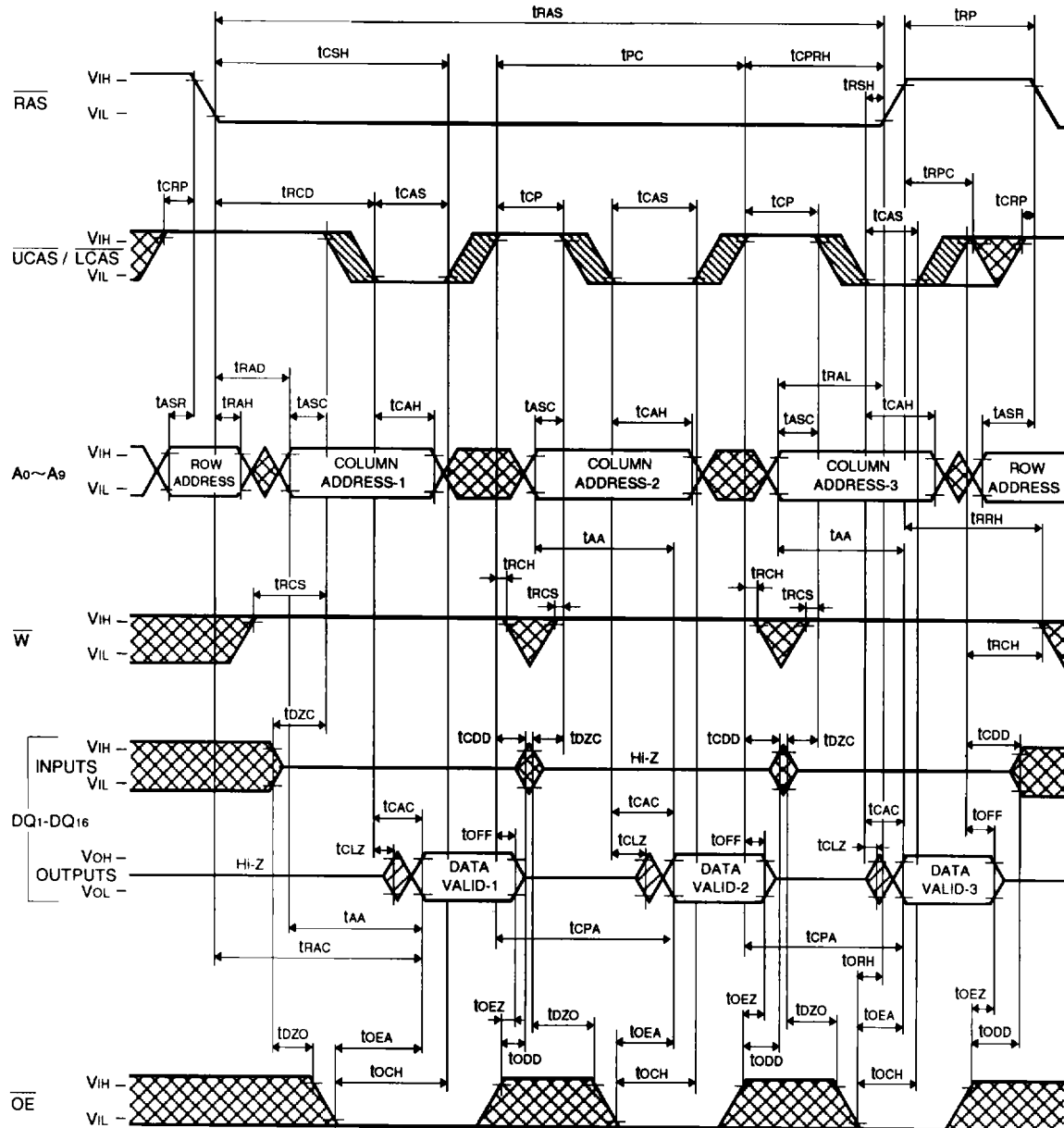
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.  
Timing requirements and output state are the same as that of each cycle shown above.

PRELIMINARY

MITSUBISHI LSI's  
**M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S**

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Fast Page Mode Read Cycle**

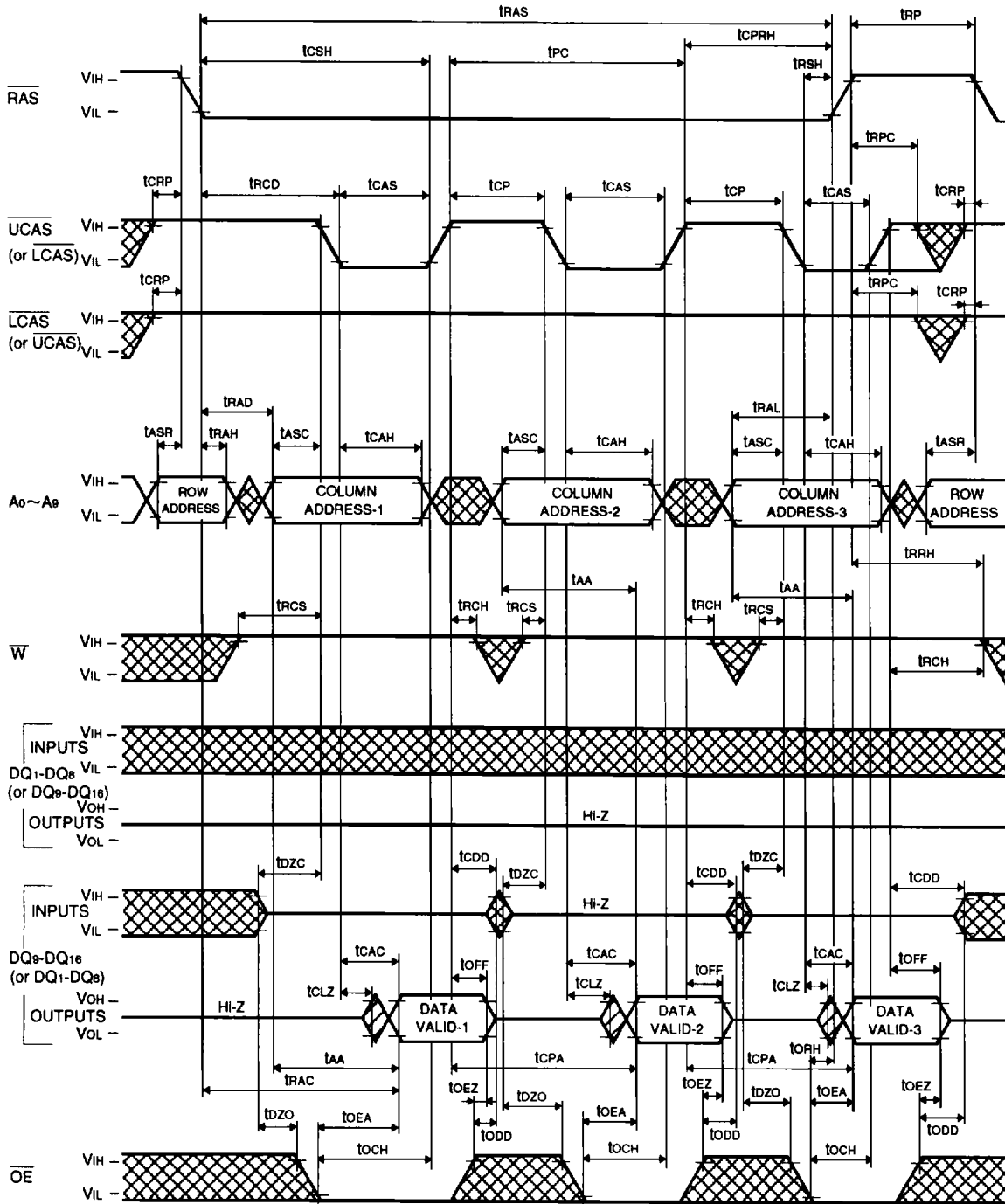


PRELIMINARY

Note: This is not a final symbol. Some parametric limits are subject to change.

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Fast Page Mode Read Cycle

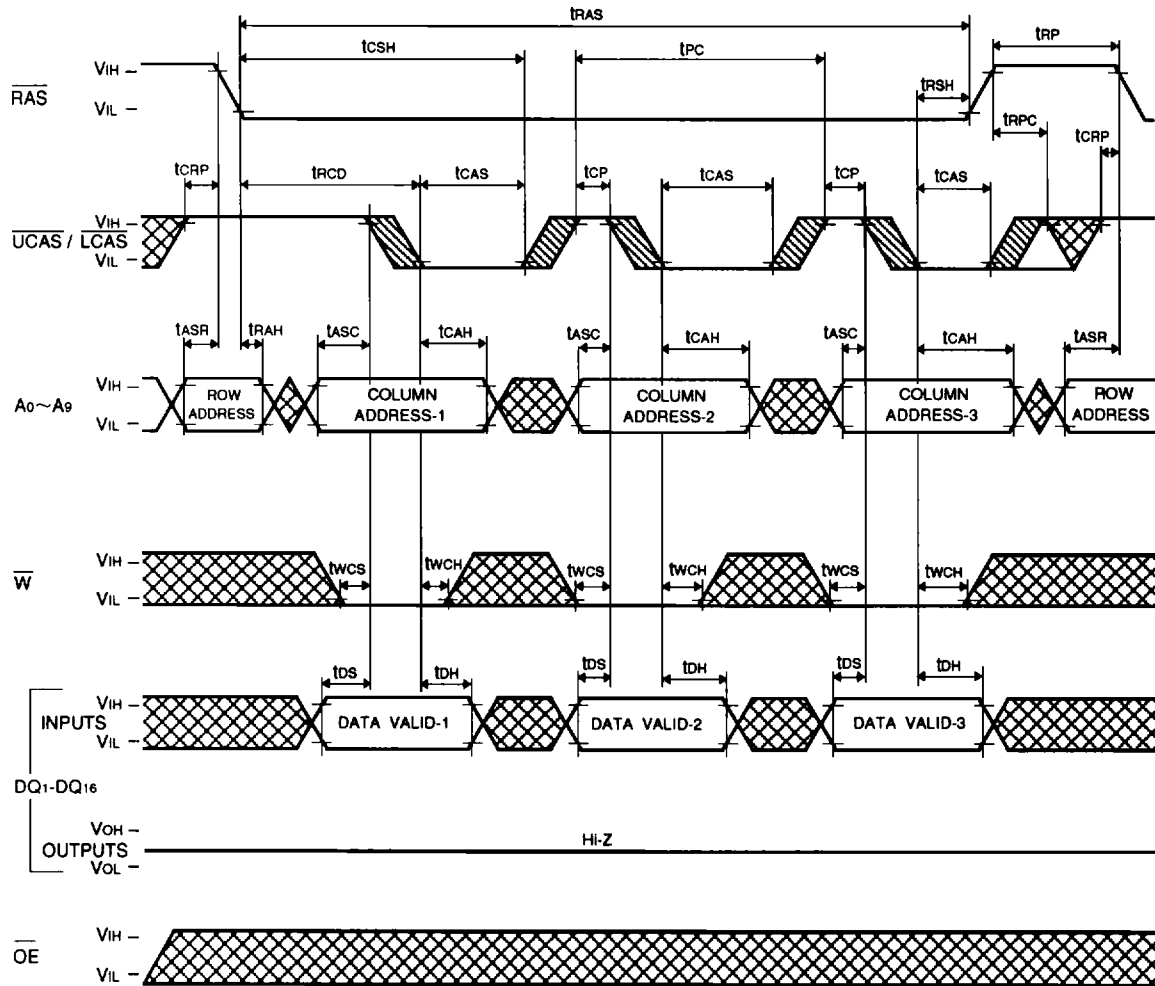


PRELIMINARY

MITSUBISHI LSI<sup>®</sup>  
M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S

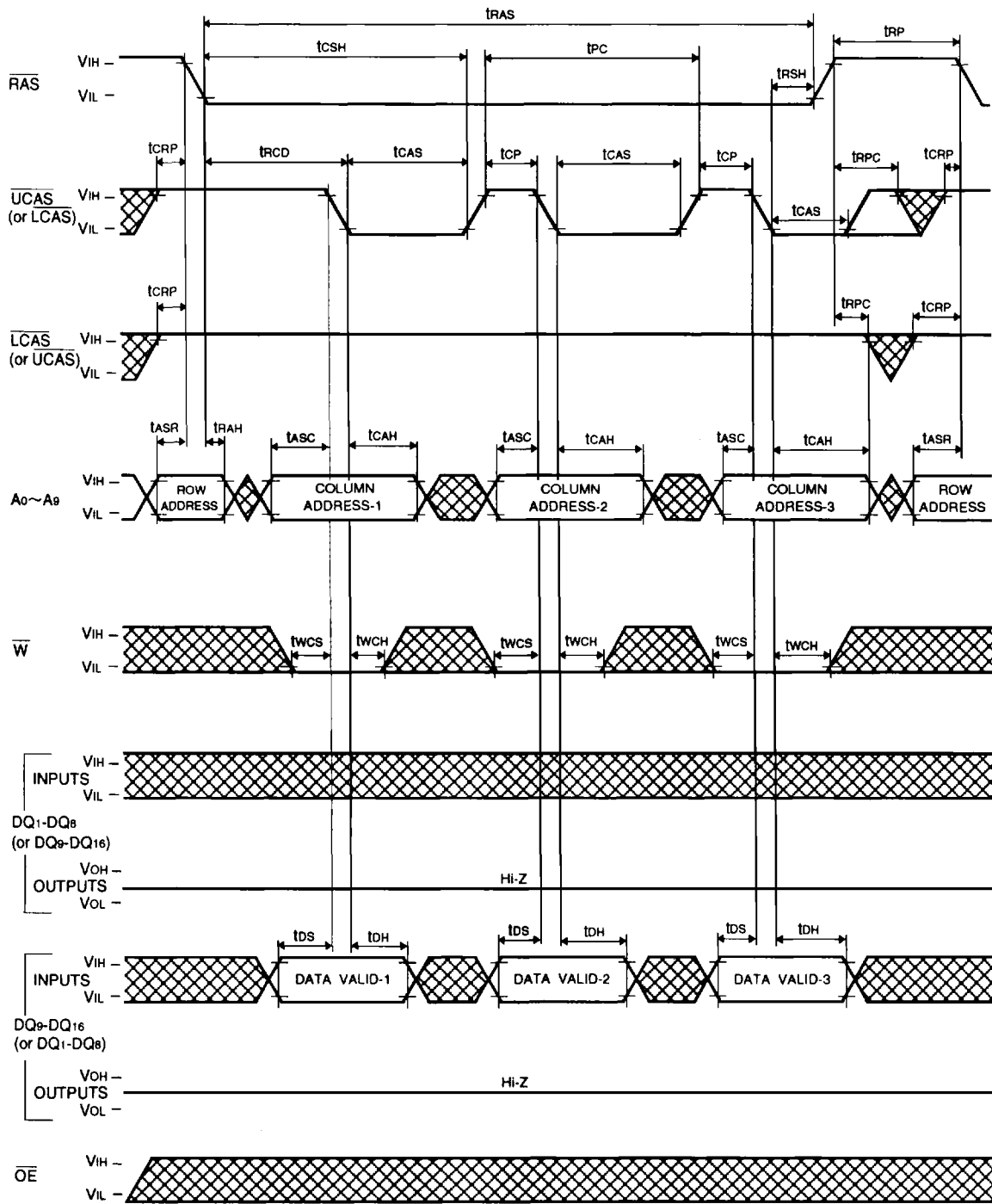
FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)



FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)



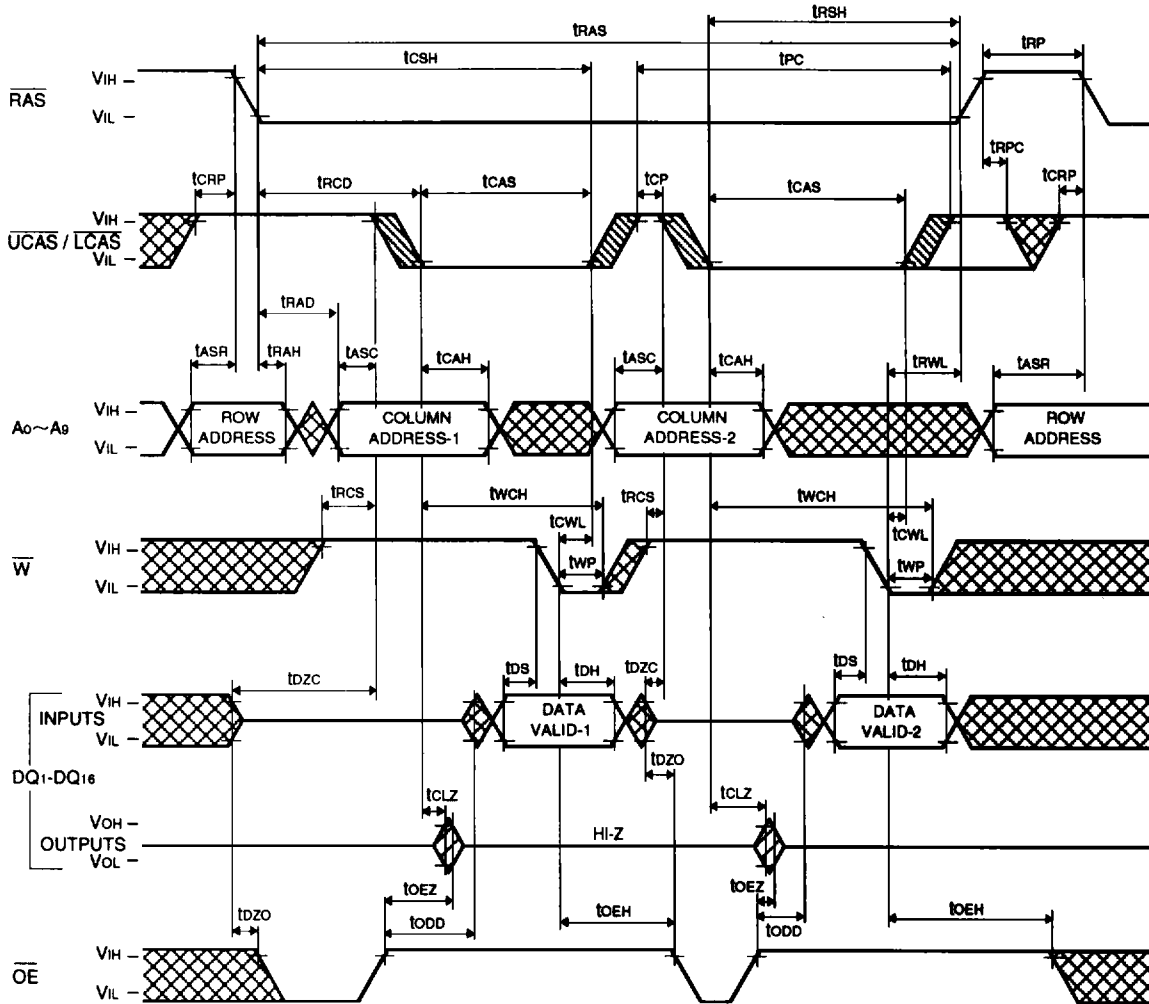


**PRELIMINARY**

Notice: This circuit diagram is preliminary.  
Some parameters may be subject to change.

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Fast Page Mode Write Cycle (Delayed Write)**

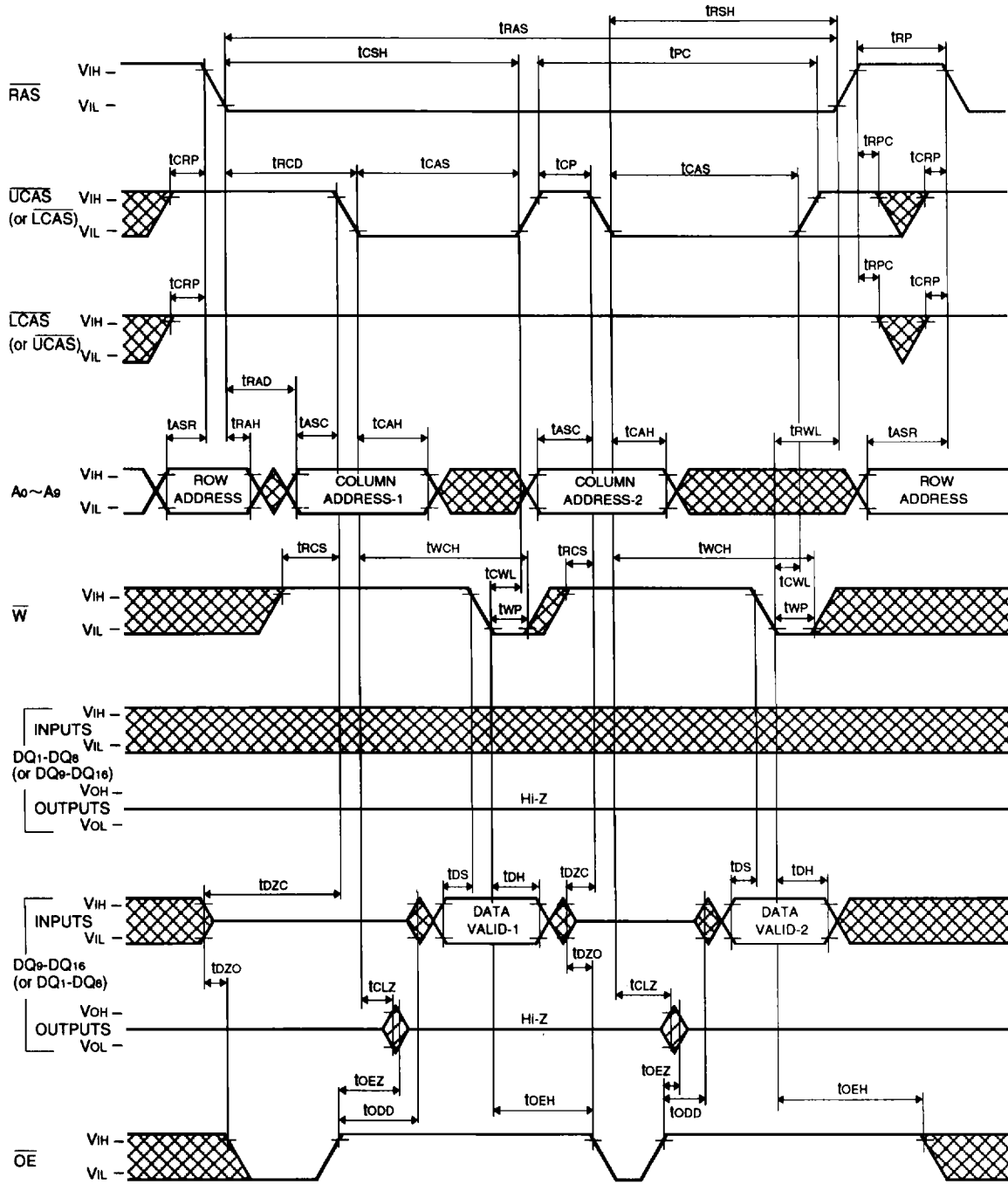


**PRELIMINARY**

Notice: This is not a final specification.  
Some parameter limits are subject to change.

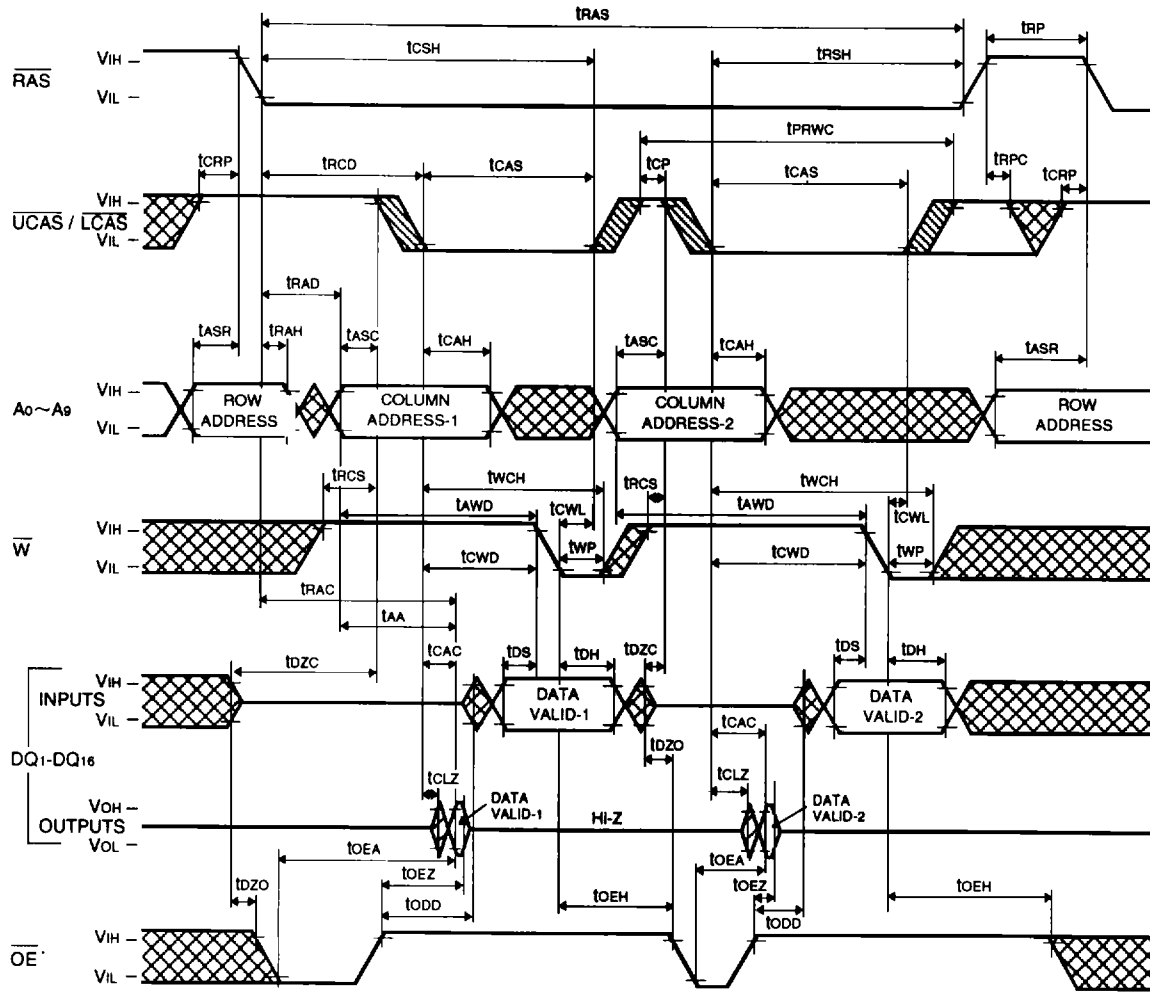
**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)**



**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Fast Page Mode Read-Write, Read-Modify-Write Cycle**

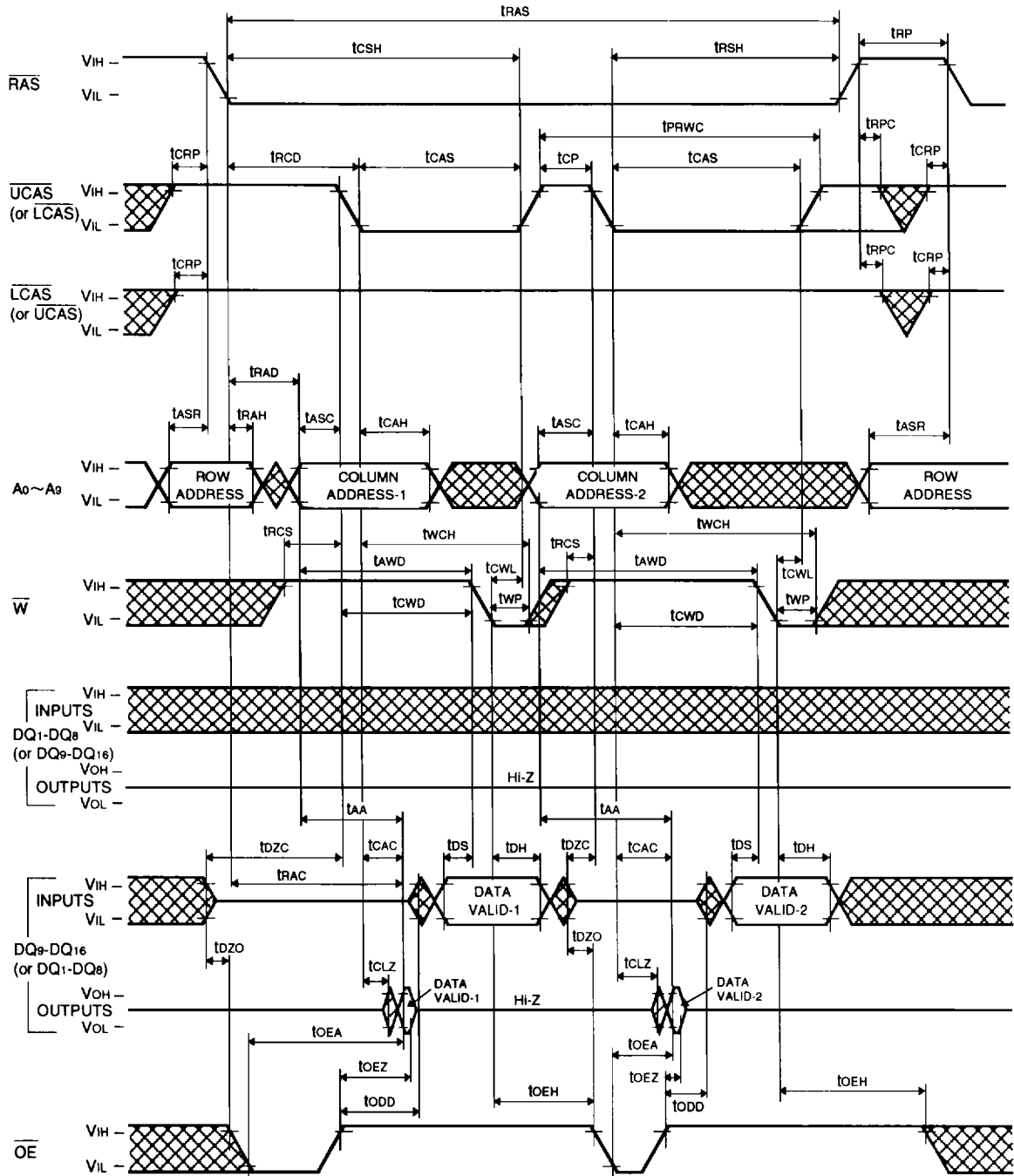


PRELIMINARY

M5M418160CJ, TP-5, -6, -7, -5S, -6S, -7S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle

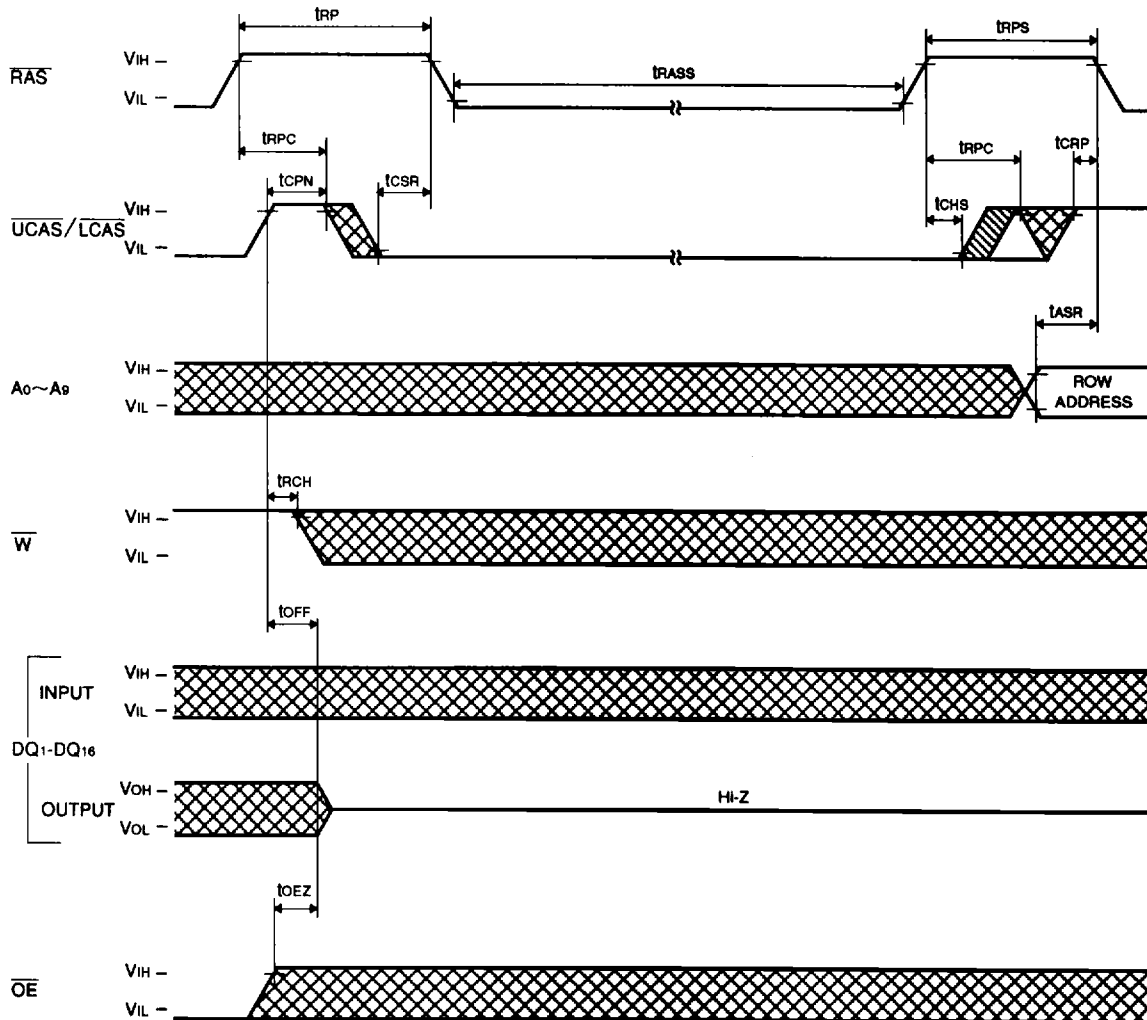


**PRELIMINARY**

Notice: This is not a final specification.  
Some parametric limits are subject to change.

**FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Self Refresh Cycle\***



**PRELIMINARY**  
 Caution: This is not a final product. Specifications are subject to change without notice. Please refer to the latest version of the data sheet.

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

**Upper / (Lower) Self Refresh Cycle\***

