National Semiconductor

March 1993

74ACQ646 • 54ACTQ/74ACTQ646 Quiet Series Octal Transceiver/Register with TRI-STATE® Outputs

General Description

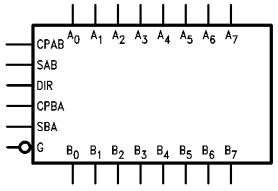
The 'ACQ/'ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1–4*.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT646
- 4 kV minimum ESD immunity
- Standard Military Drawing (SMD)
  — 'ACTQ646: 5962-92196

Logic Symbols



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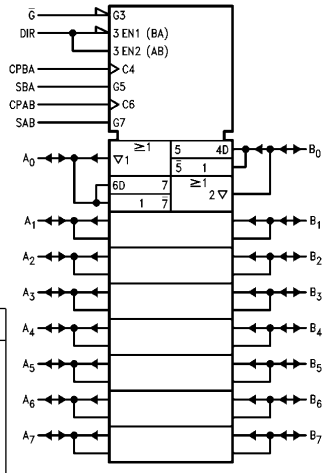
IEEE/IEC



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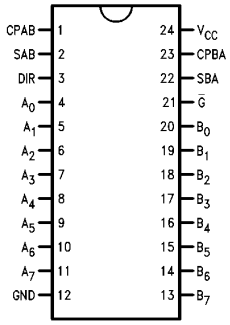
Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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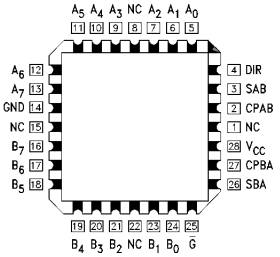
Pin Assignment for LCC



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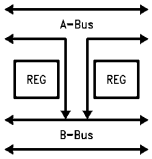
Real Time Transfer A-Bus to B-Bus



TL/F/10635–5

FIGURE 1

Real Time Transfer B-Bus to A-Bus

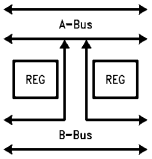


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FIGURE 2

Storage from Bus to Register

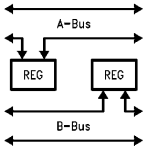

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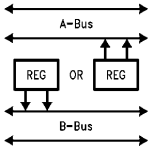
FIGURE 3

Transfer from Register to Bus



TL/F/10635–8

FIGURE 4

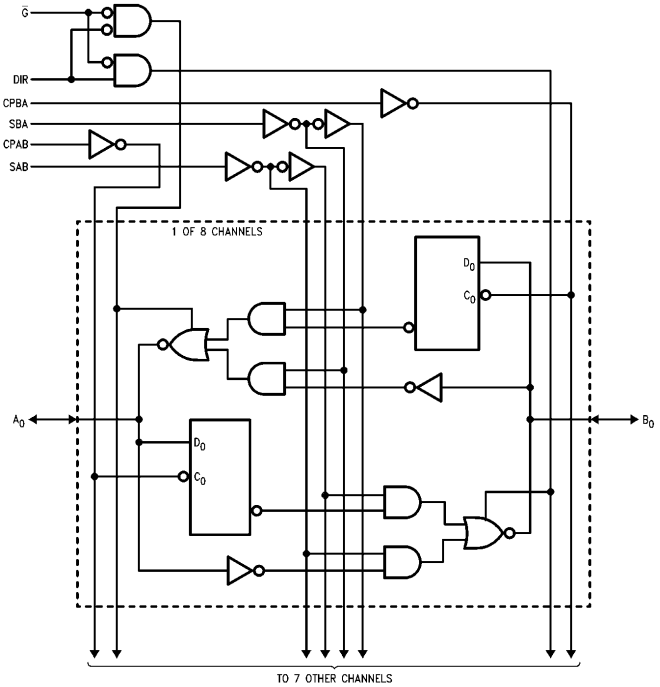
Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Logic Diagram



TL/F/10635–9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) (Note 2)	
74ACQ/ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt	
ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ		74ACQ	Units	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.85	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*Maximum of 8 outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ		74ACQ	Units	Conditions
			$T_A = +25°C$		$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximimum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5		±0.6	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 5V ('ACQ). Input-under-test switching 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} -24 mA
		5.5		4.86	4.70	4.76		I_{OH} -24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5		± 0.6	± 11.0	± 6.0	μA	$V_I = V_{IL}$, V_{IH}; $V_O = V_{CC}$, GND
I_{CCT}	Maxium I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			-50	-75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	-0.6	-1.2			V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.7	2.0			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	3.5 2.5	9.0 6.5	12.0 9.0	3.5 2.5	13.0 9.5	ns
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	3.5 2.5	9.0 6.5	12.0 9.0	3.5 2.5	13.0 9.5	ns
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	3.5 2.5	10.0 7.0	13.0 9.5	3.5 2.5	14.0 10.5	ns
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.5 2.5	10.0 7.0	13.0 9.5	3.5 2.5	14.0 10.5	ns
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	3.5 2.5	9.5 6.5	12.5 9.0	3.5 2.5	13.5 10.0	ns
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	3.5 2.5	9.5 6.5	12.5 9.0	3.5 2.5	13.5 10.0	ns
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.5 2.5	10.5 8.0	14.5 10.5	3.5 2.5	15.5 11.5	ns
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.5 2.5	10.5 8.0	14.5 10.5	3.5 2.5	15.5 11.5	ns
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	8.0 5.0	11.0 7.5	2.5 1.5	12.0 8.0	ns
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	8.0 5.0	11.0 7.5	2.5 1.5	12.0 8.0	ns
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	4.5 3.0	11.0 8.5	15.5 11.0	4.5 3.0	17.0 11.5	ns
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	4.5 3.0	11.0 8.5	15.5 11.0	4.5 3.0	17.0 11.5	ns
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.0	8.0 5.0	11.0 7.5	1.5 1.0	12.0 8.0	ns
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.0	8.0 5.0	11.0 7.5	1.5 1.0	12.0 8.0	ns
t_{OS}	Output to Output Skew**	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V.
Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW Bus to Clock	3.3 5.0		3.0 3.0	3.0 3.0	ns
t_H	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0		1.5 1.5	1.5 1.5	ns
t_W	Clock Pulse Width HIGH or LOW	3.3 5.0		4.0 4.0	4.0 4.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V.
*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Clock to Bus	5.0	2.5	8.5	10.5	2.0	12.0	2.5	11.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Bus to Bus	5.0	2.0	8.0	10.0	2.0	11.0	2.0	10.5	ns
t_{PLH}, t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	5.0	2.5	8.5	10.5	2.0	12.5	2.5	11.0	ns
t_{PZH}, t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	2.5	10.0	12.0	1.0	15.0	2.5	12.5	ns
t_{PHZ}, t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	1.0	7.0	8.5	1.0	12.0	1.0	9.0	ns
t_{PZH}, t_{PZL}	Enable Time DIR to A_n or B_n	5.0	2.5	10.0	12.0	1.0	15.0	2.5	12.5	ns
t_{PHZ}, t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	1.0	7.0	8.5	1.0	12.0	1.0	9.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** Select to Bus or Clock to Bus	5.0		0.5	1.0				1.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** Bus to Bus	5.0		1.0	1.5				1.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW Bus to Clock	5.0		3.0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW Bus to Clock	5.0		1.5	1.5	1.5	ns
t_W	Clock Pulse Width HIGH or LOW	5.0		4.0	4.0	4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	90.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

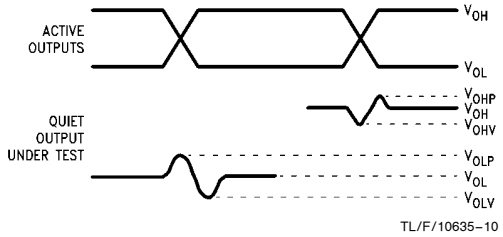
1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

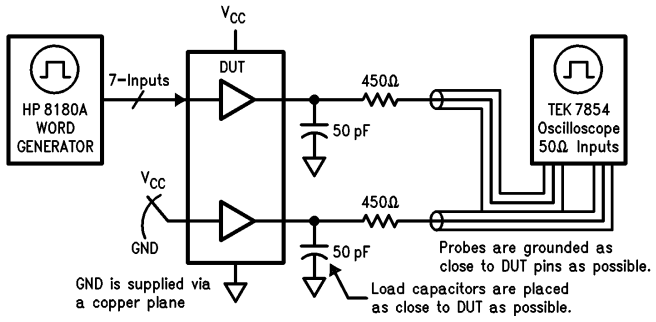


TL/F/10635–10

FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

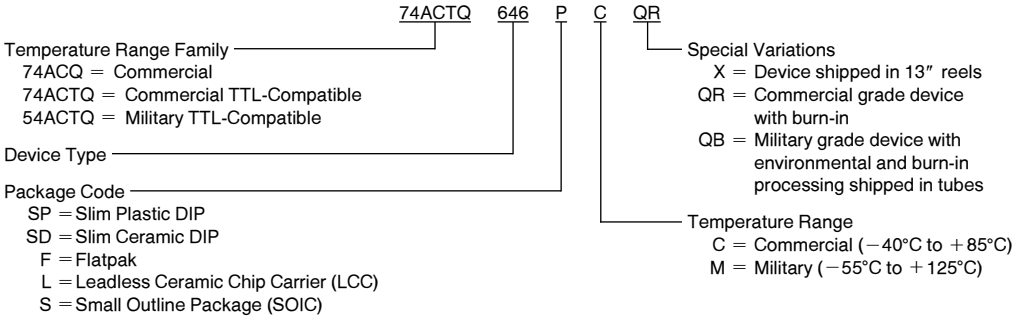


TL/F/10635–11

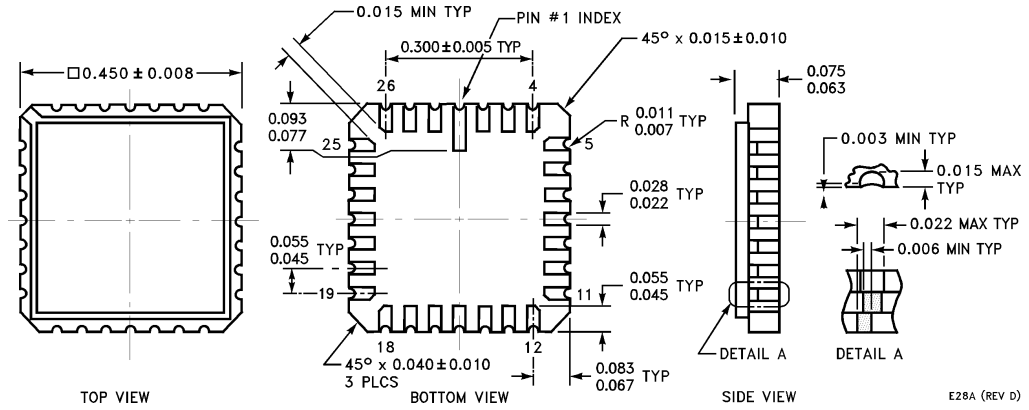
FIGURE 2. Simultaneous Switching Test Circuit

Ordering Information

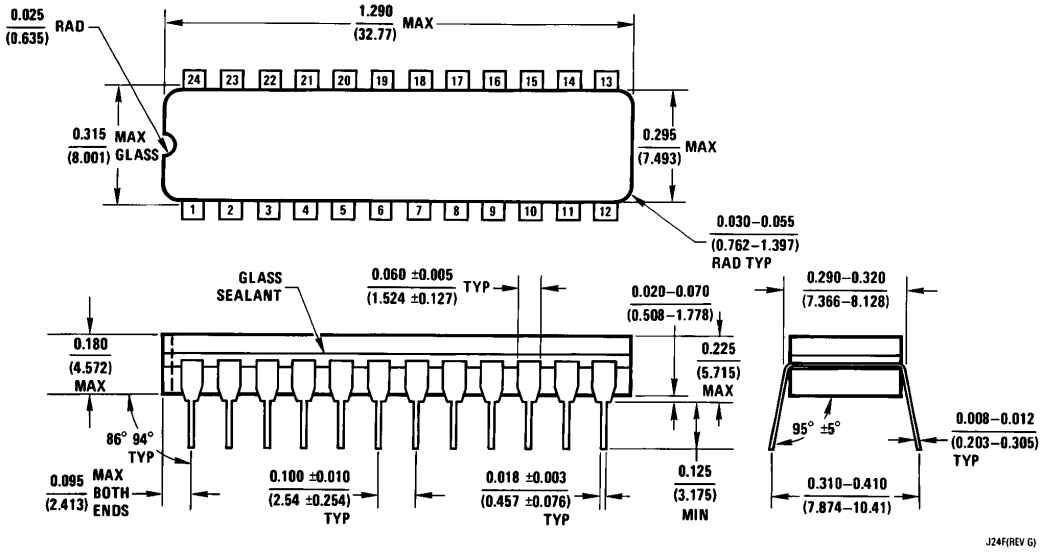
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

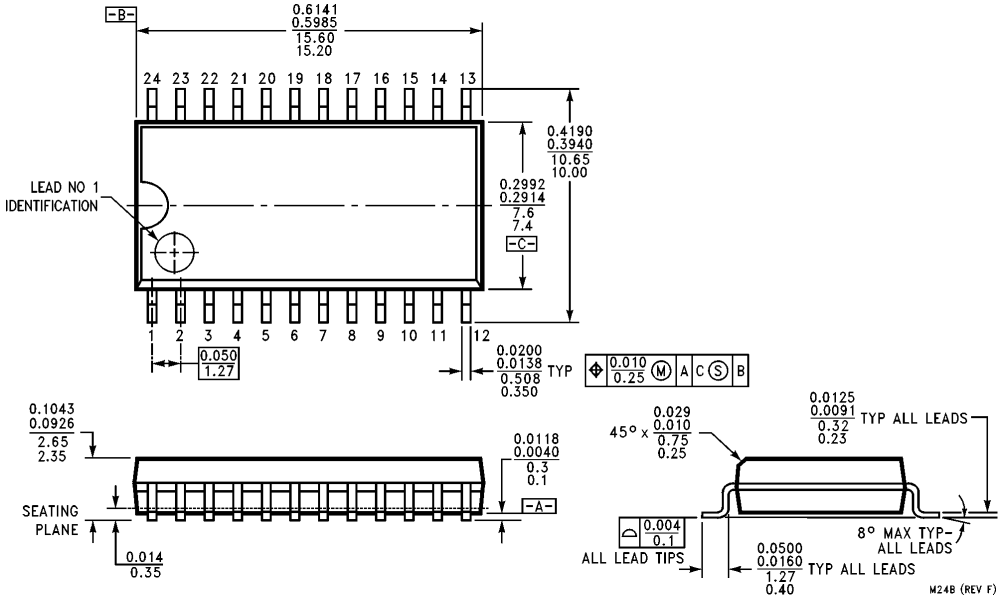


28-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

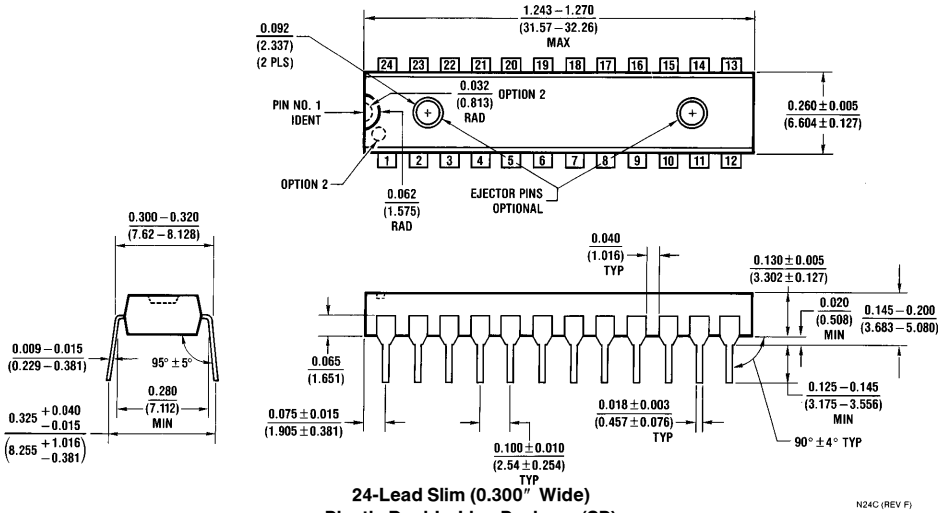


24-Lead Slim (0.300″ Wide)
Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)



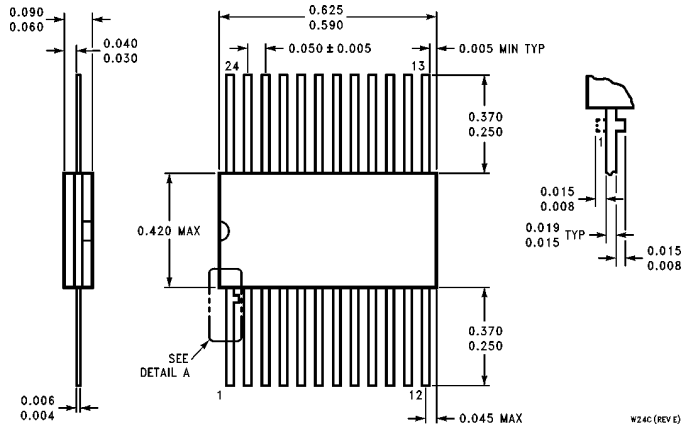
24-Lead Small Outline Integrated Circuit (S)
NS Package Number M24B



24-Lead Slim (0.300″ Wide)
Plastic Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)

Lit. # 115100



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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