REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device 02. Editorial changes throughout. Change drawing CAGE tp 67268.	90-03-07	W. Heckman
B	Changes IAW NOR 5962-R023-99. -ljs	99-01-27	Raymond Monnin
C	Update to reflect latest changes in format and requirements. Editorial changes throughout. -les	01-11-28	Raymond Monnin

The original first sheet of this drawing has been replaced.

CURRENT CAGE CODE 67628

REV																				
SHEET																				
REV	C	C	C																	
SHEET	15	16	17																	

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
87-02-09

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, BIPOLAR, OCTAL, 3-STATE, BIDIRECTIONAL, BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86723**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

5962-E007-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86838	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2947	Octal, 3-state, bi-directional, bus transceivers noninverting
02	2946	Octal, 3-state, bi-directional, bus transceivers inverting

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or GDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square chip carrier

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	775 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Ambient operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figures 4 through 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage, A_0 - A_7	V_{OH1}	V_{CC} = 4.5 V, $T/\overline{R}$ = 0.8 V, CD = 0.7 V	I_{OH} = -0.4 mA	1, 2, 3	All	3.35		V
			I_{OH} = -3.0 mA	1, 2, 3	All	2.7		V
High level output voltage, B_0 - B_7	V_{OH2}	V_{CC} = 4.5 V, $T/\overline{R}$ = 2.0 V, CD = 0.7 V	I_{OH} = -0.4 mA	1, 2, 3	All	3.35		V
			I_{OH} = -5.0 mA	1, 2, 3	All	2.7		V
			I_{OH} = -10 mA	1, 2, 3	All	2.4		V
Low level output voltage, A_0 - A_7	V_{OL1}	V_{CC} = 4.5 V, $T/\overline{R}$ = 0.8 V, CD = 0.7 V, I_{OL} = 12 mA		1, 2, 3	All		0.4	V
Low level output voltage, B_0 - B_7	$V_{OL 2}$	V_{CC} = 4.5 V, $T/\overline{R}$ = 2.0 V, CD = 0.7 V	I_{OL} = 20 mA	1, 2, 3	All		0.4	V
			I_{OL} = 48 mA	1, 2, 3	All		0.55	V
Input clamp voltage, A_0 - A_7 and B_0 - B_7	$V_{I C1}$	V_{CC} = 4.5 V, CD = 2.0 V, I_{IN}= -12 mA		1, 2, 3	All		-1.5	V
Input clamp voltage, CD, $T/\overline{R}$	$V_{I C2}$	V_{CC} = 4.5 V, I_{IN}= -12 mA		1, 2, 3	All		-1.5	V
High level input current, A_0 - A_7	I_{IH1}	V_{CC} = 5.5 V, $T/\overline{R}$ = 2.0 V, CD = 0.7 V, V_{IN} = 2.7 V		1, 2, 3	All		80	µA
High level input current, B_0 - B_7	I_{IH2}	V_{CC} = 5.5 V, $T/\overline{R}$ = CD = 0.7 V, V_{IN} = 2.7 V		1, 2, 3	All		80	µA
High level input current, CD, $T/\overline{R}$	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3	All		20	µA
High level input current, A_0 - A_7, B_0 - B_7	I_{IH4}	V_{CC} = 5.5 V, CD = 2.0 V, V_{IN} = 5.5 V		1, 2, 3	All		1	mA
High level input current, $T/\overline{R}$, CD	I_{IH5}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		1	mA
Low level input current, A_0 - A_7	I_{IL1}	V_{CC} = 5.5 V, $T/\overline{R}$ = 2.0 V, CD = 0.7 V, V_{IN} = 0.4 V		1, 2, 3	All		-200	µA
Low level input current, B_0 - B_7	I_{IL2}	V_{CC} = 5.5 V, $T/\overline{R}$ = 0.7 V, CD = 0.7 V, V_{IN} = 0.4 V		1, 2, 3	All		-200	µA
Low level input current, CD, $T/\overline{R}$	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1, 2, 3	All		-250	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Short circuit output current, A_0 - A_7	I_{OS1}	V_{CC} = 5.5 V, $T/\overline{R}$ = 0.8 V, CD = 0.7 V, V_{OUT} = 0.0 V 1/		1, 2, 3	All	-10	-75	mA
Short circuit output current, B_0 - B_7	I_{OS2}	V_{CC} = 5.5 V, $T/\overline{R}$ = 2.0 V, CD = 0.7 V, V_{OUT} = 0.0 V 1/		1, 2, 3	All	-25	-150	mA
Functional tests		See 4.3.1c		7, 8	All			
Off state output current high	I_{OZH}	V_{CC} = 5.5 V, CD = 2.0 V, V_{OUT} = 4.0 V	A_0 - A_7	1, 2, 3	All		80	µA
			B_0 - B_7	1, 2, 3	All		200	µA
Off state output current low, A_0 - A_7, B_0 - B_7	I_{OZL}	V_{CC} = 5.5 V, CD = 2.0 V, V_{OUT} = 0.4 V		1, 2, 3	All		-200	µA
Supply current	I_{CC}	V_{CC} = 5.5 V, CD = 2.0 V, $T/\overline{R}$ = 0.4 V	V_{IN} = 0.4 V	1, 2, 3	01		100	mA
			V_{IN} = 2.0 V	1, 2, 3	02		100	mA
		V_{CC} = 5.5 V, CD = 0.4 V, $T/\overline{R}$ = 2.0 V	V_{IN} = 0.4 V	1, 2, 3	01		140	mA
			V_{IN} = 2.0 V	1, 2, 3	02		150	mA
Propagation delay time, input B port to output A port	t_{PHL1}	CD = $T/\overline{R}$ = 0.4 V, R_1 = 1 kΩ, R_2 = 5 kΩ, C_1 = 30 pF (See figure 4)		9 2/	01		18	ns
					02		12	ns
				9, 10, 11 3/	01		24	ns
					02		19	ns
	t_{PLH1}			9 2/	01		18	ns
					02		16	ns
				9, 10, 11 3/	01		24	ns
					02		23	ns
Disable time, CD to A port	t_{PLZ1}	$T/\overline{R}$ = 0.4 V, R_5 = 1 kΩ, C_4 = 15 pF (See figure 6)	B_0 - B_7 = 0.4 V, S_3 = 1	9 2/	All		15	ns
				9, 10, 11 3/	All		21	ns
	t_{PHZ1}		B_0 - B_7 = 2.4 V, S_3 = 0	9 2/	All		15	ns
				9, 10, 11 3/	All		21	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Enable time, CD to A port	t_{PZL1}	C_4 = 30 pF, $T/\overline{R}$ = 0.4 V, (See figure 6) 4/	B_0 - B_7 = 0.4 V S_3 = 1 R_5 = 1 kΩ	9 2/	All		25	ns
				9, 10, 11 3/	All		33	ns
	t_{PZH1}		B_0 - B_7 = 2.4 V S_3 = 0 R_5 = 5 kΩ	9 2/	All		25	ns
				9, 10, 11 3/	All		33	ns
Propagation delay time, input A port to output B port	t_{PHL2}	CD = 0.4 V, $T/\overline{R}$ = 2.4 V, (See figure 4) 4/	R_1 = 100Ω R_2 = 1 kΩ C_1 = 300 pF	9 2/	01		23	ns
					02		18	ns
				9, 10, 11 3/	01		34	ns
					02		29	ns
			R_1 = 667Ω R_2 = 5 kΩ C_1 = 45 pF	9 2/	01		18	ns
					02		12	ns
				9, 10, 11 3/	01		25	ns
					02		19	ns
	t_{PLH2}		R_1 = 100Ω R_2 = 1 kΩ C_1 = 300 pF	9 2/	01		23	ns
					02		20	ns
				9, 10, 11 3/	01		34	ns
					02		30	ns
			R_1 = 667Ω R_2 = 5 kΩ C_1 = 45 pF	9 2/	01		18	ns
					02		14	ns
				9, 10, 11 3/	01		25	ns
					02		22	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Disable time, CD to B port	t_{PLZ2}	$T/\overline{R}$ = 2.4 V, R_5 = 1 kΩ C_4 = 15 pF, (See figure 6) 4/	A_0 - A_7 = 0.4 V S_3 = 1	9 2/	All		18	ns
				9, 10, 11 3/	All		26	ns
	t_{PHZ2}		A_0 - A_7 = 2.4 V S_3 = 0	9 2/	All		15	ns
				9, 10, 11 3/	All		21	ns
Enable time, CD to B port	t_{PZL2}	A_0 - A_7 = 0.4 V, $T/\overline{R}$ = 2.4 V, S_3 = 1, (See figure 6) 4/	R_5 = 100Ω C_4 = 300 pF	9 2/	All		35	ns
				9, 10, 11 3/	All		43	ns
			R_5 = 667Ω C_4 = 45 pF	9 2/	All		22	ns
				9, 10, 11 3/	All		30	ns
	t_{PZH2}	A_0 - A_7 = 2.4 V, $T/\overline{R}$ = 2.4 V, S_3 = 0, (See figure 6) 4/	R_5 = 1 kΩ C_4 = 300 pF	9 2/	All		35	ns
				9, 10, 11 3/	All		43	ns
			R_5 = 5 kΩ C_4 = 45 pF	9 2/	All		22	ns
				9, 10, 11 3/	All		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, from transmit mode to receive, $T/\overline{R}$ to A port	t_{TRL}	A port; $S_2 = 1$; $C_2 = 30$ pF; CD = 0.4 V, $R_3 = 1$ kΩ (See figure 5) 4/	9 2/	01		38	ns
				02		33	ns
			9, 10, 11 3/	01		48	ns
				02		43	ns
		B port; $S_1 = 0$; $R_4 = 100\Omega$; $C_3 = 5$ pF (See figure 5) 4/	9 2/	01		38	ns
				02		33	ns
			9, 10, 11 3/	01		48	ns
				02		43	ns
	t_{TRH}	A port; $S_2 = 0$; $C_2 = 30$ pF; CD = 0.4 V, $R_3 = 5$ kΩ (See figure 5) 4/	9 2/	01		38	ns
				02		33	ns
			9, 10, 11 3/	01		48	ns
				02		43	ns
		B port; $S_1 = 1$; $R_4 = 100\Omega$; $C_3 = 5$ pF (See figure 5) 4/	9 2/	01		38	ns
				02		33	ns
			9, 10, 11 3/	01		48	ns
				02		43	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, from transmit mode to receive, $T/\overline{R}$ to B port	t_{RTL}	A port; $S_2 = 0$; $C_2 = 5$ pF; CD = 0.4 V, $R_3 = 300\Omega$ (See figure 5) 4/	9 2/	01		40	ns
				02		35	ns
			9, 10, 11 3/	01		51	ns
				02		47	ns
		B port; $S_1 = 1$; $R_4 = 100\Omega$; $C_3 = 300$ pF (See figure 5) 4/	9 2/	01		40	ns
				02		35	ns
			9, 10, 11 3/	01		51	ns
				02		47	ns
	t_{RTH}	A port; $S_2 = 1$; $C_2 = 5$ pF; CD = 0.4 V, $R_3 = 300\Omega$ (See figure 5) 4/	9 2/	01		40	ns
				02		35	ns
			9, 10, 11 3/	01		51	ns
				02		47	ns
		B port; $S_1 = 0$; $R_4 = 1$ kΩ; $C_3 = 300$ pF (See figure 5) 4/	9 2/	01		40	ns
				02		35	ns
			9, 10, 11 3/	01		51	ns
				02		47	ns

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed one second.
2/ $V_{CC} = 5.0$ V.
3/ $V_{CC} = 4.5$ V to 5.5 V.
4/ All ac loads are correlated from load of 50 pF during test.

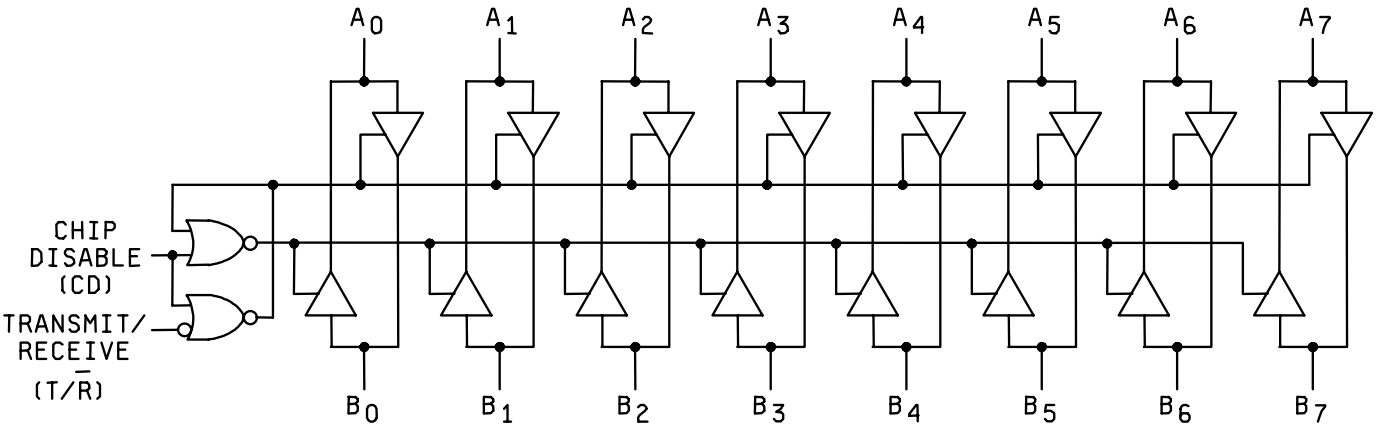
Device types	01	02
Case outlines	R, 2	R, 2
Terminal number	Terminal symbols	
1	A_0	A_0
2	A_1	A_1
3	A_2	A_2
4	A_3	A_3
5	A_4	A_4
6	A_5	A_5
7	A_6	A_6
8	A_7	A_7
9	CD	CD
10	GND	GND
11	$T/\overline{R}$	$T/\overline{R}$
12	B_7	B_7
13	B_6	B_6
14	B_5	B_5
15	B_4	B_4
16	B_3	B_3
17	B_2	B_2
18	B_1	B_1
19	B_0	B_0
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

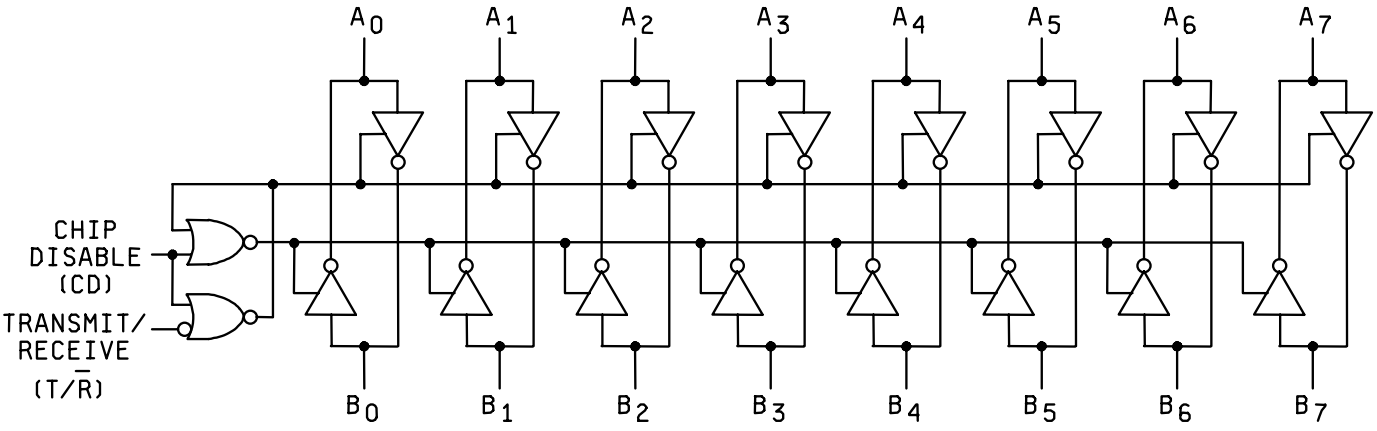
Inputs	Conditions		
Chip disable	L	L	H
Transmit/$\overline{\text{Receive}}$	L	H	X
A Port	Out	In	Z
B Port	In	Out	Z

H = high level
L = low level
Z = high impedance state
X = irrelevant

FIGURE 2. Truth table.

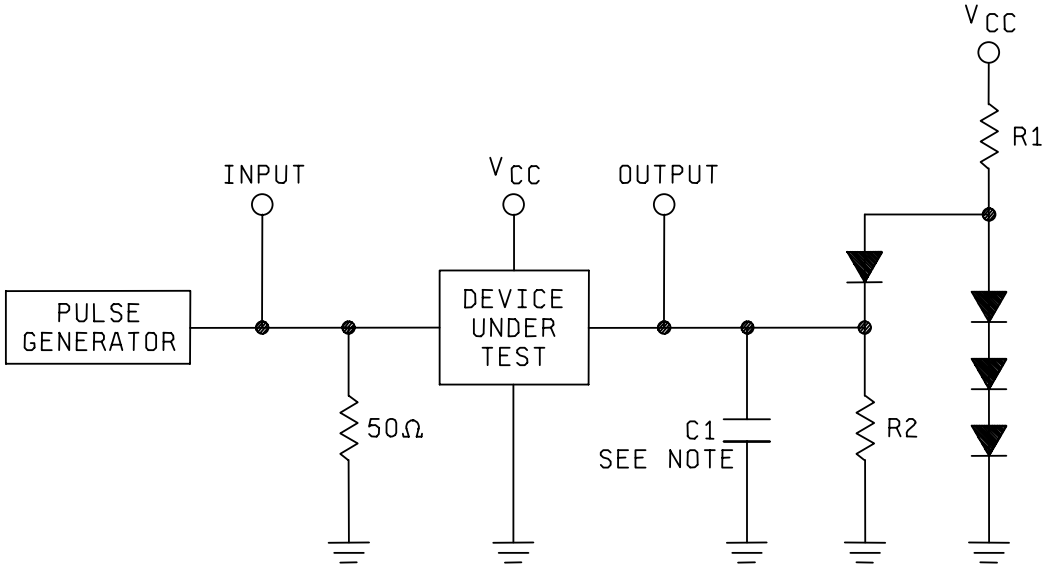


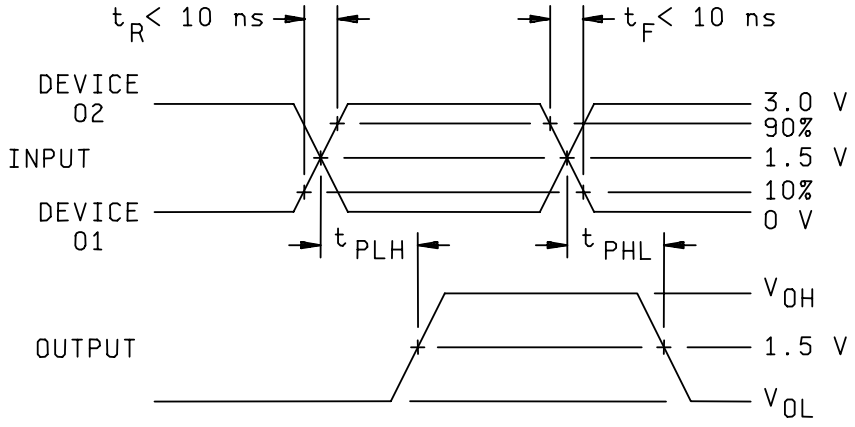
DEVICE 01 (NONINVERTING)



DEVICE 02 (INVERTING)

FIGURE 3. Logic diagram.

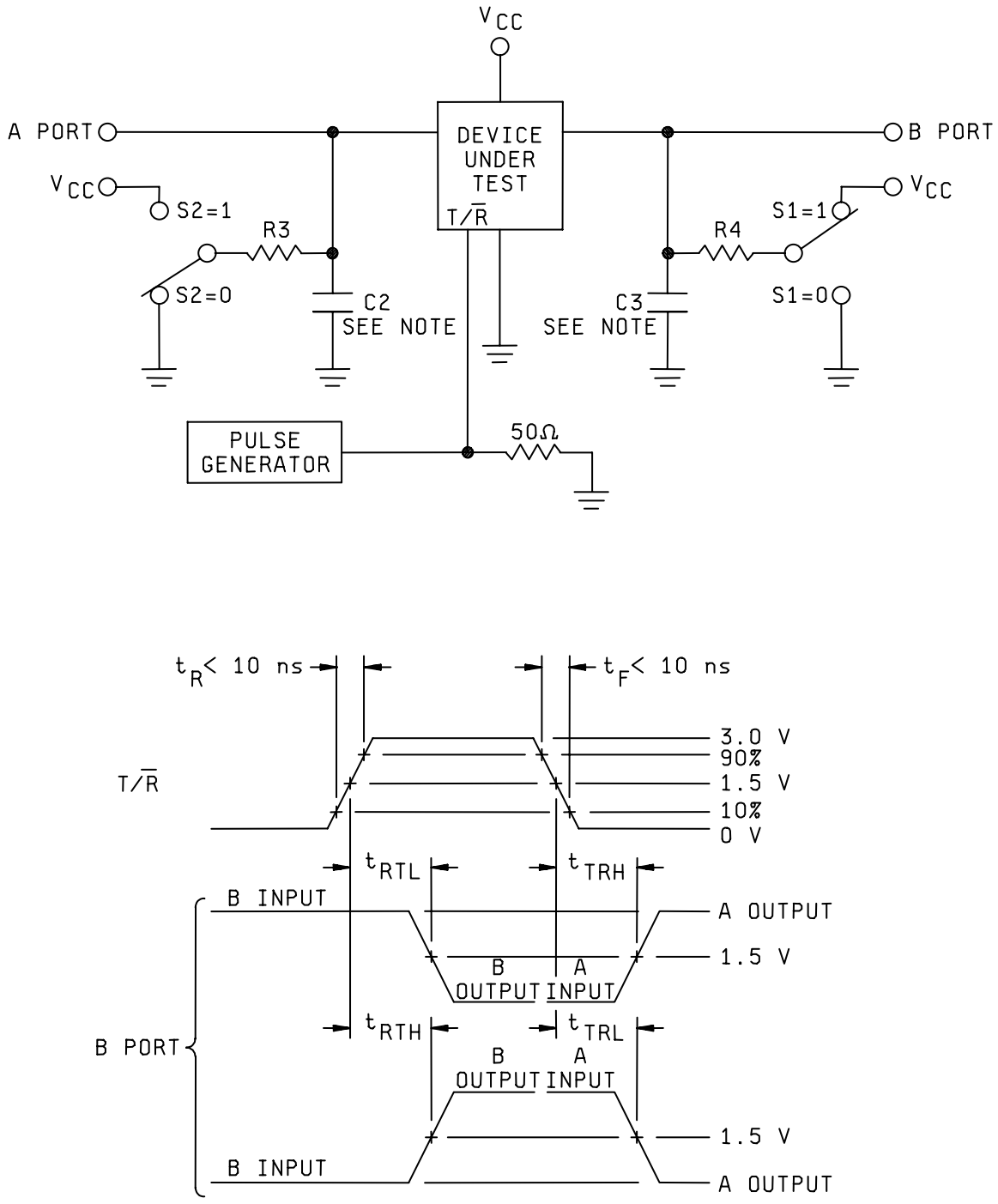




NOTE: C1 includes test fixture capacitance.

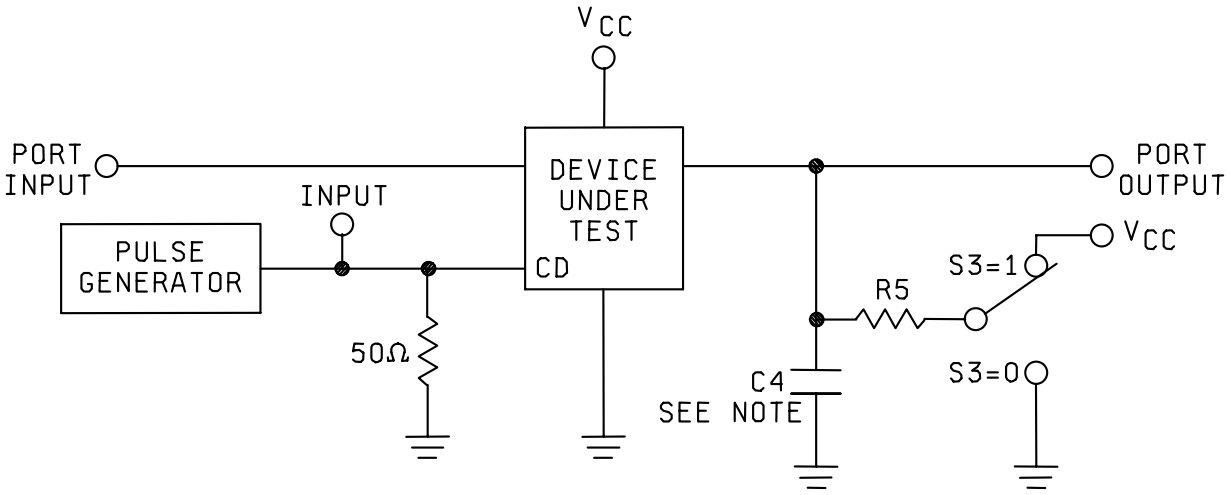
From A/B port to B/A port.

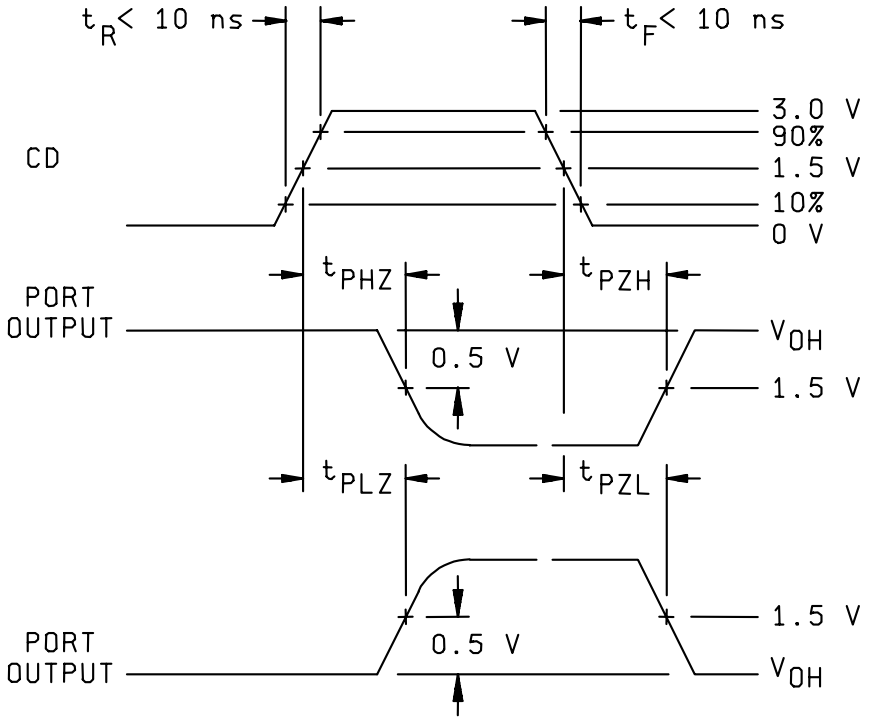
FIGURE 4. Test circuit and switching waveforms.



NOTE: C2 and C3 include test fixture capacitance.

FIGURE 5. Test circuit and switching waveforms - From $T/\overline{R}$ to A or B port.





NOTE: C4 includes test fixture capacitance, port input is in a fixed logical condition.

FIGURE 6. Test circuit and switching waveforms - From CD to A or B port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-11-07

Approved sources of supply for SMD 5962-86723 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8672301RA	3V146 0DKS7 3/	2947/BRA GEM07501BRA AM2947/BRA
5962-8672301RC	0DKS7	GEM07501BRC
5962-86723012A	3V146 0DKS7 3/	2947/B2A GEM07501B2A AM2947/B2A
5962-86723012C	0DKS7	GEM07501B2C
5962-8672302RA	3V146 0DKS7 3/	2946/BRA GEM13302BRA AM2947/BRA
5962-8672302RC	0DKS7	GEM13302BRC
5962-86723022A	3V146 0DKS7 3/	2946/B2A GEM13302B2A AM2947/B2A
5962-86723022C	0DKS7	GEM13302B2C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No current source.

Vendor CAGE number	Vendor name and address
3V146	ROCHESTER ELECTRONICS 10 Malcom Hoyt Drive Newburyport, MA 01950
0DKS7	SARNOFF, DAVID RESEARCH CENTER 201 Washington Road Princeton, NJ 08540-5300