



Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (128K x 8-BIT) REVOLUTIONARY PINOUT

PRELIMINARY
IDT71124

FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise.
- Equal access and cycle times
 - Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in Plastic 32-pin 400 mil SOJ and 32-pin 400 mil TSOP Type II

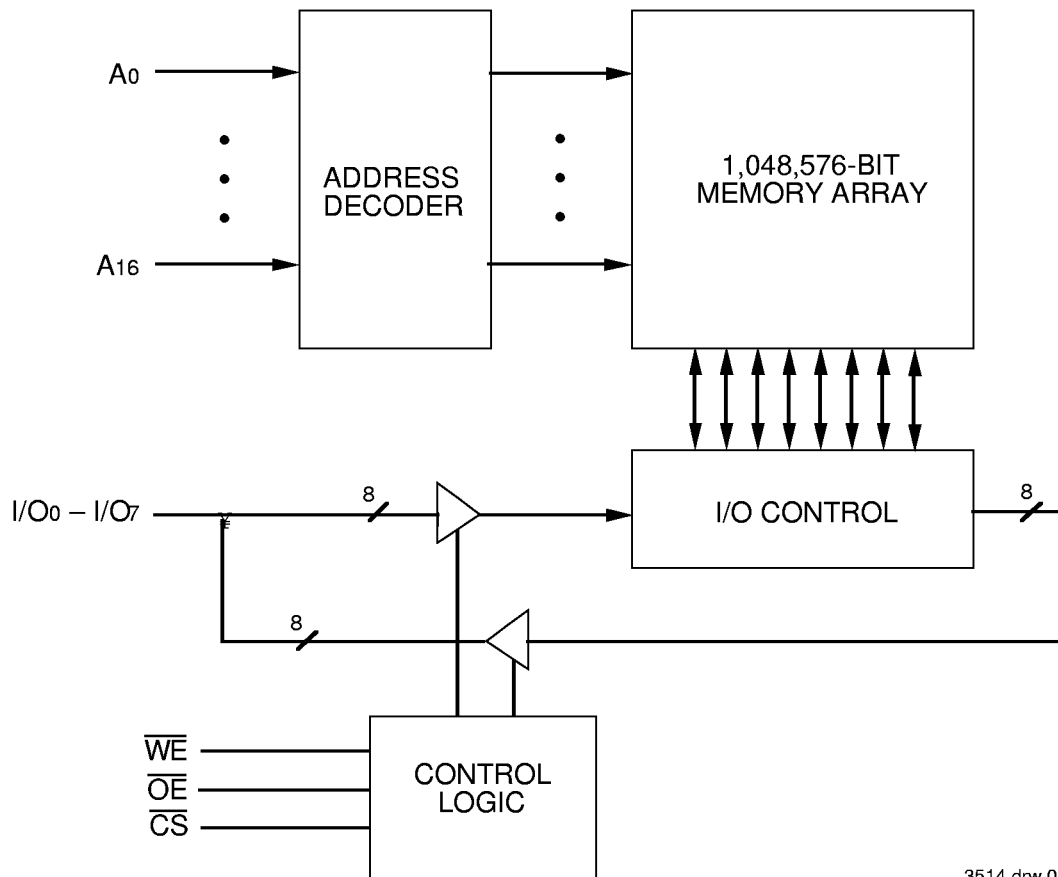
DESCRIPTION:

The IDT71124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

The IDT71124 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71124 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71124 is packaged in Plastic 32-pin 400 mil SOJ 32-pin 400 mil TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



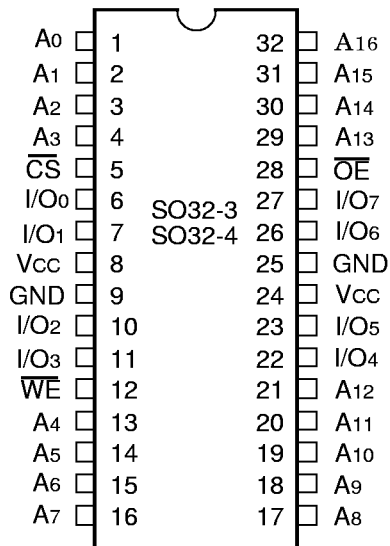
3514 drw 01

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COMMERCIAL TEMPERATURE RANGE

DECEMBER 1996

PIN CONFIGURATION



3514 drw 02

SOJ/TSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0 ⁽²⁾	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.25	W
I _{OUT}	DC Output Current	50	mA

NOTES:

3514 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE^(1,2)

\overline{CS}	\overline{OE}	\overline{WE}	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I _{SB})
V _{HC} ⁽³⁾	X	X	High-Z	Deselected - Standby (I _{SB1})

NOTES:

3514 tbl 01

- H = V_{IH}, L = V_{IL}, x = Don't care.
- V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V.
- Other inputs \geq V_{HC} or \leq V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	8	pF

NOTE:

3514 tbl 03

- This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	V _{CC} +0.5	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

3514 tbl 04

- V_{IL} (min.) = -1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71124		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	5	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	—	5	μA
V _{OL}	Output LOW Voltage	I _{OL} = 8mA, V _{CC} = Min.	—	0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	V

3514 tbl 05

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

($V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

Symbol	Parameter	71124S12 ⁽²⁾		71124S15		71124S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC}	Dynamic Operating Current and $\overline{CS} \leq V_{IL}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = f_{MAX}$ ⁽²⁾	160	—	155	—	140	—	mA
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = f_{MAX}$ ⁽²⁾	35	—	35	—	35	—	mA
I _{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = 0$ ⁽²⁾ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	10	—	10	—	10	—	mA

NOTES:

- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{RC}$ (all address inputs are cycling at f_{MAX}); $f = 0$ means no address input lines are changing.
- 12ns specification is preliminary.

3514 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3514 tbl 07

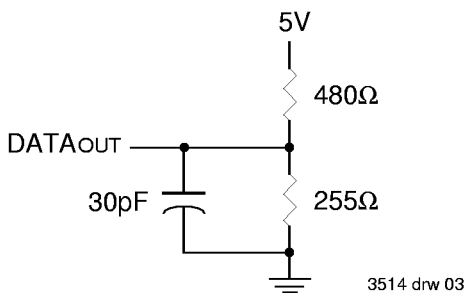
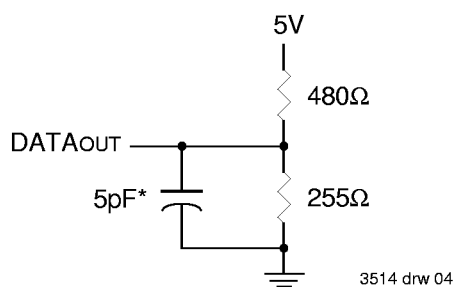


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, Commercial Range)

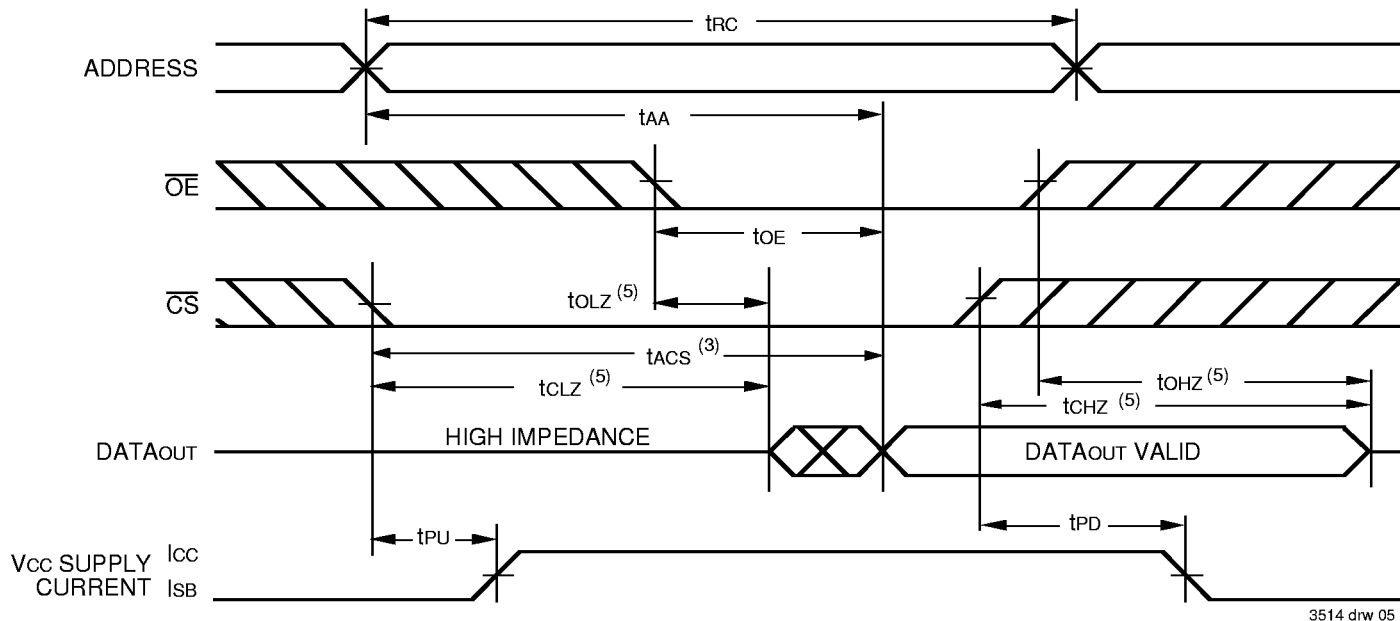
Symbol	Parameter	71124S12 ⁽³⁾		71124S15		71124S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t _{CLZ} ⁽²⁾	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t _{CHZ} ⁽²⁾	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t _{OE}	Output Enable to Output Valid	—	6	—	7	—	8	ns
t _{OLZ} ⁽²⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t _{OHZ} ⁽²⁾	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t _{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t _{PU} ⁽²⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t _{PD} ⁽²⁾	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
Write Cycle								
t _{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End-of-Write	10	—	12	—	15	—	ns
t _{CW}	Chip Select to End-of-Write	10	—	12	—	15	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	10	—	12	—	15	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	ns
t _{OW} ⁽²⁾	Output Active from End-of-Write	3	—	3	—	4	—	ns
t _{WHZ} ⁽²⁾	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

NOTES:

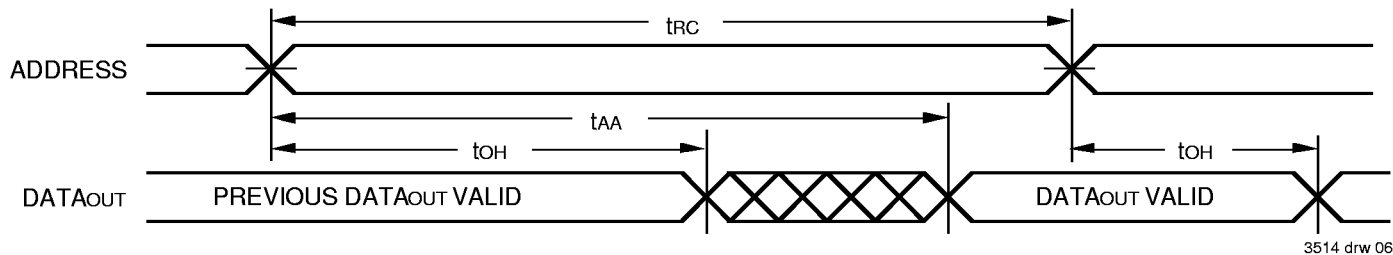
- 0°C to +70°C temperature range only.
- This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
- 12ns specification is preliminary.

3514 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



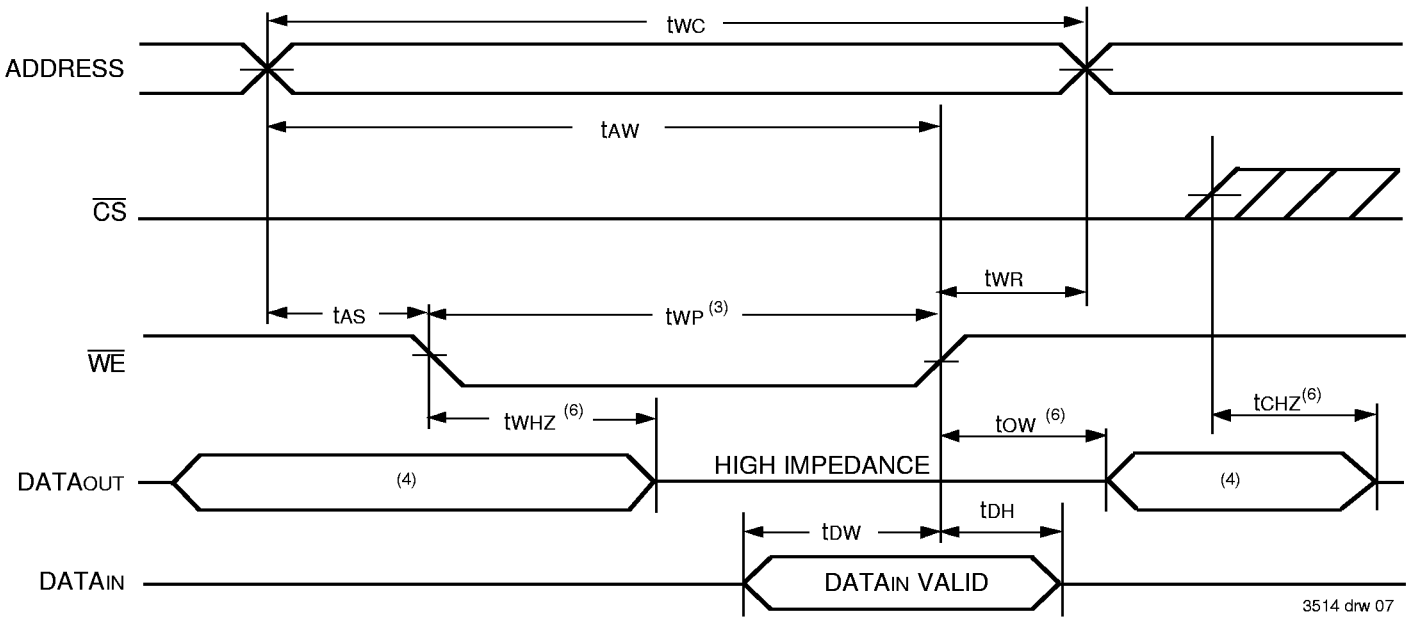
TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



NOTES:

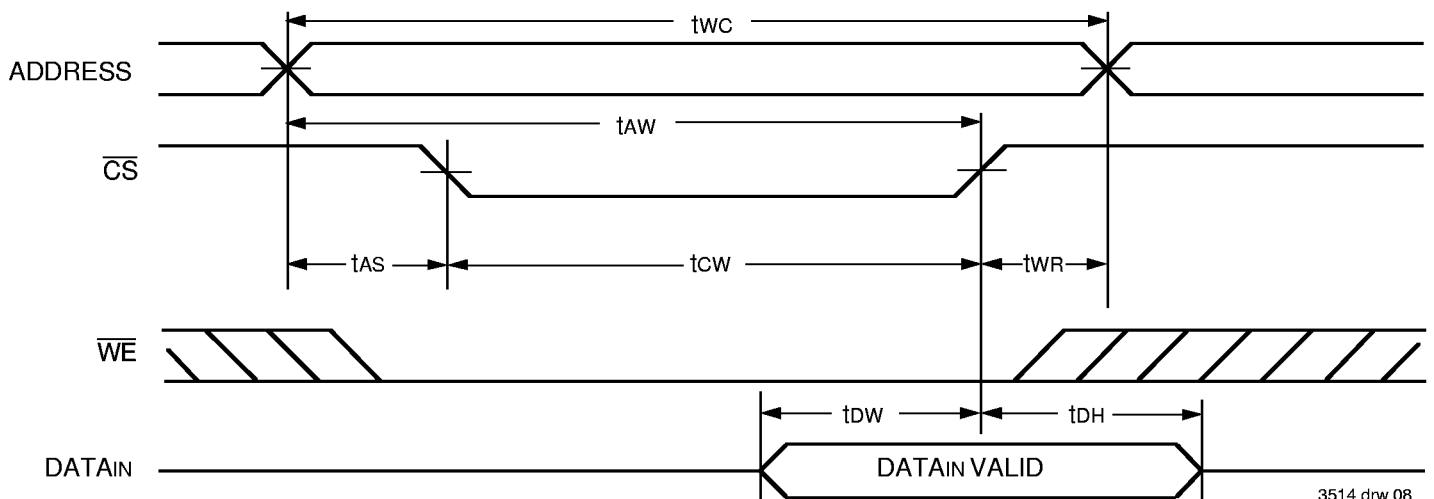
1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address must be valid prior to or coincident with the later of \overline{CS} transition LOW; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200mV$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1, 2, 3, 5)



3514 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1, 2, 5)

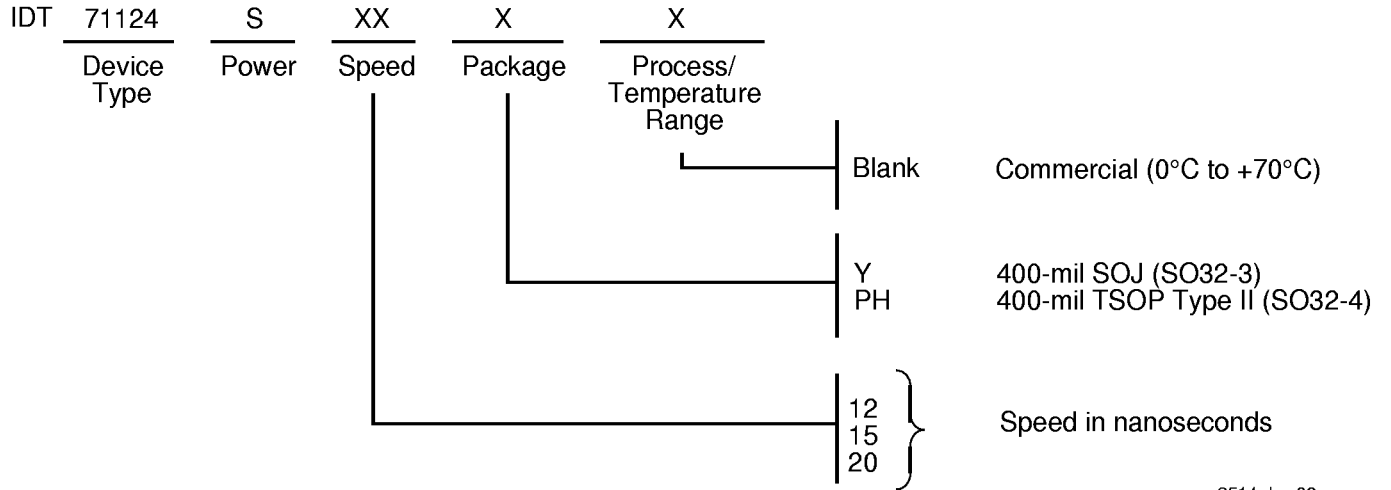


3514 drw 08

NOTES:

1. \overline{WE} must be HIGH, \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
3. \overline{OE} is continuously HIGH. During a \overline{WE} controlled write cycle with \overline{OE} LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high impedance state. \overline{CS} must be active during the t_{CW} write period.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

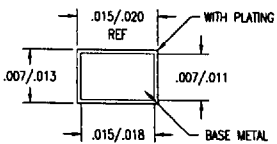
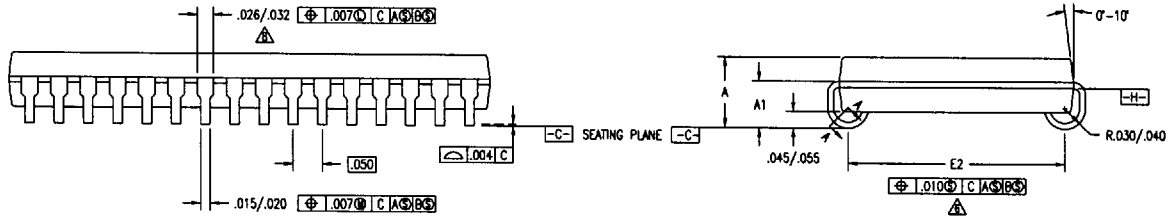
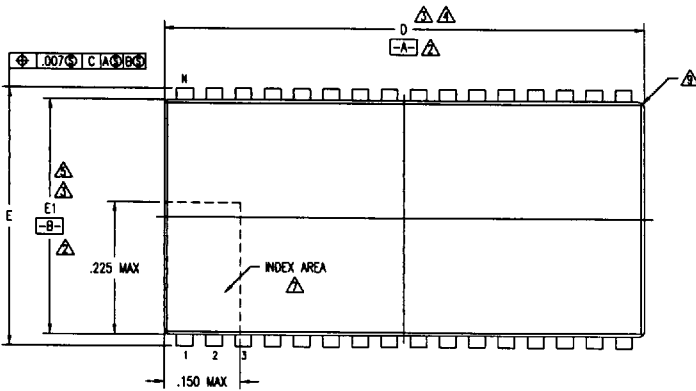
ORDERING INFORMATION



3514 drw 09

PACKAGE DIAGRAM OUTLINES
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20287	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. VU
27321	02	ADD A2 DIM	11/14/94	T. VU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
27945	04	ADD 44 LD	06/25/95	



SECTION A-A

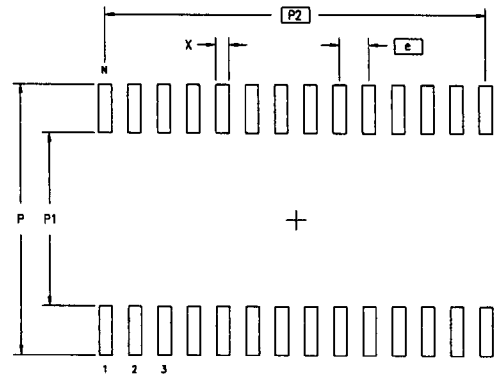
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stonder Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TWC: 910-338-2070
DECIMAL	ANGULAR	
XX±	±	
XXXX		
XXXX±		
APPROVALS	DATE	TITLE
DRWN <i>dt</i>	02/15/96	PB PACKAGE OUTLINE 400" BODY WIDTH SOJ .050" PITCH
CHECKED		
SIZE	DRAWING NO.	REV
C	PSC-4033	04
DO NOT SCALE DRAWING		

PACKAGE DIAGRAM OUTLINES
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20267	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. WU
27321	02	ADD A2 DIM	11/14/94	T. WU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. WU
27945	04	ADD 44 LD	06/25/95	

SYMBOL	JEDEC # S028-6				JEDEC # S032-3				JEDEC # S044-1			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA	MIN	NOM		MAX	AB	MIN		NOM	MAX	AE	
A	.131	.138	.145		.131	.138	.145		.131	.138	.145	
A1	.082	-	-		.082	-	-		.082	-	-	
D	.720	.725	.730	3,4	.820	.825	.830	3,4	1.120	1.125	1.130	3,4
E	.435	.440	.445		.435	.440	.445		.435	.440	.445	
E1	.395	.400	.405	3,5	.395	.400	.405	3,5	.395	.400	.405	3,5
E2	.360	.370	.380	6	.360	.370	.380	6	.360	.370	.380	6
N	28				32				44			

LAND PATTERN DIMENSIONS



NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- DIMENSION E2 TO BE DETERMINED AT SEATING PLANE **-C-** CONTACT POINT
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-061, VARIATION AA, AB & AE

	MIN	MAX	MIN	MAX	MIN	MAX
P	.458	.466	.458	.466	.458	.466
P1	.290	.294	.290	.294	.290	.294
P2	.650 BSC		.750 BSC		1.050 BSC	
X	.018	.026	.018	.026	.018	.026
e	.050 BSC		.050 BSC		.050 BSC	
N	28		32		44	

TOLERANCES UNLESS SPECIFIED		 2875 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TWR: 910-338-2070
DECIMAL	ANGULAR	
XXX	±	
XXXX		
XXXXX		
APPROVALS	DATE	TITLE
DRAWN <i>Ad</i>	02/15/98	PB PACKAGE OUTLINE
CHECKED		.400" BODY WIDTH SOJ
		.050" PITCH
		SIZE C
		DRAWING No. PSC-4033
		REV 04