

# P54/74FCT377T/AT/CT

## OCTAL D FLIP-FLOP WITH CLOCK ENABLE

### ★ FEATURES

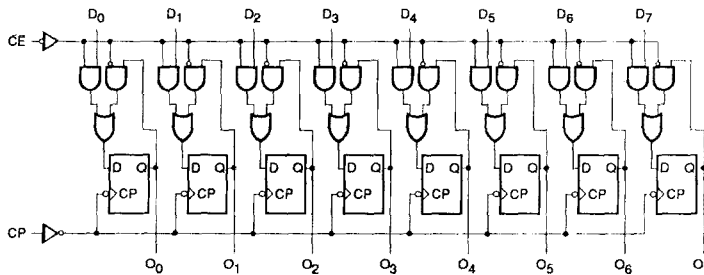
- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.2ns max. (Com'l)  
FCT-A speed at 7.2ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'l), 32 mA (Mil)  
15 mA Source Current (Com'l), 12 mA (Mil)
- Clock Enable for Address and Data Synchronization Application
- Eight Edge-Triggered D Flip-Flops
- Manufactured in 0.7 micron PACE Technology™

### ★ DESCRIPTION

The 'FCT377T have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Clock Enable ( $\overline{CE}$ ) is LOW. The register is fully edge-triggered. The state of each D input one set-

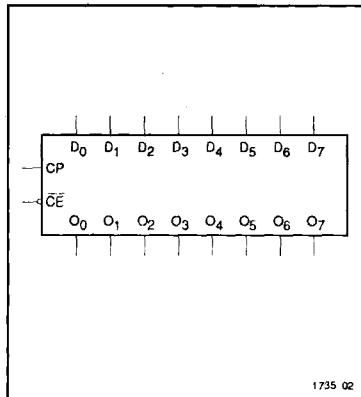
up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The  $\overline{CE}$  input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

### ★ FUNCTIONAL BLOCK DIAGRAM

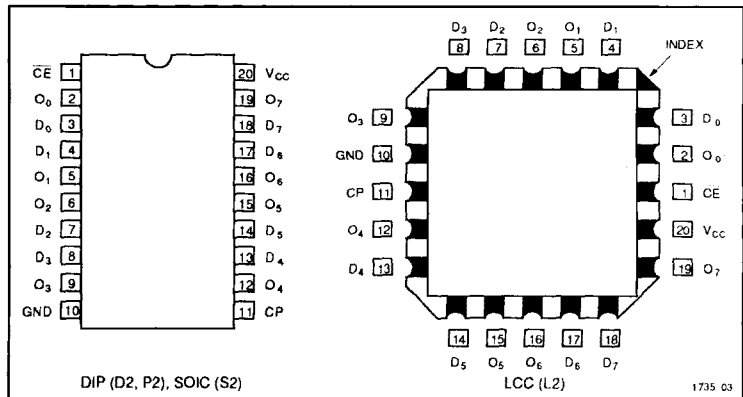


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### ★ LOGIC SYMBOL



### PIN CONFIGURATIONS



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## ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Ambient Temperature Under Bias	-65 to +135	°C
$V_{CC}$	$V_{CC}$ Potential to Ground	-0.5 to +7.0	V
$P_T$	Power Dissipation	0.5	W

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### Notes:

- Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
$I_{OUTPUT}$	Current Applied to Output	120	mA
$V_{IN}$	Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	Voltage Applied to Output	-0.5 to +7.0	V

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- Unused inputs must always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground.

## RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage ( $V_{CC}$ )	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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## DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ <sup>1</sup>	Max	Units	$V_{CC}$	Conditions	
$V_{IH}$	Input HIGH Voltage	2.0			V			
$V_{IL}$	Input LOW Voltage			0.8	V			
$V_H$	Hysteresis		0.2		V		All inputs	
$V_{IK}$	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	$I_{IN} = -18mA$	
$V_{OH}$	Output HIGH Voltage	Military	2.4	3.3	V	MIN	$I_{OH} = -12mA$	
		Commercial	2.4	3.3	V	MIN	$I_{OH} = -15mA$	
$V_{OL}$	Output LOW Voltage	Military		0.3	0.5	V	MIN	$I_{OL} = 32mA$
		Commercial		0.3	0.5	V	MIN	$I_{OL} = 48mA$
		Commercial		0.3	0.5	V	MIN	$I_{OL} = 64mA$
$I_I$	Input HIGH Current			20	μA	MAX	$V_{IN} = V_{CC}$	
$I_{IH}$	Input HIGH Current			5	μA	MAX	$V_{IN} = 2.7V$	
$I_{IL}$	Input LOW Current			-5	μA	MAX	$V_{IN} = 0.5V$	
$I_{OZH}$	Off State $I_{OUT}$ HIGH-Level Output Current			10	μA	MAX	$V_{OUT} = 2.7V$	
$I_{OZL}$	Off State $I_{OUT}$ LOW-Level Output Current			-10	μA	MAX	$V_{OUT} = 0.5V$	
$I_{OS}$	Output Short Circuit Current <sup>2</sup>	-60	-120	-225	mA	MAX	$V_{OUT} = 0.0V$	
$C_{IN}$	Input Capacitance <sup>3</sup>		5	10	pF	MAX	All inputs	
$C_{OUT}$	Output Capacitance <sup>3</sup>		9	12	pF	MAX	All outputs	
$I_{CC}$	Quiescent Power Supply Current		0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$	

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### Notes:

- Typical limits are at  $V_{CC} = 5.0V$ ,  $T_A = +25^\circ C$  ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

- This parameter is guaranteed but not tested.

**DC CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ <sup>1</sup>	Max	Units	Conditions
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 3.4V^2$ , $f_1 = 0$ , Outputs Open
$I_{CCD}$	Dynamic Power Supply Current <sup>3</sup>	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$ , One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{CE} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
$I_C$	Total Power Supply Current <sup>5</sup>	1.7	4.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , $\overline{CE} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , $\overline{CE} = \text{GND}$ , $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		4.0	7.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$ , $\overline{CE} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$ , $\overline{CE} = \text{GND}$ , $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

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**Notes:**

- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$   
( $V_{IN} = 3.4V$ )

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_0 = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$f_1 = \text{Input Frequency}$

$N_1 = \text{Number of Inputs at } f_1$

All currents are in milliamps and all frequencies are in megahertz.

**TRUTH TABLE**

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"		l	h	H
Load "0"		l	l	L
Hold (Do Nothing)		h	X	No Change
	X	H	X	No Change

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H = HIGH Voltage Level

h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition

L = LOW Voltage Level

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition

X = Immaterial

= LOW-to-HIGH Clock Transition



### AC CHARACTERISTICS

Symbol	Parameter	'FCT377T				'FCT377AT				'FCT377CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	2.0	5.5	2.0	5.2	ns	1, 5

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Note: AC Characteristics guaranteed with C<sub>L</sub> = 50pF as shown in Figure 1.

### AC OPERATING REQUIREMENTS

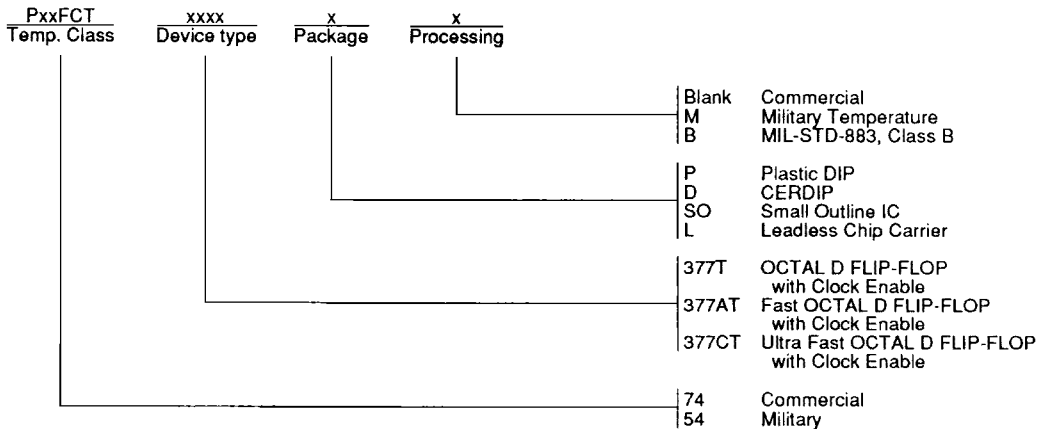
Symbol	Parameter	'FCT377T				'FCT377AT				'FCT377CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW Data to CP	3.0	—	2.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW Data to CP	2.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
t <sub>w</sub> (H) t <sub>w</sub> (L)	Setup Time, HIGH or LOW $\overline{CE}$ to CP	4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns	5
t <sub>w</sub> (H) t <sub>w</sub> (L)	Hold Time, HIGH or LOW $\overline{CE}$ to CP	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	6
t <sub>w</sub> (L)	Clock Pulse Width LOW <sup>2</sup>	7.0	—	7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	ns	6

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**Notes:**

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, t<sub>v</sub>(L) = t<sub>v</sub>(H) = 4.0ns and t<sub>t</sub> = t<sub>r</sub> = 1.0ns.

### ORDERING INFORMATION



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