IXLD02SI
Differential Ultra Fast Laser Diode Driver

Features
- Ultra Fast Pulsed Current Sink
- 17MHz Max Operating Frequency
- <1.5ns Minimum Pulse Width
- 600ps Rise and Fall Times
- Pulse Width and Frequency Agile
- Real Time Electronic Programming of Current and Pulse Width
- Low Inductance High Power Package Design
- Simultaneous Frequency, Pulse Width and Amplitude Modulation

Applications
- High Speed Laser Diode Drivers
- Low Power Ultra Fast Line Drivers
- Differential Power Drivers
- Pulse Generators
- High Speed High Frequency Modulators

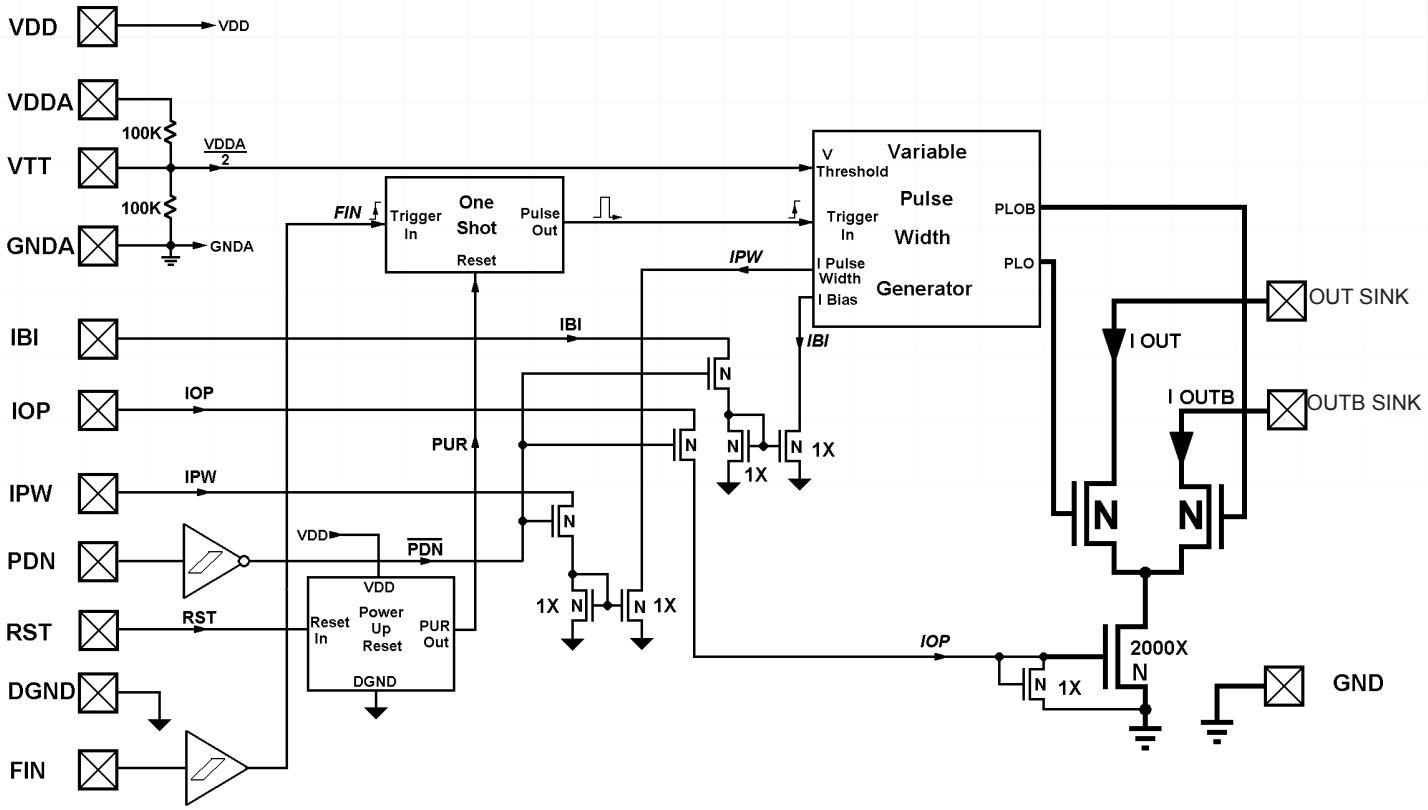
General Description

The IXLD02 is an ultra high-speed differential laser diode driver designed specifically to drive single junction laser diodes. Complementary sink outputs are provided via a low inductance multi-pin topology. These two signals make their transitions at the same time with transition times in the picoseconds. This technique provides the highest possible slew rate across the diode.

These performance features are combined with frequency agility to a maximum operating frequency of 17MHz, a minimum pulse width of <1.5ns and rise and fall times of approximately 600ps. In addition, the pulse width and the current programming can be modulated in real time to >10MHz. The IXLD02 is assembled in a high power SO-28 surface mount package.

For additional operational instructions, see the IXLD02 Evaluation Board application note on the IXYSRF wesite at www.ixysrf.com.

Figure 1 - Functional Diagram



Absolute Maximum Ratings (Note 1)

Name	Definition	Min	Typ	Max	Units	Test Conditions
VDD	Logic supply voltage input	-0.4		5.5	V	
VDDA	Analog bias supply voltage input	-0.4		5.5	V	
VTT	Internal bias voltage input	-0.4	VDDA/2	VDDA+.5	V	
IBI	Internal bias current input	-10	0.1	10	mA	
V_{IBI}	Applied IBI terminal voltage	-0.4		VDDin+0.5	V	
IPW	Pulse width programming current input	-10	0.1	10	mA	
V_{IPW}	Applied IPW terminal voltage	-0.4		VDDin+0.5	V	
IOP	Output sink current programming input	-10	1	10	mA	
V_{IOP}	Applied IOP terminal voltage	-0.4		VDDin+0.5	V	
V_{PDN}	Power-down logic input	-0.4		VDDin+0.5	V	
V_{RST}	Reset logic input	-0.4		VDDin+0.5	V	
V_{FIN}	Pulse frequency logic input	-0.4		VDDin+0.5	V	
I_{OUT}	Output sink pulse current	-0.1		3	A	Note 2
V_{OUT}	True ouput voltage	-0.4		9	V	
IOUTB	Complement output sink pulse current	-0.1		3	A	Note 2
V_{OUTB}	Complement output voltage	-0.4		9	V	
T_C	Device Case Temperature	-40	25	85	°C	Measured at the bottom of the SO28 package heat slug insert
P_D	Package power dissipation @ T_c=85C			32	Watts	SO28 package heat slug insert held at T_C=85°C
R_{THJC}	Thermal resistance, junction to case			2	°C/W	
T_J	Junction Temperature			150	°C	
T_S	Storage temperature	-55		150	°C	
T_L	Lead temperature (soldering, 10 sec)			300	°C	

Note 1: Operating the device beyond parameters with listed "Absolute Maximum Ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Ordering Information			
Part Number	**Package Type**	**Temp Range**	**Grade**
IXLD02SI	28-Pin SOIC	-40°C to +85°C	Industrial

Recommended Operating Conditions

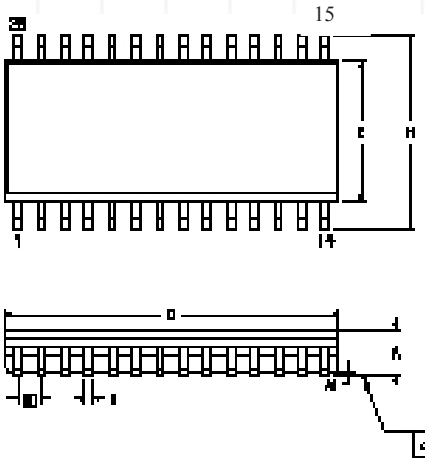
Unless otherwise noted, VDD=VDDA=5V, T_c=25C

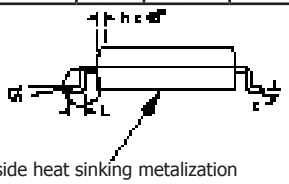
Name	Definition	Min	Typ	Max	Units	Test Conditions
VDD	Logic supply input voltage	4.5		5.5	V	
VDDA	Analog bias supply input voltage	4.5		5.5	V	
VTT	Internal bias voltage input	2	VDDA/2	3	V	Measured with Zin>10meg DVM
R_{VTT}	VTT terminal resistance	30	50	70	Kohms	Measured with VDDin=VDDA=0V
I_{IBI}	Internal bias current input range	10	100	300	uA	External current source between VDDA and IBI terminals
V_{IBI}	Measured IBI terminal voltage	0.6		1.7	V	I_{IBI}=100uA
I_{IPW}	Pulse width programming current input range	-1	100	400	uA	External current source between VDDA and IPW terminals
V_{IPW}	Measured IPW terminal voltage	0.6		1.7	V	I_{IPW}=100uA
t_{PW}	I_{OUT}=2A peak, Output sink current pulse width		1		ns	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA
I_{IOP}	OUT and OUTB output sink current, I_{OUT} programming current	0	1	3	mA	External current source between VDDA and IOP terminals.
V_{IOP}	Measured IOP terminal voltage	0.6		1.7	V	IBI=100uA
I_{OUT}/I_{IOP}	Output current to programming current gain	1800	2000	2200	I/I	I_{IOP}=1mA V_{OUT}=V_{OUTB}=10V
V_{IH}	Logic input high threshold for PDN, RST, & FIN inputs	0.7 *VDD			V	
V_{IL}	Logic input high threshold for PDN, RST, & FIN inputs			.3*VDD	V	
I_{LIN}	Logic input bias current for PDN, RST, & FIN inputs	-10		10	uA	For logic inputs, PDN, RST, & FIN held at:- 0.5V<V_{LIN}<VDD
t_{PDN} disable	IXLD02 power down delay, V_{PDN} logical low to high transition		50		ns	

t_{PDN} enable	IXLD02 power up delay, V_{PDN} logical high to low transition		30		ns	
$t_{RST.}$	IXLD02 reset logic delay, V_{RST} logical low to high transition		100		ns	
$t_{RST.}$	IXLD02 reset logic delay, V_{RST} logical low to high transition		100		ns	
t_{FIN}	IXLD02 pulse frequency input, V_{FIN}, logical low to high transition to I_{OUT} pulse delay		50		ns	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA
f_{FINmax}	Maximum pulse frequency, FIN, logic input	17			MHz	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA
I_{OUT}	Peak pulse sink current	1.6	2	2.4	A Note 2	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA, V_{OUT}=V_{OUTB}=10V
t_R	Rise time		600		ps	
t_F	Fall time		600		ps	
T_{ONDLY}	On-time propagation delay		30		ns	
T_{OFFDLY}	Off-time propagation delay		30		ns	
P_{Wmax}	Pulse width maximum		>1		us	
T_j	Jitter		$\leq$300		ps	
V_{OUT}	OUT terminal voltage	5		7	V	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA, 1.4A<I_{OUT}<2.6A peak
I_{OUTB}	Minimum complement sink pulse current OUTB.	0	0.2	0.4	A	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA., V_{OUT}=V_{OUTB}=10V
V_{OUTB}	OUTB terminal voltage	8		7	V	I_{IBI}=400uA, I_{IPW}=300uA, I_{IOP}=1mA, 0A<I_{OUT}<0.6A minimum

Note 2: The IXLD02 does not provide any output voltage or current, rather it sinks current by manipulating the output SINK MOSFETs in a linear manner. The apparent resistance of the SINK MOSFETs are typically used with external resistors to form two voltage divider networks, one at the anode and one at the cathode of the diode. In order to maintain a nominal reverse and forward diode bias, the external resistors need to be within a certain range of values relative to the resistance presented by the SINK MOSFETs. This range of values however limits the maximum current delivered to the diode and is well below the maximum current level that SINK MOSFETs can actually sink, upwards of 1A is common in practice. Please refer to the EVLD02 application note for further information.

Pin Configurations And Package Outline





Bottom-side heat sinking metalization

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.697	.713	17.70	18.10
E	.291	.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
	0°	8°	0°	8°

NOTE: Bottom-side heat sinking metalization is connected to ground

Pin Description

Pins	Name	Description
1, 2, 13, 14	VDD	This pin is a high current, low inductance pin designed to accept peaks of 2Amps at 5V.
3	VDDA	This is a low current analog power input. Circuit components sensitive to the noise present on VDD in are supplied by this pin.
4	VTT	This pin is the 1/2VDDA internal analog comparator reference point.
5	GNDA	Low current, low noise analog return. Noise sensitive circuit components are returned here.
6	IBI	The current, I_{IBI}, flowing into the IBI pin acts as a baseline current with respect to I_{IPW} current to compensate for internal delays. See Figure 2
7	IOP	A current, I_{IOP}, into the IOP pin programs the laser diode output switches, pins 19 through 24. The program ratio is 1:1000X. This means a 1mA current will produce 1Amp. See Figure 2.
8	IPW	A current, I_{IPW}, flowing into the IPW pin determines the output current pulse width, t_{PW} , w ith respect to I_{IBI}. If I_{IPW}=I_{IBI}, the pulse width is 0. As I_{IPW} approaches I_{IBI} but less than I_{IBI}, the pulse width becomes nonzero. See Figure 2 for t_{PW} as a function of I_{IBI} and I_{IPW}.
9	PDN	A TTL high on this pin will power down the device so that only leakage current will flow from VDD to DGND. A TTL low will turn on the device within 30ns. See Figure 3.
10	RST	A system reset pin, which initializes the device so that it starts in a predetermined initial state.
11	DGND	This pin is the return for the input logic, I_{IBI}, I_{IOP}, and I_{IPW} currents. It is internally connected to the other grounds, AGND or GND, through the substrate.
12	FIN	With PDN low, a positive edge of a TTL compatible signal here will produce the pulse current output available at the OUT and a complement of it at OUTB pins. Refer to Figure 3 for FIN and PDN timing.
15, 16, 17, 18 ,25, 26, 27, 28	GND	Output ground pins designed for low inductance.
19, 20. 21	OUT	True laser d iode drive sink output. Designed for low inductance and output voltage compliance to +7V.
22, 23, 24	OUTB	Complementary laser diode drive sink output. Designed for low inductance and output voltage compliance to +7V.

Figure 2 - Programmed I_{OUT} pulse width, t_{PW} as a function of I_{IPW} and I_{IBI}

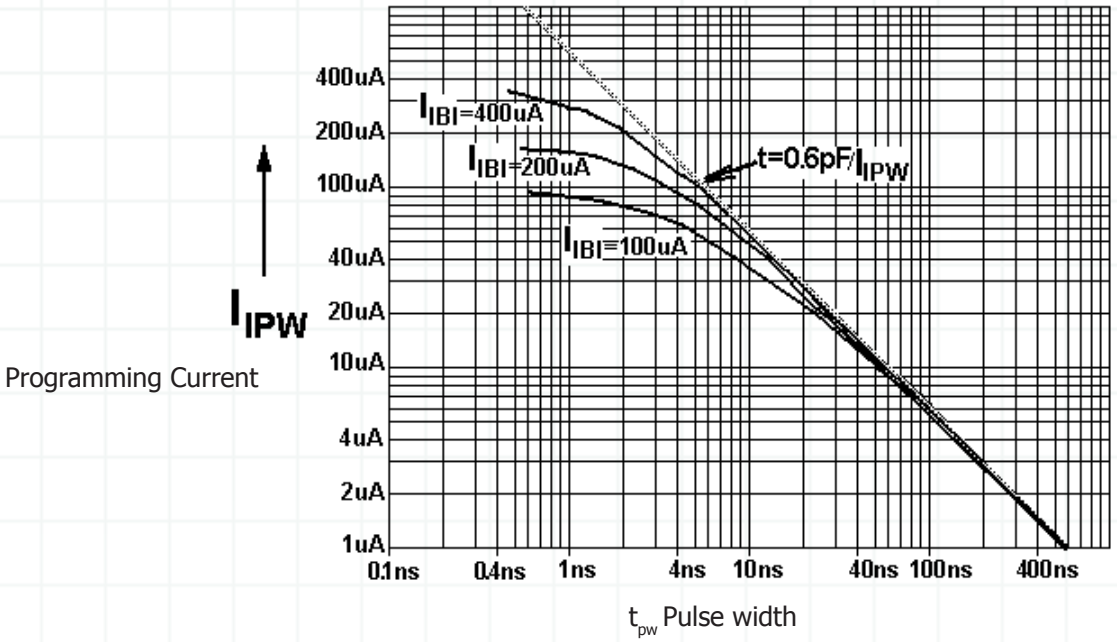


Figure 2 is an illustration of the pulse width vs. programming current. The programming current is typically a DC level, however it could just as well be a time varying signal. The bandwidth of this portion of the IXLD02 is equivalent to the maximum operating frequency of 17MHz. For the fastest response time this pin 8 (IPW) should be driven from a low source impedance.

Figure 3 - Control Gate Timing Diagram

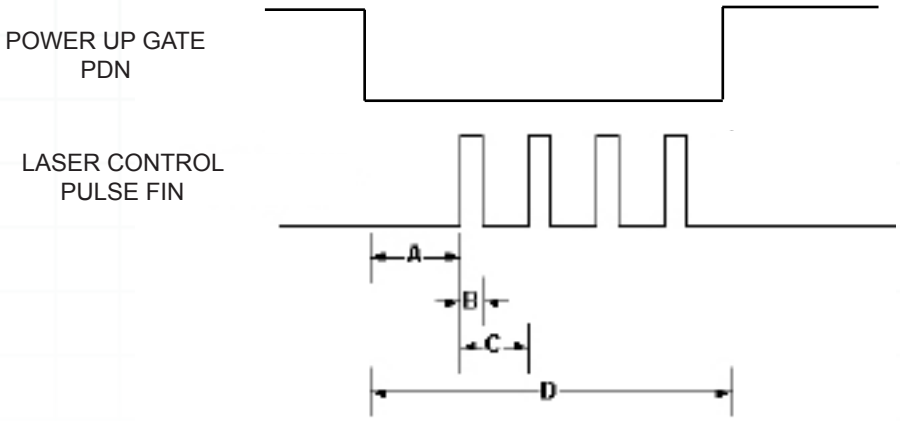


Figure 3 is a timing chart for the IXLD02. The proper gating of the IXLD02 is extremely important. The device is capable of 2A of current and may consume in excess of 3A during the pulse. If the supply voltage is at 7V with 3A of current, the total power dissipated is 21W. Therefore ample heat sinking must be provided, and/or the duty cycle must be limited so that the power dissipation capability of the device is not exceeded.

The Power Up Gate (PDN) is applied to activate the device. Time interval "**A**" can be >30ns. At the end of this time period the control gate "**B**" (FIN), can be applied. The range of "**B**" is from 1ns to several µs. The maximum frequency 1/C is approximately 17MHz.

Figure 4 - Duty Cycle

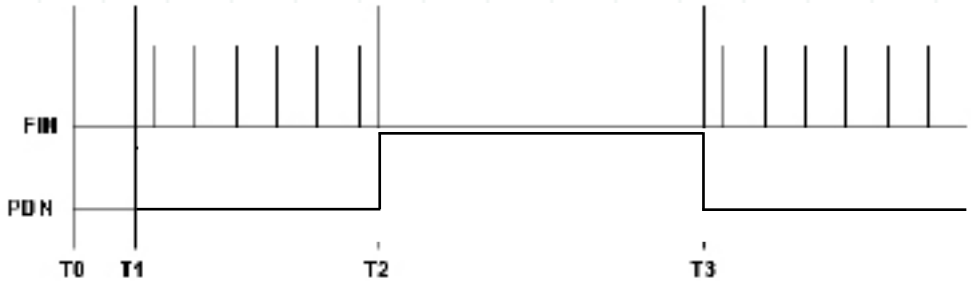


Figure 4 illustrates the Duty Cycle (DC), FIN and PDN relation ships. The PDN command must be in a TTL "High" state 30ns prior to the first FIN pulse. It must stay in this state for the duration of the laser light burst, T1 to T2.

The Duty cycle is defined as:

$$\text{Duty Cycle} = \frac{T2 - T1}{T3 - T1}$$

Power in the IC is: Total DC Power x Duty Cycle

Figure 5 - IPW And IOP Modulation

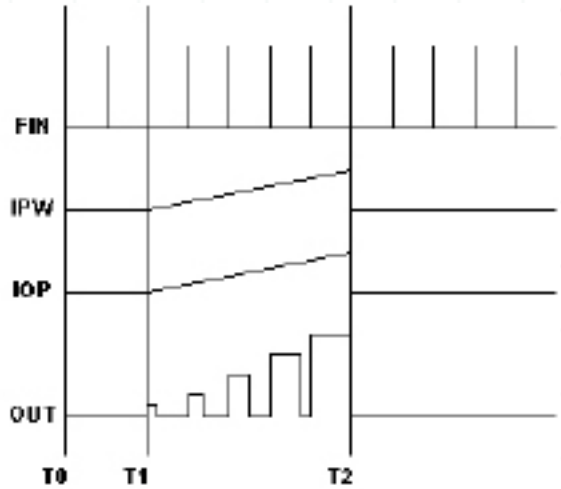


Figure 5 illustrates the simultaneous modulation of both the IPW control current and the IOP control current. The FIN frequency in this figure is held constant. At T0 the IPW and the IOP signals are near zero, both begin to ramp up at T1 and reach their maximums at T2. As illustrated, the output current rises in amplitude with the increasing IOP and the pulse width widens with the IPW ramp.

An additional mode of modulation can be added to the two above by also modulating the frequency of the FIN signal. This will allow three mode of simultaneous modulation. The three modes do not have to be used together; each is fully independent. The obvious caveat is that the pulse width must be consistent with the chosen frequency. This agility provides the designer with a broad range of design choices.