

**1 K x 8  
CMOS DUAL PORT RAM  
3.3 Volt**

**FEATURES**

- SINGLE 3.3 V  $\pm$  0.3 VOLT POWER SUPPLY
- FAST ACCESS TIME  
45 NS(\*) TO 70 NS
- 67130L/67140L LOW POWER
- 67130V/67140V VERY LOW POWER
- EXPANDABLE DATA BUS TO 16 BITS OR MORE  
USING MASTER/SLAVE DEVICES WHEN USING  
MORE THAN ONE DEVICE.
- ON CHIP ARBITRATION LOGIC
- BUSY OUTPUT FLAG ON MASTER
- BUSY INPUT FLAG ON SLAVE
- INT FLAG FOR PORT TO PORT COMMUNICATION
- FULLY ASYNCHRONOUS OPERATION FROM  
EITHER PORT
- BATTERY BACKUP OPERATION :  
2 V DATA RETENTION

**4**

(\*) Preliminary

**INTRODUCTION**

The L 67130/67140 are very low power CMOS dual port static RAMs organized as 1024 x 8. They are designed to be used as a stand-alone 8 bits dual port RAM or as a combination MASTER/SLAVE dual port for 16 bits or more width systems. The MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need for additional discrete logic.

Master and slave devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by CS permits the onchip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8T) memory cell and fabricated with the state of the art 1.0  $\mu$ m lithography named SCMOS, the M67130/140 combine an extremely low standby supply current (typ = 1.0  $\mu$ A) with a fast access time at 45 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5  $\mu$ W.

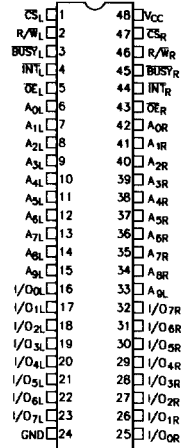
For military/space applications that demand superior levels of performance and reliability the L 67130/140 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

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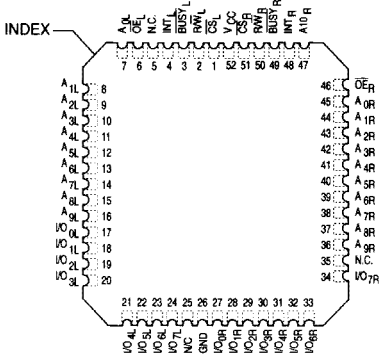
# INTERFACE

## PIN CONFIGURATION

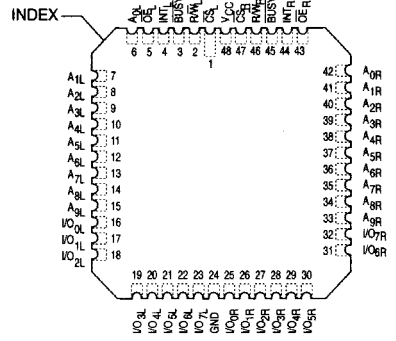
48 PIN DIL (top view), ceramic, plastic 600 mils



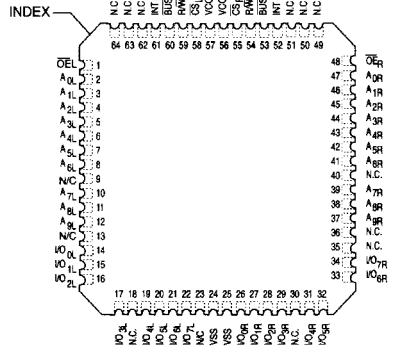
52 PIN PLCC (top view)



48 PIN LCC (top view)

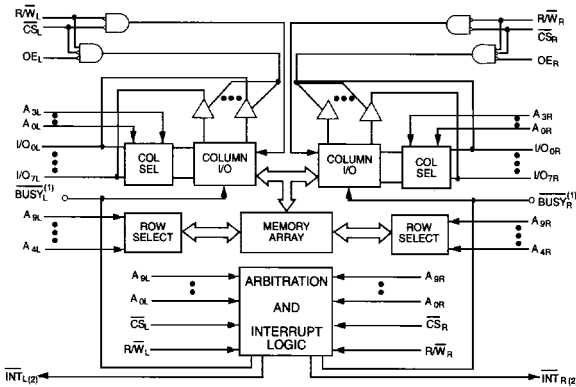


64 PIN VQFP (top view)



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## BLOCK DIAGRAM



**Note 1** : L 67130 (MASTER) : BUSY is open drain output and requires pullup resistor  
 L 67140 (SLAVE) : BUSY in input  
**Note 2** : Open drain output requires pull-up resistor

## PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS}_L$	$\overline{CS}_R$	Chip select
$\overline{R/W}_L$	$\overline{R/W}_R$	Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - 9L$	$A_{0R} - 9R$	Address
$I/O_{0L} - 7L$	$I/O_{0R} - 7R$	Data Input/Output
$BUSY_L$	$BUSY_R$	Busy Flag
$INT_L$	$INT_R$	Interrupt Flag
VCC		Power
GND		Ground

## FUNCTIONAL DESCRIPTION

The L 67130/L 67140 has two ports with separate control, address and I/O pins that permit independent read/write access to any memory location. These devices have an automatic power-down feature controlled by  $\overline{CS}$ .  $\overline{CS}$  controls on-chip power-down circuitry which causes the port concerned to go into stand-by mode when not selected ( $\overline{CS}$  high). When a port is selected access to the full memory array is permitted. Each port has its own Output Enable control ( $\overline{OE}$ ). In read mode, the port's  $\overline{OE}$  turns the Output drivers on when set LOW. Non-conflicting READ/WRITE conditions are illustrated in table 1.

## INTERRUPT LOGIC

The interrupt flag ( $\overline{INT}$ ) allows communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ( $\overline{INT}_L$ ) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Similarly, the right port interrupt flag ( $\overline{INT}_R$ ) is set when the left port writes to memory location 3FF (hex), and the right port must read memory location 3FF in order to clear the interrupt flag ( $\overline{INT}_R$ ). The 8 bit message at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not reserved for mail boxes but become part of the RAM. See table 3 for the interrupt function.

## ARBITRATION LOGIC

The arbitration logic will resolve an address match or a chip select match down to a minimum of 5 ns and determine which port has access. In all cases, an active  $BUSY$  flag will be set for the inhibited port.

The  $BUSY$  flags are required when both ports attempt to access the same location simultaneously. Should this conflict arise, on-chip arbitration logic will determine which port has access and set the  $BUSY$  flag for the inhibited port.  $BUSY$  is set at speeds that allow the processor to hold the operation with its associated address and data. It should be noted that the operation is invalid for the port for which  $BUSY$  is set LOW. The inhibited port will be given access when  $BUSY$  goes inactive.

A conflict will occur when both left and right ports are active and the two addresses coincide. The on-chip arbitration determines access in these circumstances. Two modes of arbitration are provided: (1) if the addresses match and are valid before  $\overline{CS}$  on-chip control logic arbitrates between  $\overline{CS}_L$  and  $\overline{CS}_R$  for access; or (2) if the  $\overline{CS}$ s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to table 2). The inhibited port's  $BUSY$  flag is set and will reset when the port granted access completes its operation in both arbitration modes.

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## DATA BUS WIDTH EXPANSION

## MASTER/SLAVE DESCRIPTION

Expanding the data bus width to 16 or more bits in a dual-port RAM system means that several chips may be active simultaneously. If every chip has a hardware arbitrator, and the addresses for each chip arrive at the same time one chip may activate its  $L\overline{BUSY}$  signal while another activates its  $R\overline{BUSY}$  signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To overcome this "Busy Lock-Out" problem, MHS has developed a MASTER/SLAVE system which uses a single hardware arbitrator located on the MASTER. The SLAVE has  $BUSY$  inputs which allow direct interface to the MASTER with no external components, giving a speed advantage over other systems.

When dual-port RAMs are expanded in width, the SLAVE RAMs must be prevented from writing until the  $BUSY$  input has been settled. Otherwise, the SLAVE chip may begin a write cycle during a conflict situation. On the opposite, the write pulse must extend a hold time beyond  $BUSY$  to ensure that a write cycle occurs once the conflict is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE must be inhibited by the MASTER's maximum arbitration time. If a conflict then occurs, the write to the SLAVE will be inhibited because of the MASTER's  $BUSY$  signal.

TRUTH TABLE

Table 1 : Non contention read/write control .(4)

LEFT OR RIGHT PORT <sup>(1)</sup>				FUNCTION
R/W	CS	OE	D0-7	
X	H	X	Z	Port Disabled and in Power Down Mode. ICCSB or ICCSB1
L	L	X	DATA <sub>IN</sub>	Data on Port Written into memory <sup>(2)</sup>
H	L	L	DATA <sub>OUT</sub>	Data in Memory Output on Port <sup>(3)</sup>
H	L	H	Z	High Impedance Outputs

- Notes : 1.  $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$ .  
 2. If BUSY = L, data is not written.  
 3. If BUSY = L, data may not be valid, see  $t_{WDD}$  and  $t_{DOD}$  timing.  
 4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE.

Table 2 : Arbitration. (6)

LEFT PORT		RIGHT PORT		FLAGS (5)		FUNCTION
CS <sub>L</sub>	A <sub>0L</sub> - A <sub>9L</sub>	CS <sub>R</sub>	A <sub>0L</sub> - A <sub>9R</sub>	BUSY <sub>L</sub>	BUSY <sub>R</sub>	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
<b>ADDRESS ARBITRATION WITH CE LOW BEFORE ADDRESS MATCH</b>						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
<b>CS ARBITRATION WITH ADDRESS MATCH BEFORE CS</b>						
LL5R	= A <sub>0R</sub> - A <sub>9R</sub>	LL5R	= A <sub>0L</sub> - A <sub>9L</sub>	H	L	L-Port Wins
RL5L	= A <sub>0R</sub> - A <sub>9R</sub>	RL5L	= A <sub>0L</sub> - A <sub>9L</sub>	L	H	R-Port Wins
LW5R	= A <sub>0R</sub> - A <sub>9R</sub>	LW5R	= A <sub>0L</sub> - A <sub>9L</sub>	H	L	Arbitration Resolved
LW5R	= A <sub>0R</sub> - A <sub>9R</sub>	LW5R	= A <sub>0L</sub> - A <sub>9L</sub>	L	H	Arbitration Resolved

- Notes : 5. INT Flags Don't Care.  
 6. X = DON'T CARE, L = LOW, H = HIGH.  
 LV5R = Left Address Valid  $\geq$  5 ns before right address.  
 RV5L = Right Address Valid  $\geq$  5 ns before left address.  
 Same = Left and Right Addresses match within 5 ns of each other.  
 LL5R = Left CS = LOW  $\geq$  5 ns before Right CS.  
 RL5L = Right CS = LOW  $\geq$  5 ns before left CS.  
 LW5R = Left and Right CS = LOW within 5 ns of each other.

Table 3 : Interrupt Flag<sup>(7, 10)</sup>

LEFT PORT					RIGHT PORT					FUNCTION
RWL	CSL	OEL	A <sub>0L</sub> -A <sub>9L</sub>	INT <sub>L</sub>	RWR	CSR	OER	A <sub>0R</sub> -A <sub>9R</sub>	INT <sub>R</sub>	
L	L	X	3FF	X	X	X	X	X	L <sup>(8)</sup>	Set Right INT <sub>R</sub> Flag
X	X	X	X	X	X	L	L	3FF	H <sup>(9)</sup>	Reset Right INT <sub>R</sub> Flag
X	X	X	X	L <sup>(9)</sup>	L	L	X	3FE	X	Set Left INT <sub>L</sub> Flag
X	L	L	3FE	H <sup>(8)</sup>	X	X	X	X	X	Reset Left INT <sub>L</sub> Flag

- Notes : 7. Assumes BUSY<sub>L</sub> = BUSY<sub>R</sub> = H.  
 8. If BUSY<sub>L</sub> = L, then NC.  
 9. If BUSY<sub>R</sub> = L, then NC.  
 10. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

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## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND):	- 0.3 V to 7.0 V
Input or output voltage applied:	(GND - 0.3 V) to (VCC + 0.3 V)
Storage temperature:	- 65 °C to + 150 °C

### \* Notice

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE	OPERATING SUPPLY VOLTAGE	OPERATING TEMPERATURE
Military	V <sub>CC</sub> = 3.3 V ± 0.3 %	- 55 °C to + 125 °C
Automotive	V <sub>CC</sub> = 3.3 V ± 0.3 %	- 40 °C to + 125 °C
Industrial	V <sub>CC</sub> = 3.3 V ± 0.3 %	- 40 °C to + 85 °C
Commercial	V <sub>CC</sub> = 3.3 V ± 0.3 %	0 °C to + 70 °C

### DC PARAMETERS

PARAMETER	DESCRIPTION	VERSION	L 67130/ 140-45		L 67130/ 140-55		L 67130/ 140-70		UNIT	VALUE
			COM	IND MIL AUTO	COM	IND MIL AUTO	COM	IND MIL AUTO		
			PRELIMINARY							
I <sub>CCSB</sub> (11)	Standby supply current (Both ports TTL level inputs)	V	1	1	1	1	1	1	mA	Max
		L	5	10	5	10	5	10	mA	Max
I <sub>CCSB1</sub> (12)	Standby supply current (Both ports CMOS level inputs)	V	10	20	10	20	10	20	µA	Max
		L	100	200	100	200	100	200	µA	Max
I <sub>CCOP</sub> (13)	Operating supply current (Both ports active)	V	80	90	70	80	60	70	mA	Max
		L	80	100	70	90	60	80	mA	Max
I <sub>CCOP 1</sub> (14)	Operating supply current (One port active - One port standby)	V	50	55	40	45	35	40	mA	Max
		L	60	65	50	55	45	50	mA	Max

Notes : 11.  $\overline{CS}_L = \overline{CS}_R \geq 2.2$  V.

12.  $\overline{CS}_L = \overline{CS}_R \geq V_{CC} - 0.2$  V.

13. Both ports active - Maximum frequency - Outputs open -  $\overline{OE} = V_{IH}$ .

14. One port active ( $t = t_{MAX}$ ) - Output open - One port stand-by TTL or CMOS Level inputs -  $\overline{CS}_L = \overline{CS}_R \geq 2.2$  V.

PARAMETER	DESCRIPTION	L 67130-45/55/70 L 67140-45/55/70	UNIT	VALUE
I <sub>I/O</sub> (15)	Input/Output leakage current	+/- 10	µA	Max
V <sub>IL</sub> (16)	Input low voltage	0.7	V	Max
V <sub>IH</sub> (16)	Input high voltage	1.8	V	Min
V <sub>OL</sub> (17)	Output low voltage (I/O <sub>0</sub> -I/O <sub>7</sub> )	0.5	V	Max
V <sub>OL</sub>	Open drain output low voltage (BUSY, INT) I <sub>OL</sub> = 16 mA	0.5	V	Max
V <sub>OH</sub> (17)	Output high voltage	1.5	V	Min
C <sub>IN</sub> (21)	Input capacitance	5	pF	Max
C <sub>OUT</sub> (21)	Output capacitance	7	pF	Max

Notes : 15. V<sub>CC</sub> = 5.5 V, V<sub>in</sub> = Gnd to V<sub>CC</sub>,  $\overline{CS} = V_{IH}$ , V<sub>out</sub> = 0 to V<sub>CC</sub>.

16. V<sub>IH</sub> max = V<sub>CC</sub> + 0.3 V, V<sub>IL</sub> min = -0.3 V or -1 V pulse width 50 ns.

17. V<sub>CC</sub> min, I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = -4 mA.

**DATA-RETENTION MODE**

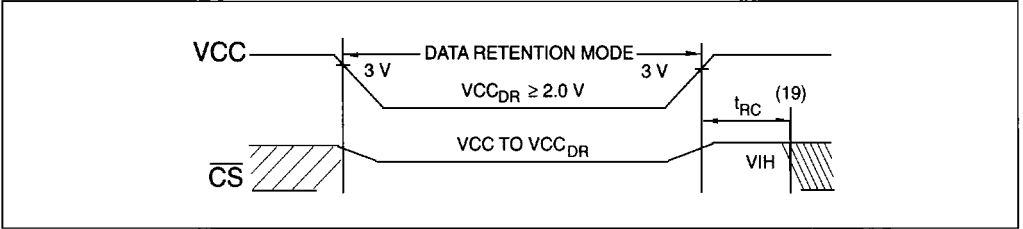
MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1 - Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CCDR}$ .

2 -  $\overline{CS}$  must be kept between  $V_{CC} - 0.2 V$  and 70 % of  $V_{CC}$  during the power up and power down transitions.

3 - The RAM can begin operation  $> t_{RC}$  after  $V_{CC}$  reaches the minimum operating voltage (3 volts).

**TIMING**



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PARAMETER	TEST CONDITIONS (18)	MAX		UNIT
		COM	MIL IND AUTO	
$ICC_{DR1}$	@ $V_{CCDR} = 2 V$	V L	10 200	$\mu A$

Notes : 18.  $\overline{CS} = V_{CC}$ ,  $V_{in} = Gnd$  to  $V_{CC}$ .

19.  $t_{RC}$  = Read cycle time.

**AC TEST CONDITIONS**

Input Pulse Levels : GND to 3.0 V  
 Input Rise/Fall Times : 5 ns  
 Input Timing Reference Levels : 1.5 V

Output Reference Levels : 1.5 V  
 Output Load : see figures 1, 2

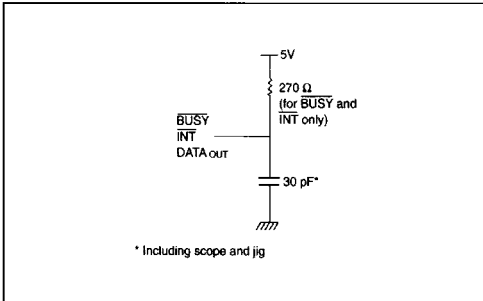


Figure 1 : Output Load.

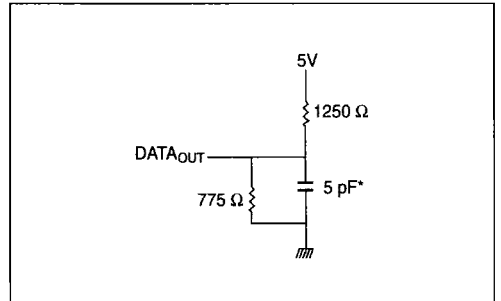


Figure 2 : Output Load.  
 (For  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{WZ}$ , and  $t_{OW}$ )

AC PARAMETERS

READ CYCLE		PARAMETER	L 67130-45 L 67140-45		L 67130-55 L 67140-55		L 67130-70 L 67140-70		UNIT
SYMBOL (23)	SYMBOL (24)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAVR	t <sub>RC</sub>	Read cycle time	45	—	55	—	70	—	ns
TAVQV	t <sub>AA</sub>	Address access time	—	45	—	55	—	70	ns
TELQV	t <sub>ACS</sub>	Chip Select access time (22)	—	45	—	55	—	70	ns
TGLQV	t <sub>AOE</sub>	Output enable access time	—	30	—	35	—	40	ns
TAVQX	t <sub>OH</sub>	Output hold from address change	0	—	0	—	0	—	ns
TELQZ	t <sub>LZ</sub>	Output low Z time (20, 21)	5	—	5	—	5	—	ns
TEHQZ	t <sub>HZ</sub>	Output high Z time (20, 21)	—	20	—	30	—	35	ns
TPU	t <sub>PU</sub>	Chip Select to power up time (21)	0	—	0	—	0	—	ns
TPD	t <sub>PD</sub>	Chip disable to power down time (21)	—	50	—	50	—	50	ns

Notes : 20. Transition is measured ± 500 mV from low or high impedance voltage with load (figures 1 and 2).

21. This parameter is guaranteed but not tested.

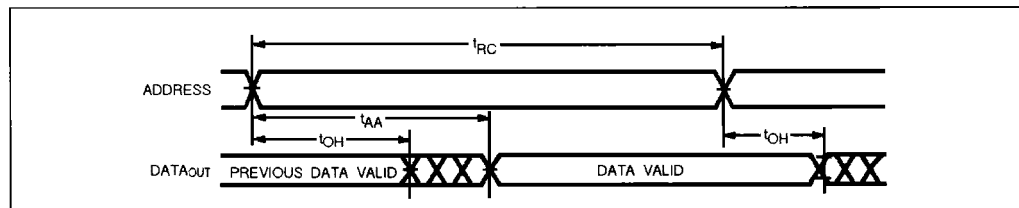
22. To access RAM CS = VIL.

23. STD symbol.

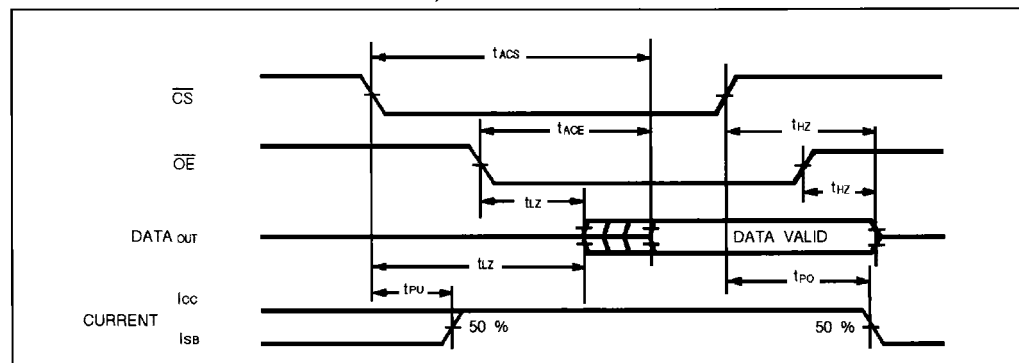
24. ALT symbol.

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TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (25, 26, 28)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (25, 27, 29)



Notes : 25. RW is high for read cycles.

26. Device is continuously enabled, CS = VIL.

27. Addresses valid prior to or coincident with CS transition low.

28. OE = VIL.

29. To access RAM, CS = VIL.

## AC PARAMETERS

WRITE CYCLE		PARAMETER	L 67130-45 L 67140-45		L 67130-55 L 67140-55		L 67130-70 L 67140-70		UNIT
SYMBOL (34)	SYMBOL (35)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAVW	t <sub>WC</sub>	Write cycle time	45	–	55	–	70	–	ns
TELWH	t <sub>SW</sub>	Chip select to end of write (32)	35	–	40	–	45	–	ns
TAVWH	t <sub>AW</sub>	Address valid to end of write	35	–	40	–	45	–	ns
TAVWL	t <sub>AS</sub>	Address Set-up Time	0	–	0	–	0	–	ns
TWLWH	t <sub>WP</sub>	Write Pulse Width	35	–	40	–	45	–	ns
TWHAX	t <sub>WR</sub>	Write Recovery Time	0	–	0	–	0	–	ns
TDVWH	t <sub>DW</sub>	Data Valid to end of write	25	–	25	–	30	–	ns
TGHQZ	t <sub>HZ</sub>	Output high Z time (30, 31)	–	20	–	30	–	40	ns
TWHDX	t <sub>DH</sub>	Data hold time (33)	0	–	0	–	0	–	ns
TWLQZ	t <sub>WZ</sub>	Write enable to output in high Z (30, 31)	–	20	–	30	–	40	ns
TWHQX	t <sub>OW</sub>	Output active from end of write (30, 31, 33)	0	–	0	–	0	–	ns

Notes : 30. Transition is measured  $\pm$  500 mV from low or high impedance voltage with load (figures 1 and 2).

31. This parameter is guaranteed but not tested.

32. To access RAM CS = VIL.

This condition must be valid for entire t<sub>SW</sub> time.

33. The specification for t<sub>DH</sub> must be met by the device supplying write data to the RAM under all operating conditions.

Although t<sub>DH</sub> and t<sub>OW</sub> values vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.

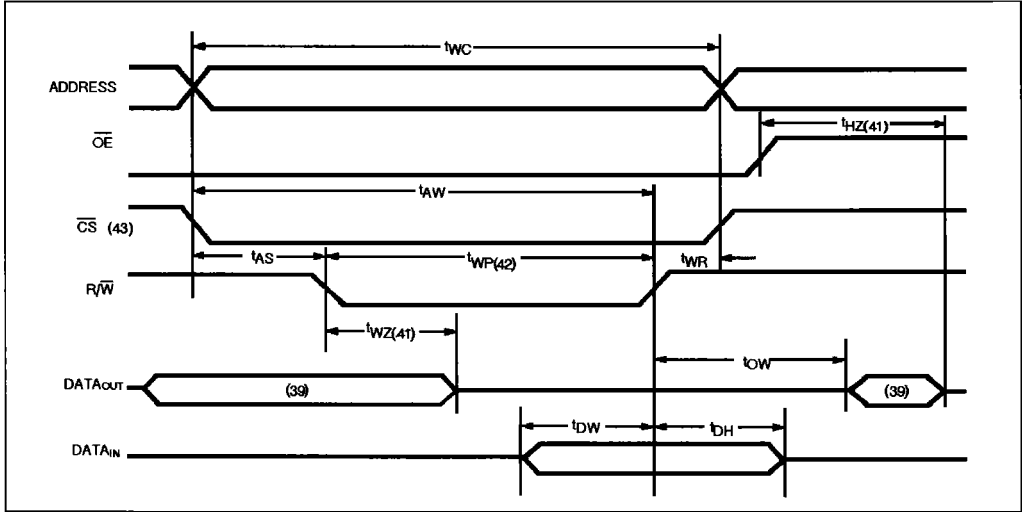
34. STD symbol.

35. ALT symbol.

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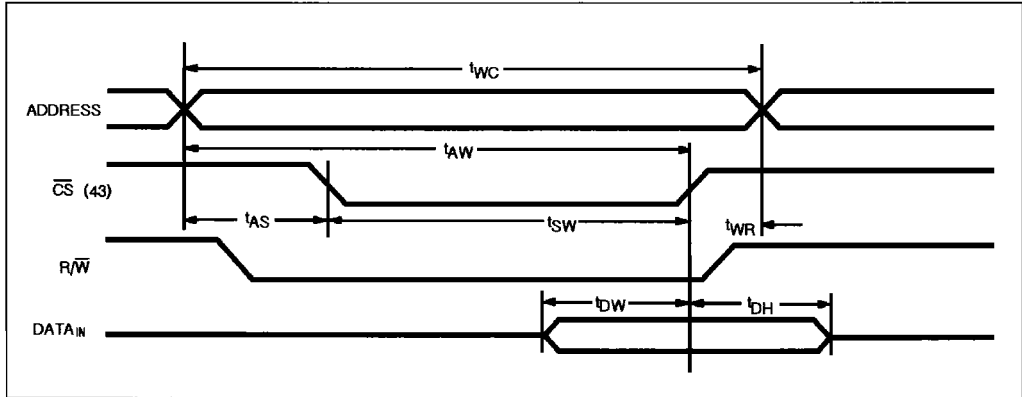


**TIMING WAVEFORM OF WRITE CYCLE NO. 1,  $\overline{R/\overline{W}}$  CONTROLLED TIMING (36, 37, 38, 42)**



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**TIMING WAVEFORM OF WRITE CYCLE NO. 2,  $\overline{CS}$  CONTROLLED TIMING (36, 37, 38, 40)**



- Notes :**
- 36.  $\overline{R/\overline{W}}$  must be high during all address transitions.
  - 37. A write occurs during the overlap ( $t_{sw}$  or  $t_{wp}$ ) of a low  $\overline{CS}$  and a low  $\overline{R/\overline{W}}$ .
  - 38.  $t_{wr}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{R/\overline{W}}$  going high to the end of write cycle.
  - 39. During this period, the I/O pins are in the output state, and input signals must not be applied.
  - 40. If the  $\overline{CS}$  low transition occurs simultaneously with or after the  $\overline{R/\overline{W}}$  low transition, the outputs remain in the high impedance state.
  - 41. Transition is measured  $\pm$  500 mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100 % tested.
  - 42. If  $\overline{OE}$  is low during a  $\overline{R/\overline{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{wp}$  or  $(t_{wz} + t_{ow})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{ow}$ . If  $\overline{OE}$  is high during an  $\overline{R/\overline{W}}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{wp}$ .
  - 43. To access RAM,  $\overline{CS} = \overline{VIL}$ .

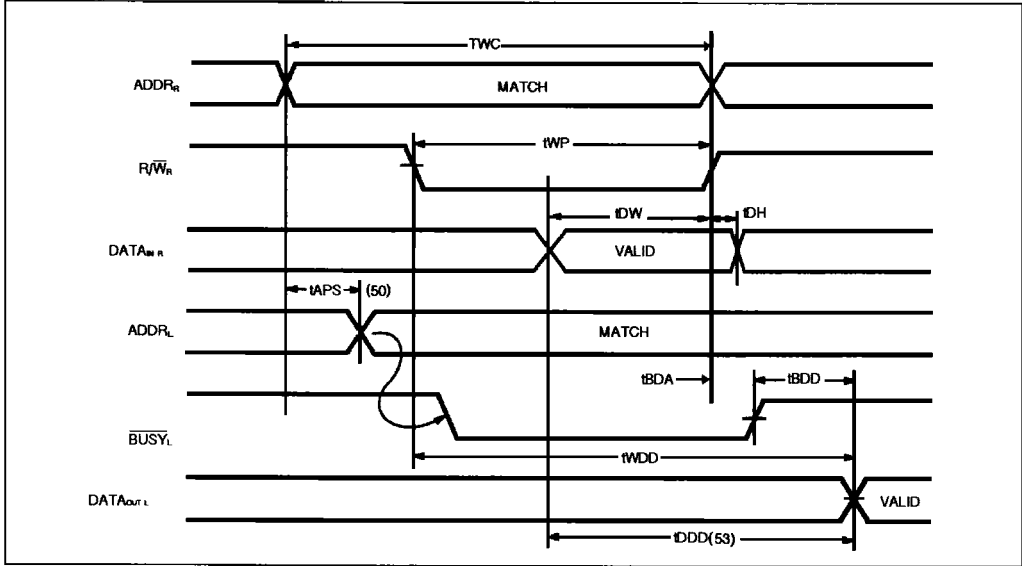
AC PARAMETERS

SYMBOL	PARAMETER	L 67130-45 L 67140-45		L 67130-55 L 67140-55		L 67130-70 L 67140-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
BUSY TIMING (For L 67130 only)								
t <sub>BAA</sub>	BUSY Access time to address	-	35	-	45	-	50	ns
t <sub>BDA</sub>	BUSY Disable time to address	-	35	-	40	-	40	ns
t <sub>BAC</sub>	BUSY Access time to Chip Select	-	30	-	35	-	50	ns
t <sub>BDC</sub>	BUSY Disable time to Chip Select	-	25	-	30	-	40	ns
t <sub>WDD</sub>	Write Pulse to data delay (44)	-	70	-	80	-	90	ns
t <sub>DDD</sub>	Write data valid to read data delay (44)	-	45	-	55	-	70	ns
t <sub>APS</sub>	Arbitration priority set-up time (45)	5	-	5	-	5	-	ns
t <sub>BDD</sub>	BUSY disable to valid data	-	Note 46	-	Note 46	-	Note 46	ns
BUSY TIMING (For L 67140 only)								
t <sub>WB</sub>	Write to BUSY input (47)	0	-	0	-	0	-	ns
t <sub>WH</sub>	Write hold after BUSY (48)	20	-	20	-	20	-	ns
t <sub>WDD</sub>	Write pulse to data delay (49)	-	70	-	80	-	90	ns
t <sub>DDD</sub>	Write data valid to read data delay (49)	-	45	-	55	-	70	ns

4

- Notes :
- 44. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with  $\overline{\text{BUSY}}$  (For L 67130 only)".
  - 45. To ensure that the earlier of the two ports wins.
  - 46. t<sub>BDD</sub> is a calculated parameter and is the greater of 0, t<sub>WDD</sub> - t<sub>WP</sub> (actual) or t<sub>DDD</sub> - t<sub>DW</sub> (actual).
  - 47. To ensure that the write cycle is inhibited during contention.
  - 48. To ensure that a write cycle is completed after contention.
  - 49. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveforms of Read with Port to port delay (For L 67140 only)".

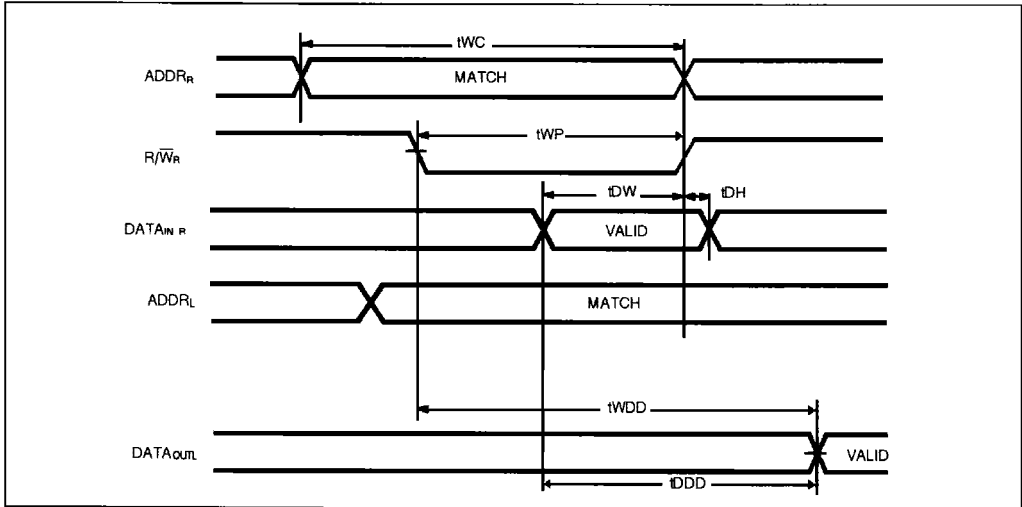
**TIMING WAVEFORM OF READ WITH  $\overline{\text{BUSY}}$  (50, 51, 52) (FOR L 67130)**



4

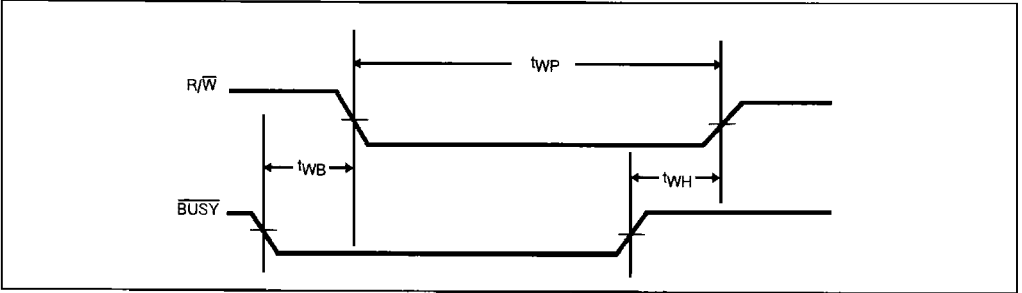
- Notes :**
- 50. To ensure that the earlier of the two port wins.
  - 51. Write cycle parameters should be adhered to, to ensure proper writing.
  - 52. Device is continuously enabled for both ports.
  - 53.  $\overline{\text{OE}}$  at L for the reading port.

**TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT (54, 55, 56) (FOR L 67140 ONLY)**



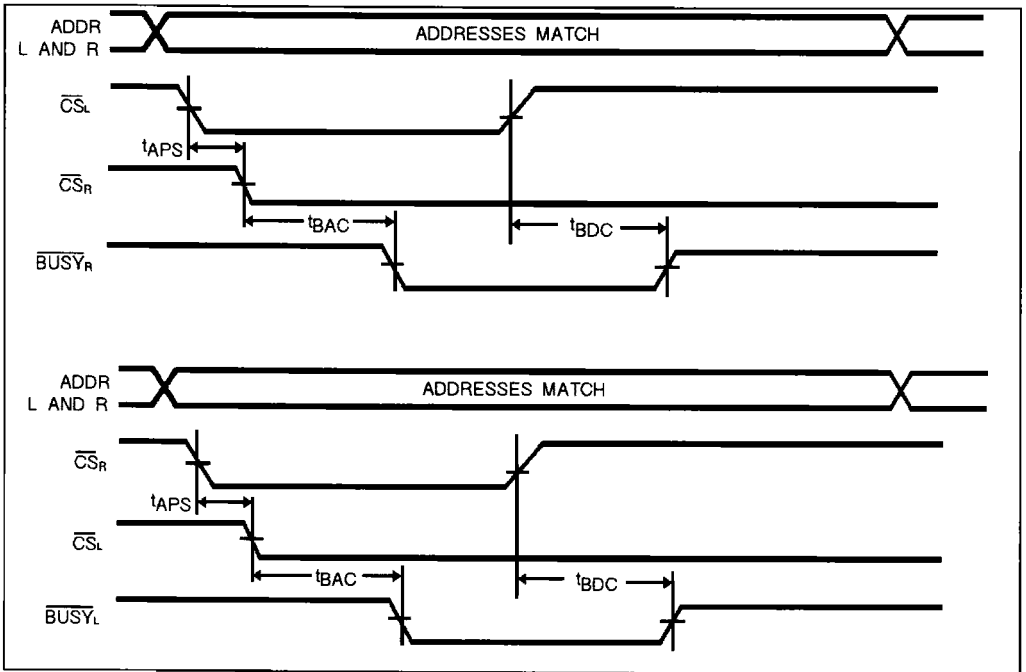
- Notes :**
- 54. Assume  $\text{BUSY} = \text{H}$  for the writing port, and  $\overline{\text{OE}} = \text{L}$  for the reading port.
  - 55. Write cycle parameters should be adhered to, to ensure proper writing.
  - 56. Device is continuously enabled for both ports.

**TIMING WAVEFORM OF WRITE WITH  $\overline{\text{BUSY}}$  (FOR L 67140)**



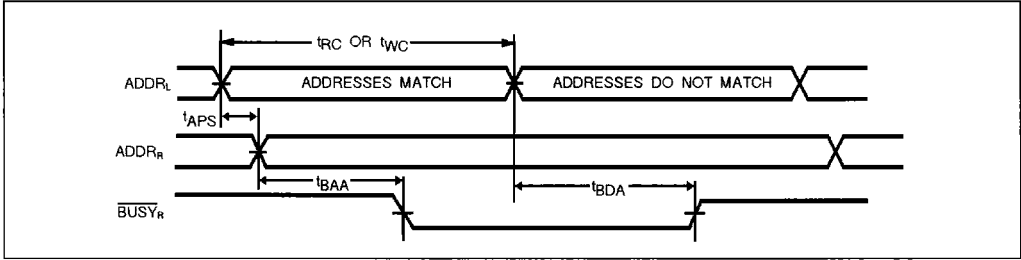
**TIMING WAVEFORM OF CONTENTION CYCLE NO. 1,  $\overline{\text{CS}}$  ARBITRATION (FOR L 67130 ONLY)**

4

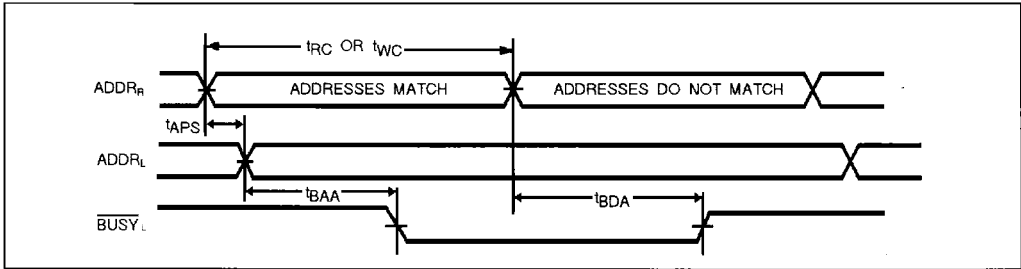


**TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR L 67130 ONLY) <sup>(57)</sup>**

**LEFT ADDRESS VALID FIRST :**



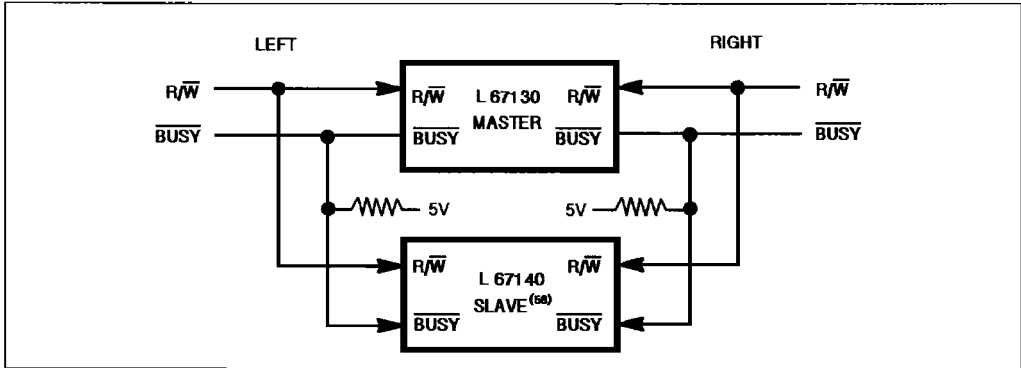
**RIGHT ADDRESS VALID FIRST :**



Note : 57.  $\overline{\text{CS}}_L = \overline{\text{CS}}_R = V_L$

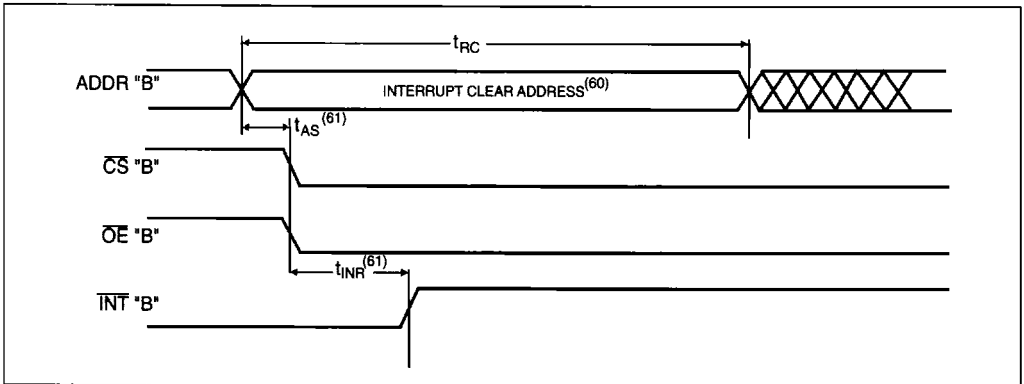
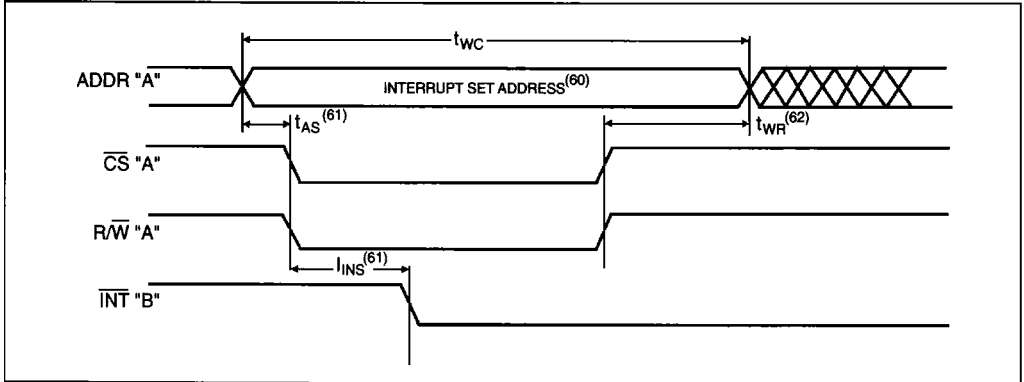
4

**16 BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS**



Note : 58. No arbitration in L 67140 (SLAVE).  $\overline{\text{BUSY}}\text{-IN}$  inhibits write in L 67140 (SLAVE).

WAVEFORM OF INTERRUPT TIMING (59)



- Notes : 59. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
- 60. See interrupt thru table.
- 61. Timing depends on which enable signal is asserted last.
- 62. Timing depends on which enable signal is de-asserted first.

AC ELECTRICAL CHARACTERISTICS OVER THE FULL OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

INTERRUPT TIMING SYMBOL	PARAMETER	L 67130/140-45		L 6 7130/140-55		L 6 7130/140-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>AS</sub>	Address set-up time	0	—	0	—	0	—	ns
t <sub>WR</sub>	Write recovery time	0	—	0	—	0	—	ns
t <sub>INS</sub>	Interrupt set time	—	40	—	45	—	60	ns
t <sub>INR</sub>	Interrupt reset time	—	40	—	45	—	60	ns

## ORDERING INFORMATION

TEMPERATURE RANGE		PACKAGE	DEVICE	SPEED	FLOW
<b>C</b>	<b>L</b>	<b>S3</b>	<b>67130V</b>	<b>55</b>	
	3.3 V ± 0.3 Volt				
	1K = 48 pin DIL ceramic 600 mils CK = 48 pin DIL side-brazed 600 mils 4K = 48 pin LCC S3 = 52 pin PLCC 3K = 48 pin DIL plastic 600 mils RD = 64 pin VQFP			45 ns 55 ns 70 ns	blank = MHS standards /883 = MIL-STD 883 Class B OR S CB = Compliant CECC 90000 level B SHXXX = Special customer request FHXXX = Flight models (space) MHXXX = Mechanical parts (space) LHXXX = Life test parts (space)
C = Commercial I = Industrial A = Automotive M = Military S = Space	0° to +70°C -40° to +85°C -40° to +125°C -55° to +125°C -55° to +125°C	67130 = 8K (1K x 8) Master 67140 = 8K (1K x 8) Slave L = Low power V = Very low power EL = Low power and rad tolerant EV = Very low power and rad tolerant			

