Micro Power Systems

T-51-09-08

MP7628

CMOS
Quad Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **On-Chip Latches for All DAC's**
- **Linearity Grades to ±1/8 LSB**
- **Single Supply Voltage (5 Volt)**
- **DAC's Matched to 1%**
- **Four Quadrant Multiplication**
- **Microprocessor TTL/CMOS Compatible**
- **Read/Write Capability for all DAC's**
- **Latch-Up Free**

APPLICATIONS

- **Microprocessor Controlled Gain and Attenuation Circuits**
- **Microprocessor Controlled/Programmable Power Supplies**
- **Hardware Redundant Applications Requiring Data Readback**
- **PDIP, CDIP, PLCC & SOIC Packages Available**

GENERAL DESCRIPTION

The MP7628 is a quad 8-bit digital-to-analog converter designed using Micro Power Systems' proven decoded DAC architecture featuring excellent DAC-to-DAC matching and guaranteed monotonicity.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

The readback function allows the user to poll or read the data latches, eliminating the need for storing information in RAM. In the event the microprocessor power supply is interrupted, it can poll the DACs to establish the last known system state.

Data is transferred into any of the four DAC data latches via common 8-bit TTL/CMOS compatible input port. Control inputs $\overline{DS1}$, $\overline{DS2}$ and $A/\overline{B}$ determine which DAC is to be loaded. The MP7628's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

The device operates at +5 V power supply and dissipates less than 5mW.

All DAC's offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7628 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Plastic leaded chip carrier (PLCC) and Surface Mount (SOIC) packages.

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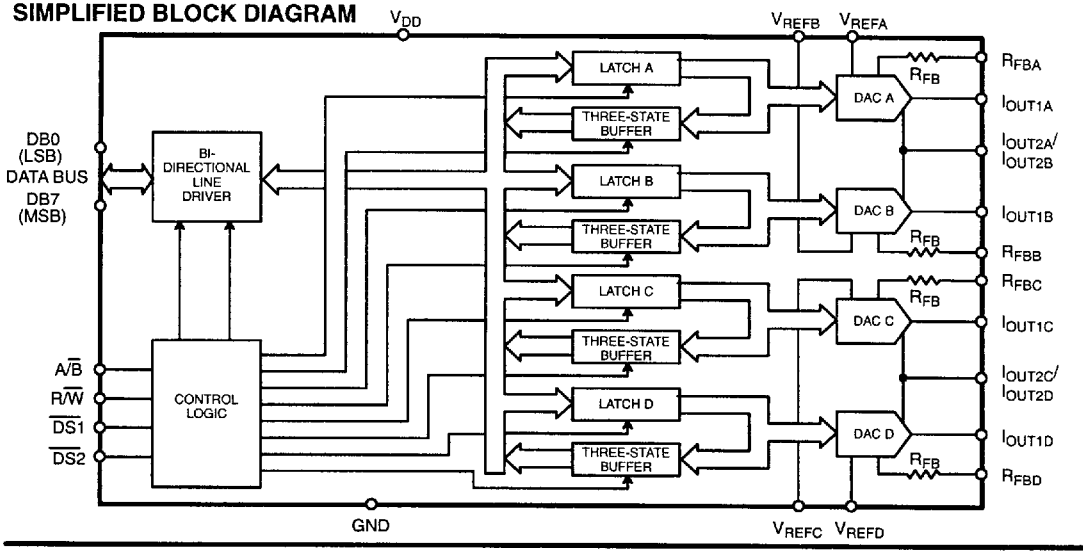
SIMPLIFIED BLOCK DIAGRAM



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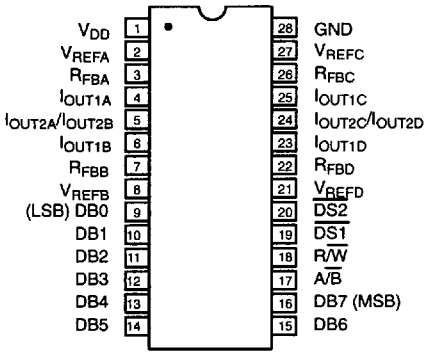
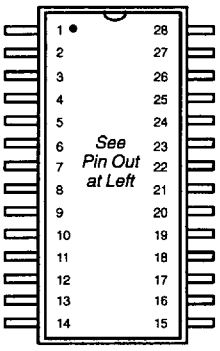
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7628JN	±1/2	±1/2	±1.8
Plastic Dip	–40 to +85°C	MP7628KN	±1/4	±1/4	±0.9
Plastic Dip	–40 to +85°C	MP7628LN	±1/8	±1/8	±0.5
SOIC	–40 to +85°C	MP7628JS	±1/2	±1/2	±1.8
SOIC	–40 to +85°C	MP7628KS	±1/4	±1/4	±0.9
SOIC	–40 to +85°C	MP7628LS	±1/8	±1/8	±0.5
PLCC	–40 to +85°C	MP7628JP	±1/2	±1/2	±1.8
PLCC	–40 to +85°C	MP7628KP	±1/4	±1/4	±0.9
PLCC	–40 to +85°C	MP7628LP	±1/8	±1/8	±0.5
Ceramic Dip	–40 to +85°C	MP7628AD	±1/2	±1/2	±1.8
Ceramic Dip	–40 to +85°C	MP7628BD	±1/4	±1/4	±0.9
Ceramic Dip	–40 to +85°C	MP7628CD	±1/8	±1/8	±0.5
Ceramic Dip	–55 to +125°C	MP7628SD	±1/2	±1/2	±1.8
Ceramic Dip	–55 to +125°C	MP7628SD/883	±1/2	±1/2	±1.8
Ceramic Dip	–55 to +125°C	MP7628TD	±1/4	±1/4	±0.9
Ceramic Dip	–55 to +125°C	MP7628TD/883	±1/4	±1/4	±0.9
Ceramic Dip	–55 to +125°C	MP7628UD	±1/8	±1/8	±0.5
Ceramic Dip	–55 to +125°C	MP7628UD/883	±1/8	±1/8	±0.5

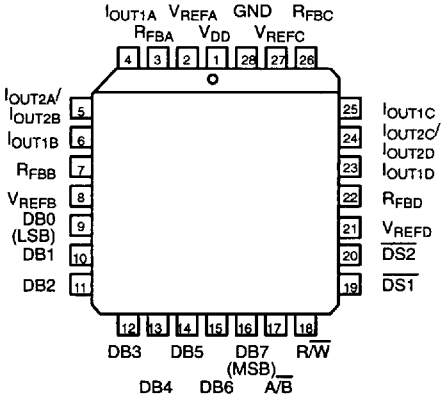
PIN CONFIGURATIONS



28 Pin CDIP, PDIP (0.600")
D28, N28



28 Pin SOIC (Jedec, 0.300")
S28



28 Pin PLCC
P28

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PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	V_{REFA}	Reference Voltage for DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	I_{OUT1A}	Current Output 1 DAC A
5	I_{OUT2A}/ I_{OUT2B}	Current Output 2 DAC A/DAC B
6	I_{OUT1B}	Current Output 1 DAC B
7	R_{FBB}	Feedback Resistor for DAC B
8	V_{REFB}	Reference Voltage for DAC B
9	DB0	Data Bit 0 (LSB)
10	DB1	Data Bit 1
11	DB2	Data Bit 2
12	DB3	Data Bit 3
13	DB4	Data Bit 4
14	DB5	Data Bit 5
15	DB6	Data Bit 6
16	DB7	Data Bit 7 (MSB)
17	A/$\overline{B}$	DAC Selection
18	R/$\overline{W}$	Read/Write
19	$\overline{DS1}$	Control 1
20	$\overline{DS2}$	Control 2
21	V_{REFD}	Reference Voltage for DAC D
22	R_{FBD}	Feedback Resistor for DAC D
23	I_{OUT1D}	Current Output 1 DAC D
24	I_{OUT2C}/ I_{OUT2D}	Current Output 2 DAC C/DAC D
25	I_{OUT1C}	Current Output 1 DAC C
26	R_{FBC}	Feedback Resistor for DAC C
27	V_{REFC}	Reference Voltage for DAC C
28	GND	Ground

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ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE (1)								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
L, C, U				±1/8		±1/8		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
L, C, U				±1/8		±1/8		
Gain Error	GE						% FSR	Using Internal R_{FB}
J, A, S				±1.5		±1.8		Digital Inputs = V_{INH}
K, B, T				±0.8		±0.9		
L, C, U				±0.4		±0.5		
Gain Temperature Coefficient (2)	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (all)	I_{OUT1}			±50		±200	nA	Digital Inputs = V_{INL}
REFERENCE INPUT								
Voltage Range (2)				±20		±20	V	
Input Resistance	R_{IN}	12		28	12	28	kΩ	
DIGITAL INPUTS (3)								
Logic Thresholds								
V_{INH}		2.4			2.4		V	
V_{INL}				0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance (2)	C_{IN}		3				pF	
DATA BUS OUTPUTS								
Output Capacitance (2)	C_{OUT}		7				pF	
Input Leakage Current	I_{LKG}			±1		±10	µA	
ANALOG OUTPUTS								
Propagation Delay (2)		500			750		ns	From digital input to 90% of final analog output current
Output Capacitance (2)								
	C_{OUT}		120				pF	DAC Inputs all 1's
	C_{OUT}		80				pF	DAC Inputs all 0's
Glitch Energy (2)		160			440		nVs	Typical for code transition from all 0's to all 1's

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ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY (5)								
Functional Voltage Range (2)	V_{DD}	4.5		5.5	4.5	5.5	V	
Supply Current	I_{DD}			50		50	µA	All digital inputs = 0 V or all = 5 V
SWITCHING CHARACTERISTICS (2, 4)								
Data Write Time	t_W	320			400		ns	
Write Strobe Req.	t_{DSW}	200			250		ns	
Data Hold Time	t_{DHLD}	40			50		ns	
Data Read Time	t_R	480			600		ns	
Tri-State Hold Time	t_{TSHD}	240			300		ns	
Read Strobe Req.	t_{DSR}	320			400		ns	

NOTES:

(1) Full Scale Range (FSR) is 10V for unipolar mode.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) See timing diagrams.
(5) Specified values guarantee functionality. Refer to other parameters for accuracy.

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Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... +7 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND (2) ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

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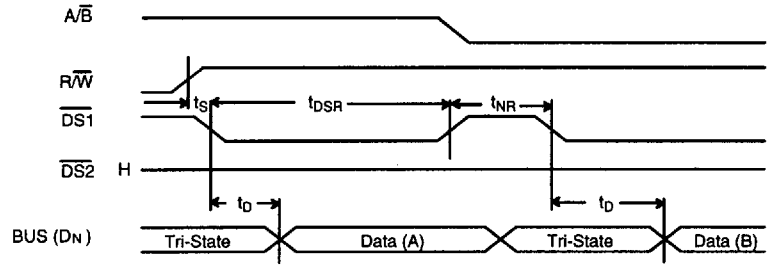
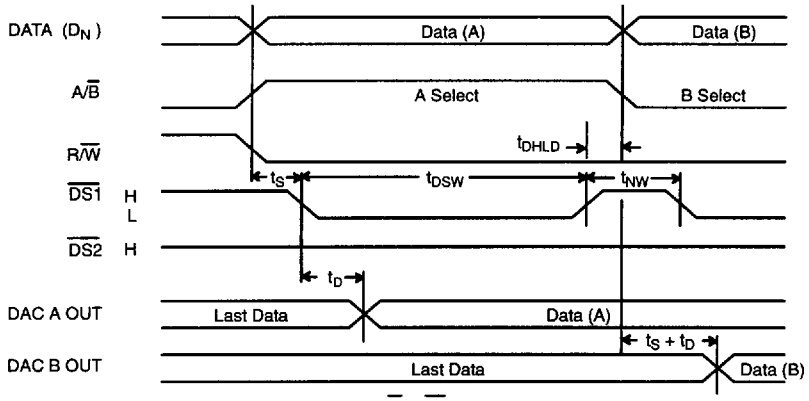
TIMING DIAGRAM READ CYCLE



Set up time for BUS, A/B, R/W	= 40 ns	t_S
Minimum DS = low pulse	= 320 ns	t_{DSR} (min)
Minimum time between DS = low pulses	= 120 ns	t_{NR}
Data delay time	= 200 ns	t_D

$t_R = t_{DSR} + t_{NR}$

TIMING DIAGRAM WRITE CYCLE



Set up time for BUS, A/B, R/W	= 40 ns	t_S
Minimum DS = low pulse	= 200 ns	t_{DSW} (min)
Minimum time between DS = low pulses	= 120 ns	t_{NW}
Data delay time	= 110 ns	t_D

$t_W = t_{DSW} + t_{NW}$

MODE SELECTION TABLE

DS1	DS2	A/B	R/W	MODE	DAC
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A & C
L	L	L	L	WRITE	B & D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE
H = HIGH STATE
X = DON'T CARE

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INTERFACE LOGIC INFORMATION

DAC Selection: All DAC latches share a common 8-bit input port. The control inputs $\overline{DS1}$, $\overline{DS2}$ A/$\overline{B}$ select which DAC can accept data from the input port.

Mode Selection: Inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC. *See Mode Selection Table on the previous page.*

Write Mode: When $\overline{DS}$ and R/$\overline{W}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7.

Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{DS}$ and R/$\overline{W}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode and the data held in the appropriate latch is outputed to the data bus.

APPLICATION NOTES

Refer to Section 8 for Applications Information

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