

## DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- HIGH SPEED:  $t_{pD} = 5 \text{ ns}$  (TYP.) at  $V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 2 \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:  
 $V_{IH} = 2V$  (MIN.),  $V_{IL} = 0.8V$  (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(\text{OPR}) = 4.5V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 139
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The 74VHCT139A is an advanced high-speed CMOS DUAL 2 TO 4 LINE DECODER/DEMULTIPLEXER fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

The active low enable input can be used for gating or as a data input for demultiplexing applications. When the enable input is held high, all four outputs are high independently of the other inputs.



**Table 1: Order Codes**

PACKAGE	T & P
SOP	74VHCT139AMTR
TSSOP	74VHCT139ATTR

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

**Figure 1: Pin Connection And IEC Logic Symbols**

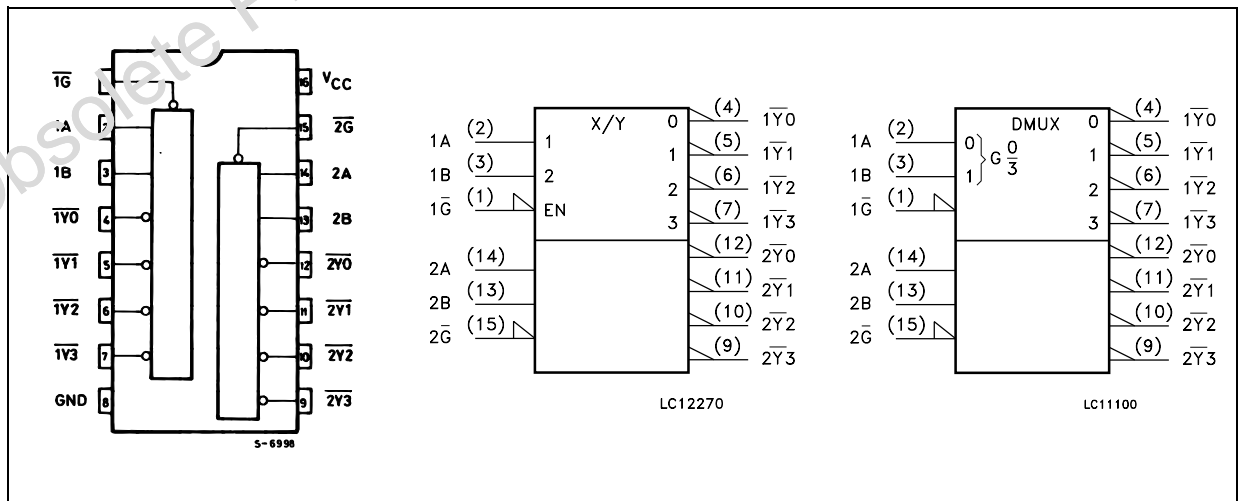


Figure 2: Input Equivalent Circuit

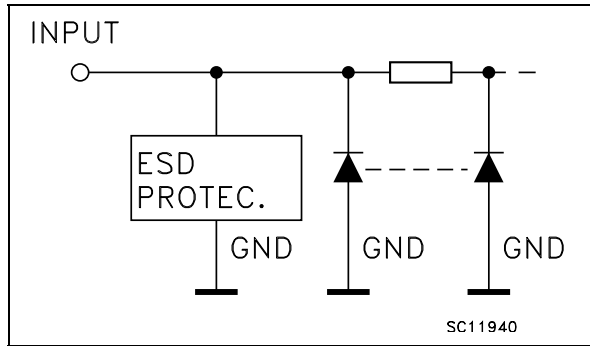


Table 2: Pin Description

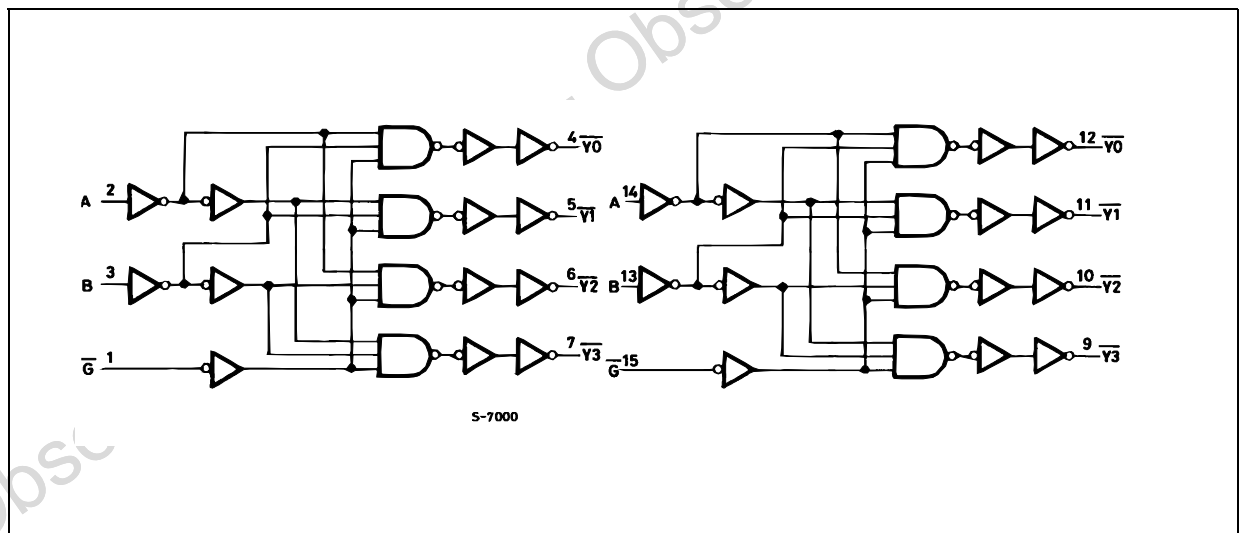
PIN N°	SYMBOL	NAME AND FUNCTION
1, 15	1G, 2G	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	1Y0 to 1Y3	Outputs
12, 11, 10, 9	2Y0 to 2Y3	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

**Table 4: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 1)	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1)  $V_{CC} = 0V$

2) High or Low State

**Table 5: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage (see note 1)	0 to 5.5	V
$V_O$	Output Voltage (see note 2)	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 20	ns/V

1)  $V_{CC} = 0V$

2) High or Low State

3)  $V_{IN}$  from 0.8V to 2V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		20	μA
+I <sub>CC</sub>	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V <sub>CC</sub> or GND			1.35		1.5		1.5	mA
I <sub>OPD</sub>	Output Leakage Current	0	V <sub>OUT</sub> = 5.5V			0.5		5.0		5.0	μA

Table 7: AC Electrical Characteristics (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> <sup>(*)</sup> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time A, B, to Y	5.0	15		5.0	7.2	1.0	8.5	1.0	8.5	ns
		5.0	50		6.5	9.2	1.0	10.5	1.0	10.5	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time G to Y	5.0	15		4.4	6.3	1.0	7.5	1.0	7.5	ns
		5.0	50		5.9	8.3	1.0	9.5	1.0	9.5	

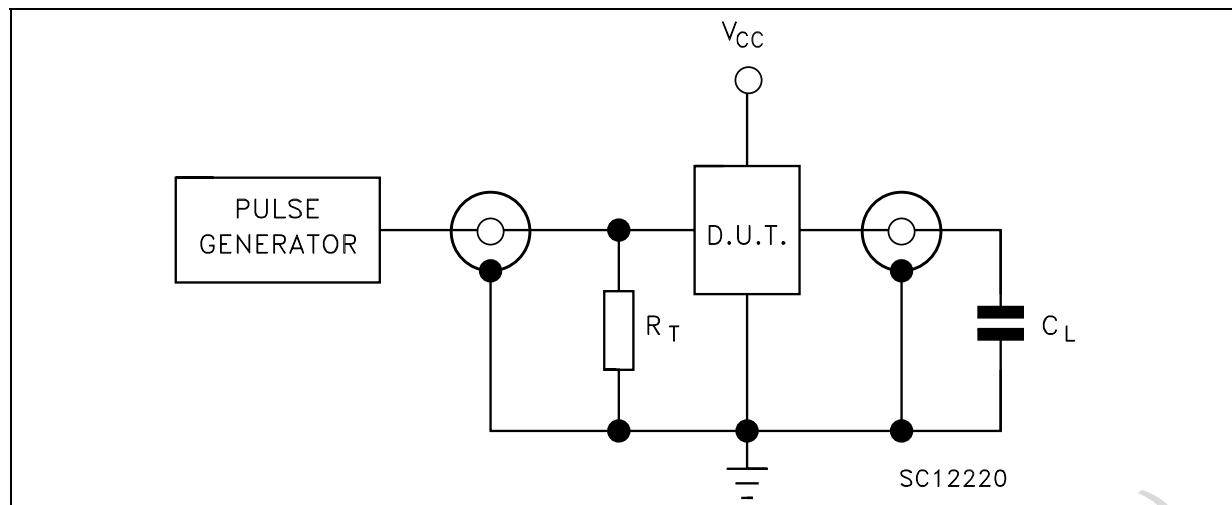
(\*) Voltage range is 5.0V ± 0.5V

Table 8: Capacitive Characteristics

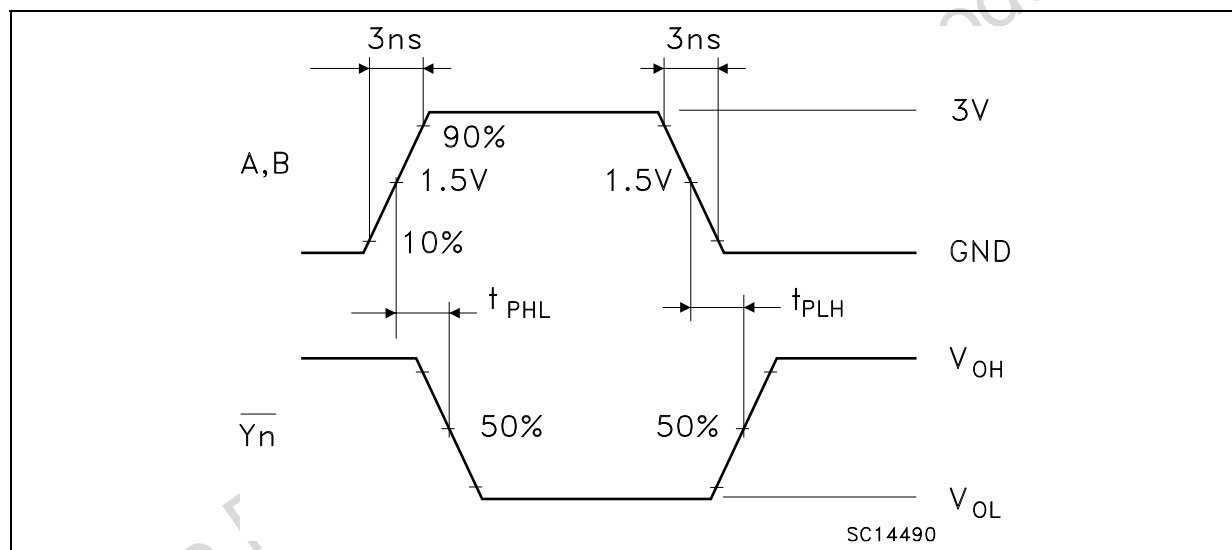
Symbol	Parameter	Test Condition		Value						Unit	
				T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance				6	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)				18						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/2 (per decoder)

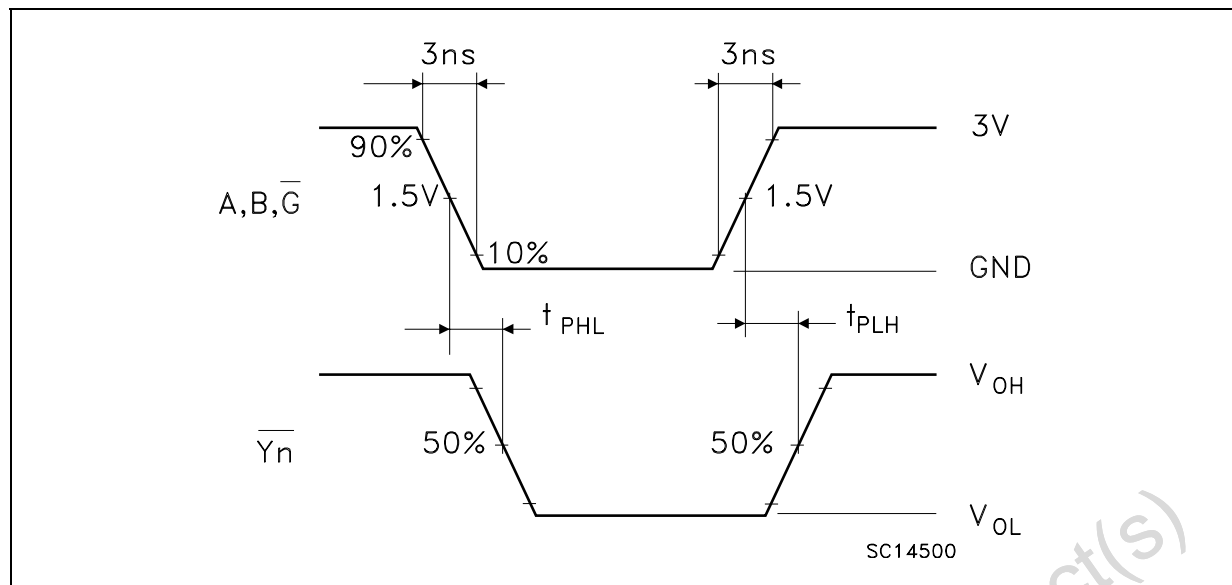
Figure 4: Test Circuit



$C_L = 15/50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

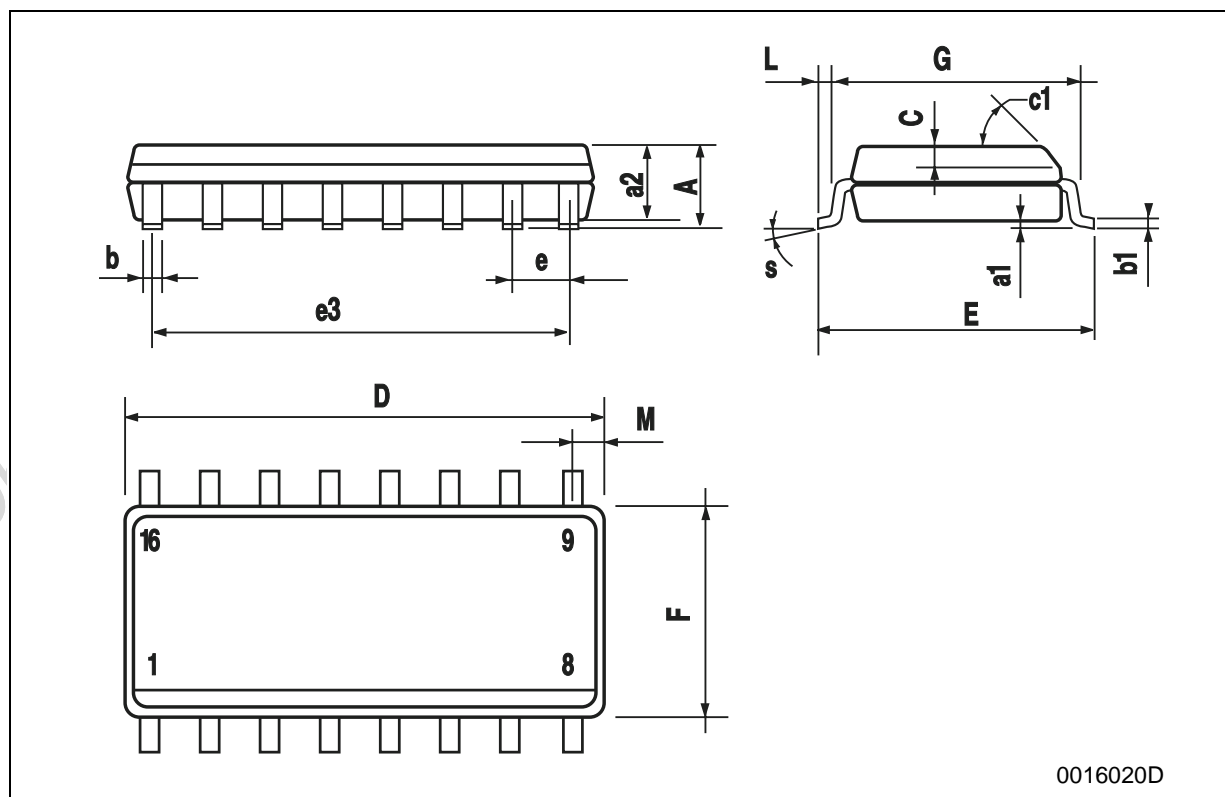
Figure 5: Waveform - Propagation Delays For Inverting Outputs ( $f=1\text{MHz}$ ; 50% duty cycle)

SC14490

Figure 6: Waveform - Propagation Delays For Non-inverting Outputs ( $f=1\text{MHz}$ ; 50% duty cycle)

## SO-16 MECHANICAL DATA

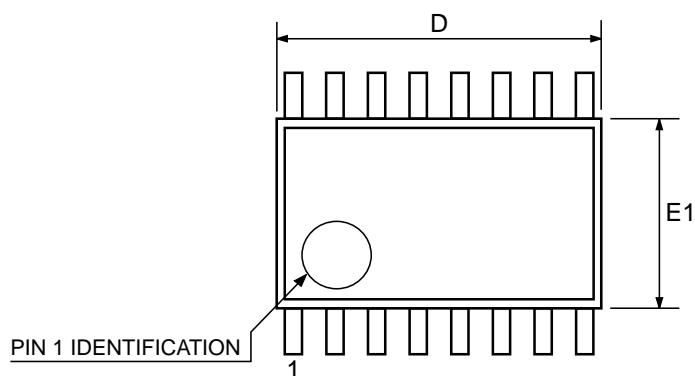
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



0016020D

## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

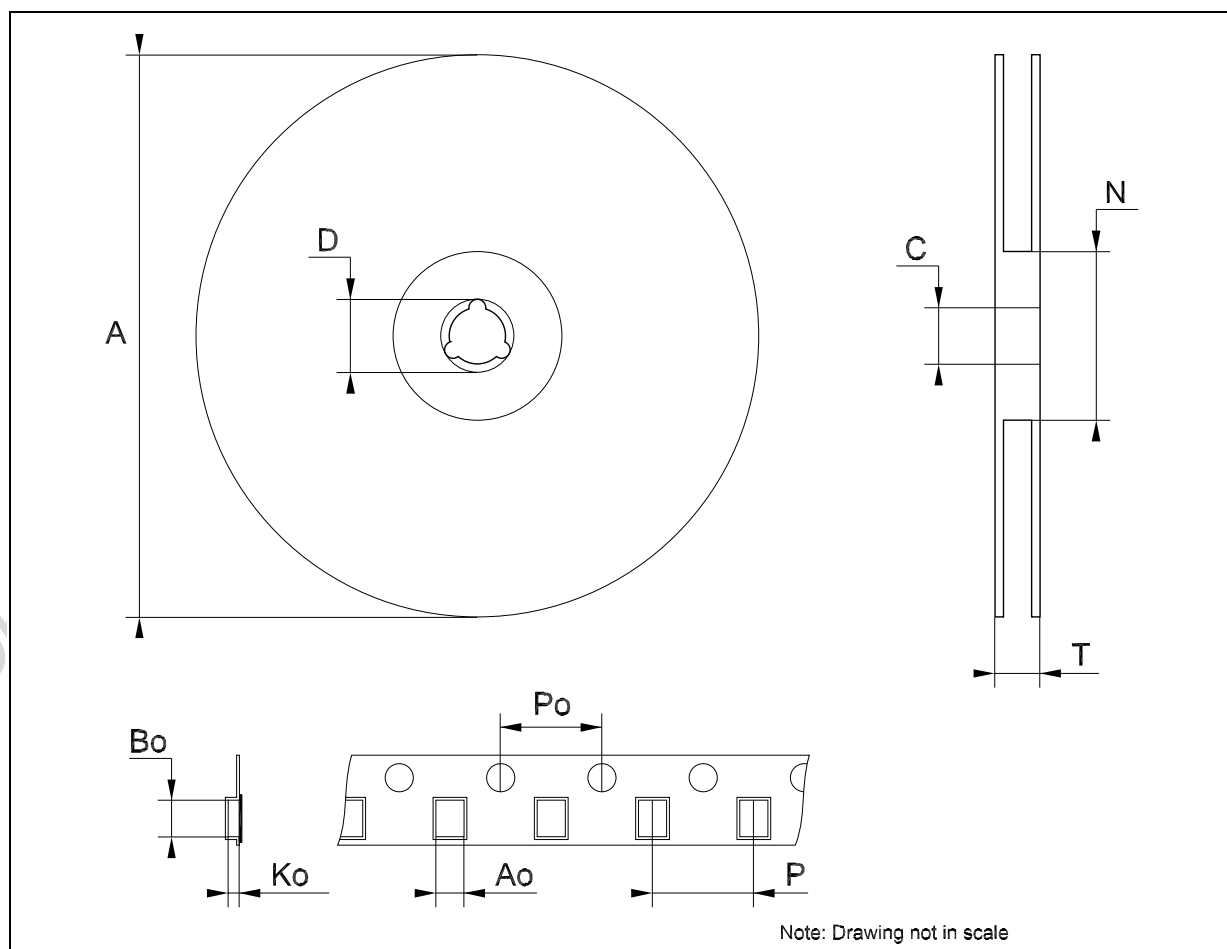


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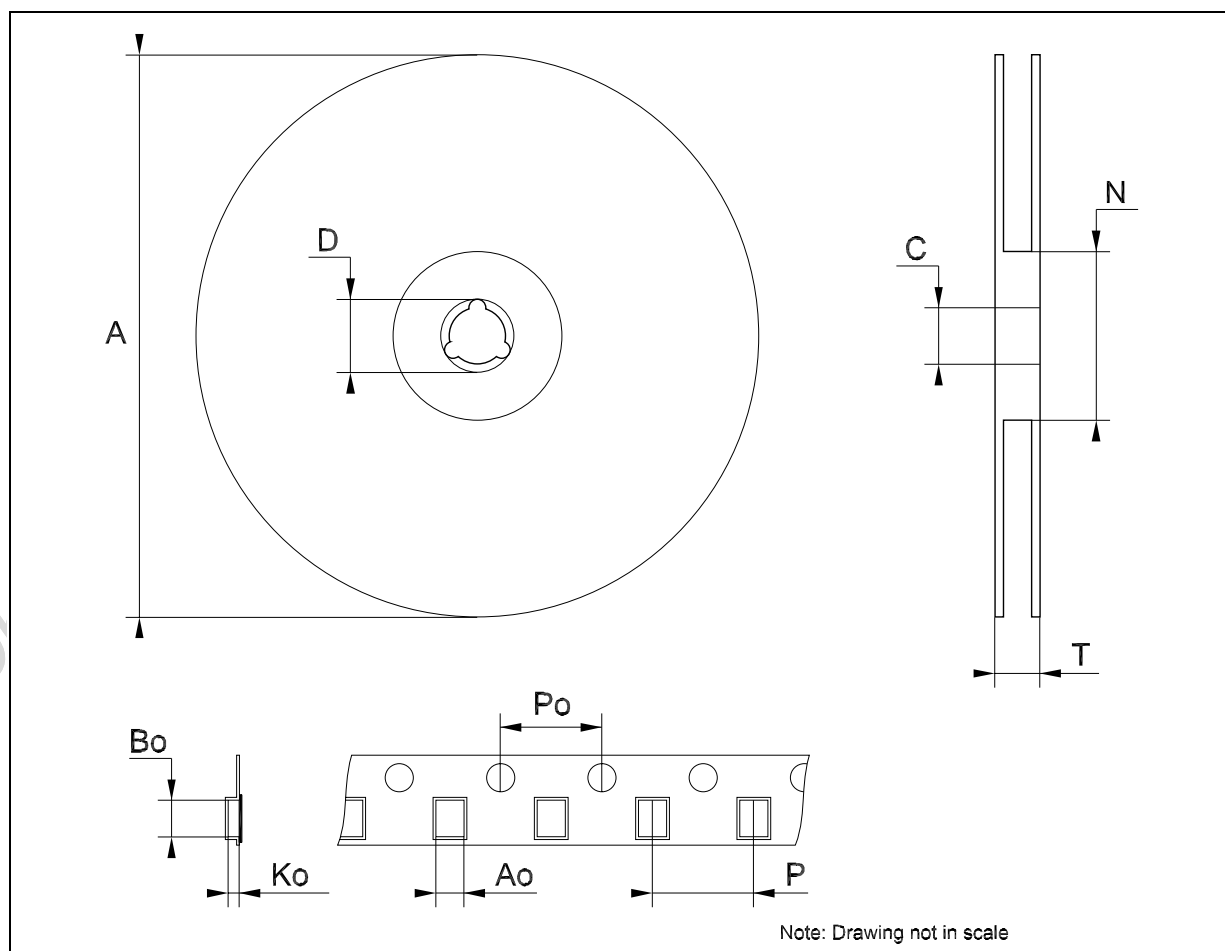
## Tape &amp; Reel SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



## Tape &amp; Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



**Table 9: Revision History**

Date	Revision	Description of Changes
16-Dec-2004	3	Order Codes Revision - pag. 1.

Obsolete Product(s) - Obsolete Product(s)

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