Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

  • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

To learn more, please visit www.rocelec.com

SN74LS109A

Dual JK Positive Edge-Triggered Flip-Flop

The SN74LS109A consists of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

ON Semiconductor™

http://onsemi.com

LOW POWER SCHOTTKY

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.
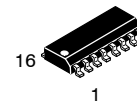
H, h = HIGH Voltage Level

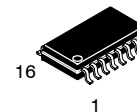L, l = LOW Voltage Level

X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input

(or output) one set-up time prior to the LOW to HIGH clock transition.

**PLASTIC
N SUFFIX
CASE 648**

**SOIC
D SUFFIX
CASE 751B**

**SOEIAJ
M SUFFIX
CASE 966**

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			– 0.4	mA
I_{OL}	Output Current – Low			8.0	mA

ORDERING INFORMATION

| Device	Package	Shipping
SN74LS109AN	16 Pin DIP	2000 Units/Box
SN74LS109AD	SOIC–16	38 Units/Rail
SN74LS109ADR2	SOIC–16	2500/Tape & Reel
SN74LS109AM	SOEIAJ–16	See Note 1
SN74LS109AMEL	SOEIAJ–16	See Note 1

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

SN74LS109A

LOGIC DIAGRAM

LOGIC SYMBOL

V_{CC} = PIN 16
GND = PIN 8
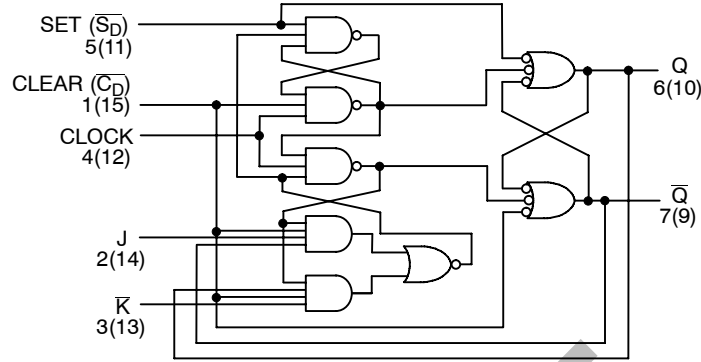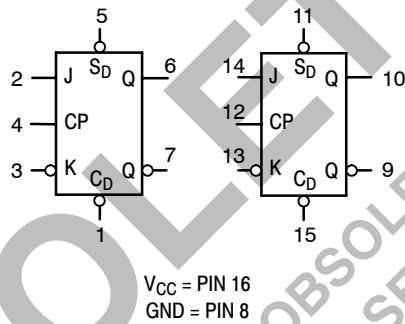
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current J, $\overline{K}$, Clock Set, Clear			20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	J, $\overline{K}$, Clock Set, Clear			0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current J, $\overline{K}$, Clock Set, Clear			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 1)	−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			8.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN74LS109A

AC CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	33		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13 25	25 40	ns ns	

AC SETUP REQUIREMENTS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock High Clear, Set Pulse Width	25			ns	$V_{CC} = 5.0$ V
t_s	Data Setup Time — HIGH LOW	20 20			ns ns	
t_h	Hold time	5.0			ns	

SN74LS109A

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R
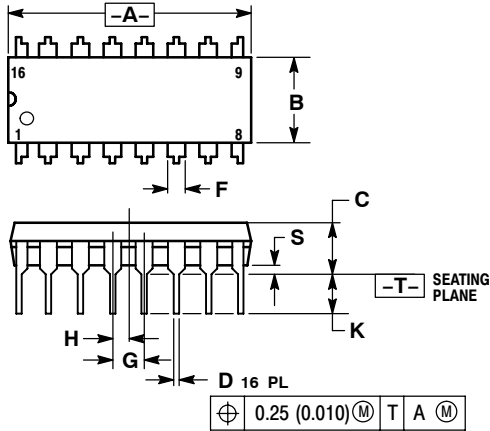
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
---	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
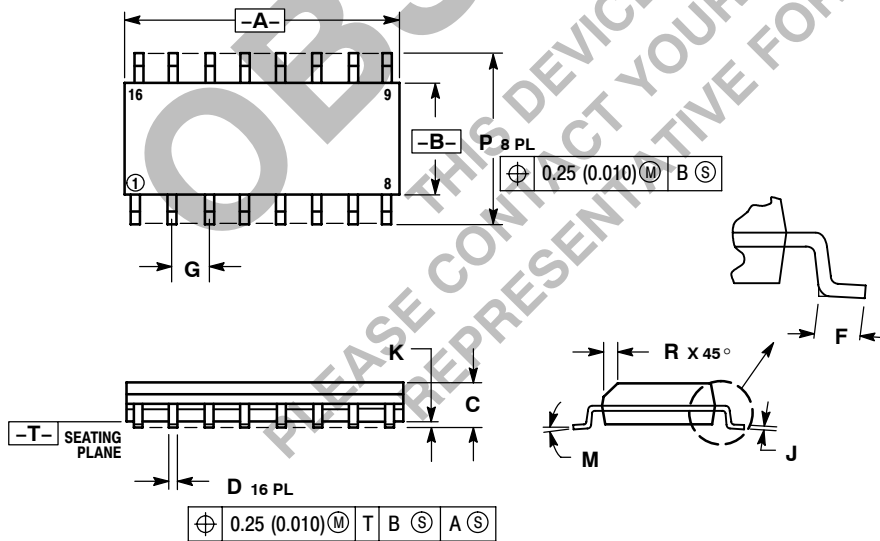
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
---	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SN74LS109A

PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 966–01
ISSUE O
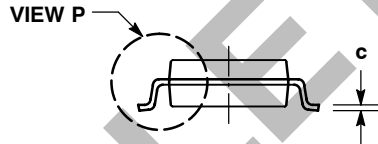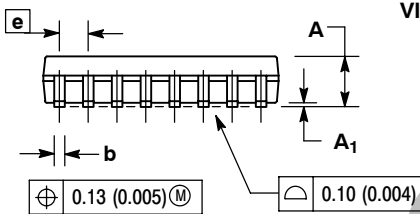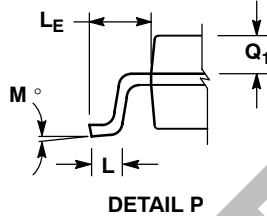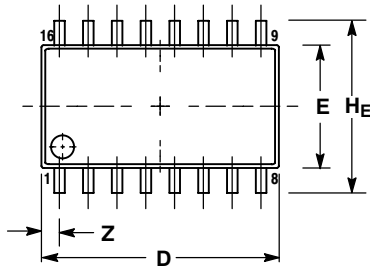
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	---	2.05	---	0.081
A$_1$	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H$_E$	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L$_E$	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q$_1$	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

SN74LS109A/D