

DM74ALS651/74ALS651-1

Octal TRI-STATE® Bus Transceiver and Register

General Description

This device incorporates an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high level logic drive provide this device with the capability of being connected directly to and driving the bus lines in a bus organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ALS651-1 version features the same performance as the standard version with the addition of increased current drive capability to meet the current requirements of various bus architectures. For all ALS-1 products, the recommended maximum I_{OL} is increased to 48 mA.

The registers in the 'ALS651 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

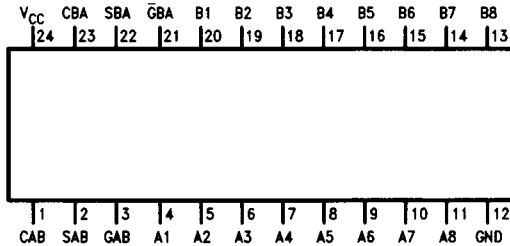
The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable (GAB and $\bar{G}BA$) control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Maximum I_{OL} increased to 48 mA for 'ALS651-1 product
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Independent registers and enables for A and B buses
- Multiplexed real-time and stored data

Connection Diagram



TL/F/10233-1

Order Number DM74ALS651NT, 74ALS651-1NT, DM74ALS651WM or 74ALS651-1WM
See NS Package Number M24B or N24C

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM74ALS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	44.5°C/W
M Package	80.5°C/W

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM74ALS651/74ALS651-1			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			-15	mA
I_{OL}	Low Level Output Current	ALS651		24	mA
		ALS651-1		48	mA
f_{CLK}	Clock Frequency	0		40	MHz
t_W	Pulse Duration, Clocks Low or High	12.5			ns
t_{SU}	Data Setup Time, A before CAB or B before CBA	10 \uparrow			ns
t_H	Data Hold Time, A after CAB or B after CBA	0 \uparrow			ns
T_A	Free Air Operating Temperature	0		70	°C

\uparrow = with reference to the low to high transition of the respective clock.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
V_{IK}	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5\text{V to }5.5\text{V}$	$I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		V	
		$V_{CC} = \text{Min}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		
			$I_{OH} = \text{Max}$	2			
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	V
			$I_{OL} = 24 \text{ mA}$		0.35	0.5	
			For 74ALS651-1 $I_{OL} = 48 \text{ mA}$		0.35	0.5	
I_I	Input Current at Max Input Voltage	$V_{CC} = \text{Max}$	I/O Ports, $V_I = 5.5\text{V}$		100	μA	
			Control Inputs, $V_I = 7\text{V}$		100		
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$, (Note 1)			20	μA	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$ (Note 1)	Control Inputs		-200	μA	
			I/O Ports		-200		
I_O	Output Drive Current	$V_{CC} = \text{Max}, V_O = 2.25\text{V}$	-30		-112	mA	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$	Outputs High		42	68	mA
			Outputs Low		52	82	
			Outputs Disabled		52	82	

Note 1: For I/O ports the TRI-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM74ALS651/ 74ALS651-1		Units
				Min	Max	
t _{PLH}	Propagation Delay Time Low to High Level Output	V _{CC} = 4.5V to 5.5V, C _L = 50 pF, R ₁ = R ₂ = 500Ω, T _A = Min to Max (Note 1)	CBA or CAB to A or B	10	32	ns
t _{PHL}	Propagation Delay Time High to Low Level Output		CBA or CAB21 to A or B	5	17	ns
t _{PLH}	Propagation Delay Time Low to High Level Output		A or B to B or A	4	18	ns
t _{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	2	10	ns
t _{PLH}	Propagation Delay Time Low to High Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	8	33	ns
t _{PHL}	Propagation Delay Time High to Low Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	7	21	ns
t _{PLH}	Propagation Delay Time Low to High Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	8	25	ns
t _{PHL}	Propagation Delay Time High to Low Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	7	21	ns
t _{PZH}	Output Enable Time to High Level Output		$\overline{\text{G}}\text{BA}$ to A	5	20	ns
t _{PZL}	Output Enable Time to Low Level Output		$\overline{\text{G}}\text{BA}$ to A	5	18	ns
t _{PHZ}	Output Disable Time from High Level Output		$\overline{\text{G}}\text{BA}$ to A	2	9	ns
t _{PLZ}	Output Disable Time from Low Level Output		$\overline{\text{G}}\text{BA}$ to A	3	12	ns
t _{PZH}	Output Enable Time to High Level Output		GAB to B	5	20	ns
t _{PZL}	Output Enable Time to Low Level Output		GAB to B	7	21	ns
t _{PHZ}	Output Disable Time from High Level Output		GAB to B	2	12	ns
t _{PLZ}	Output Disable Time from Low Level Output		GAB to B	2	14	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Function Table

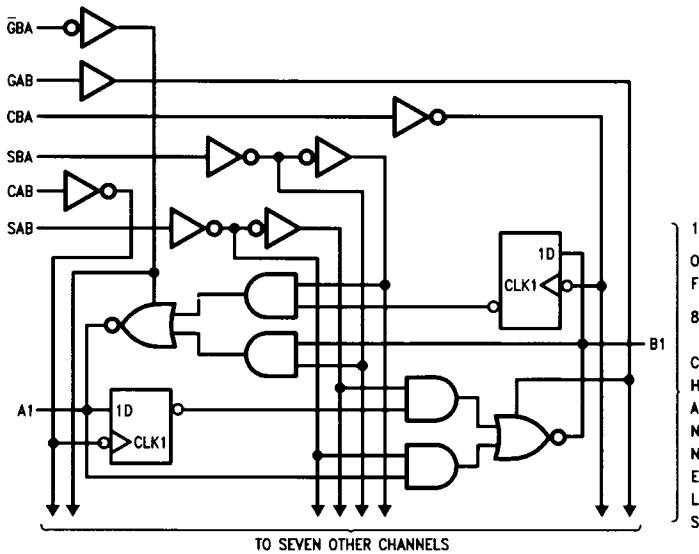
Inputs						Data I/O (Note 3)		Operation or Function
$\bar{G}AB$	GBA	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	H	↑	H/L	X	X	Input	Not Specified	Store A, Hold B
L	X	H/L	↑	X	X	Not Specified	Input	Store B, Hold A
L	H	↑	↑	X	X	Input	Input	Store A and B Data
L	H	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time \bar{B} Data to A Bus
L	L	X	H/L	X	H	Output	Input	Stored \bar{B} Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time \bar{A} Data to B Bus
H	H	H/L	X	H	X	Input	Output	Stored \bar{A} Data to B Bus
H	H	↑	↑	X (Note 4)	X	Input	Output	Store A in both Registers
L	L	↑	↑	X	X (Note 4)	Output	Input	Store B in both Registers
H	L	H/L	H/L	H	H	Output	Output	Stored \bar{A} Data to B Bus and Stored \bar{B} Data to A Bus

Note 3: The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Note 4: Select control = L; clocks can occur simultaneously
 Select control = H; clocks must be staggered in order to load both registers.

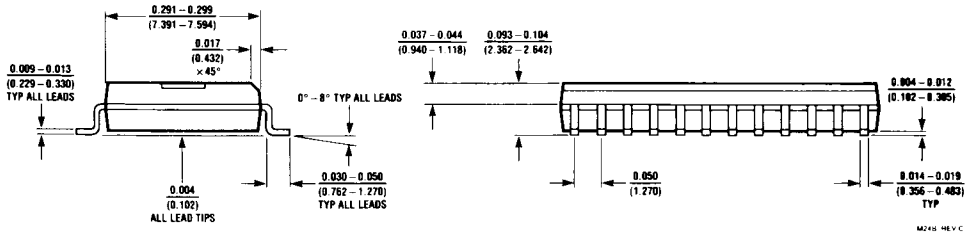
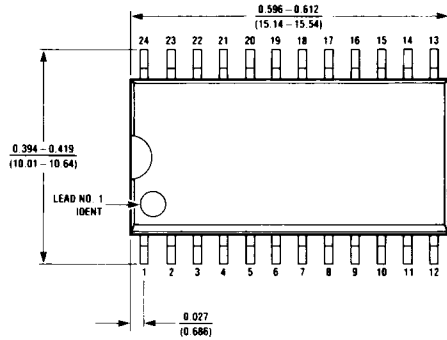
H = High Logic Level, L = Low Logic Level, X = Don't Care (Either Low or High Logic Levels, including transitions), H/L = Either Low or High Logic Level excluding transitions, ↑ = Positive-going edge of pulse.

Logic Diagram



TL/F/10233-2

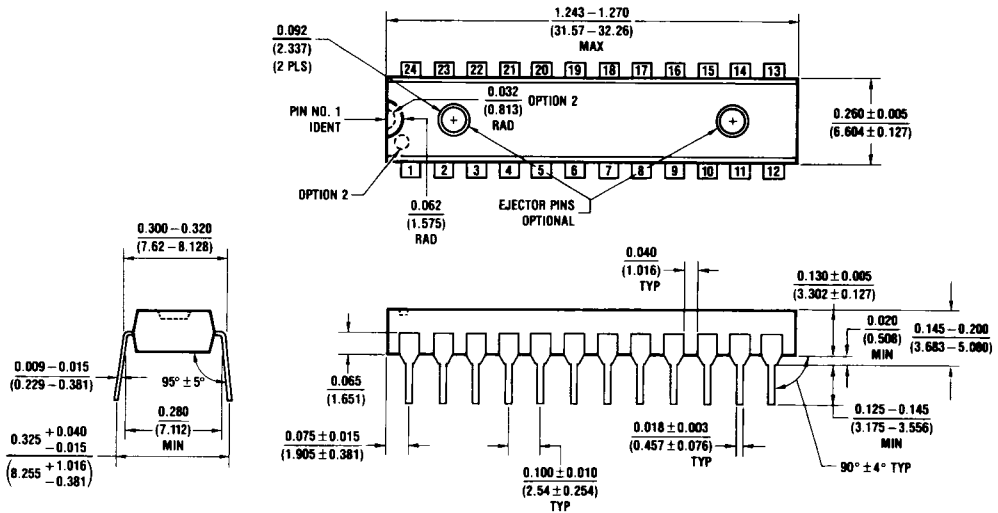
Physical Dimensions inches (millimeters)



S.O. Package (M)
Order Number DM74ALS651WM or 74ALS651-1WM
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 102575



N24C (REV F)

Molded Dual-In-Line Package (NT)
Order Number DM74ALS651NT or 74ALS651-1NT
NS Package Number N24C

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APR 06 1992



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