MOSEL VITELIC *MS6265*

8K x 8 SLOW SPEED CMOS STATIC RAM
ULTRA LOW DATA RETENTION CURRENT

Features

- Available in 100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS6265
  - 220mW (Max.) Operating
  - 5.5µW (Max.) Power Down
    16.6µW (Max.) Industrial Temp
  - 0.6µA (Max.) I_{CCDR}
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- 64K bit EPROM pin compatible
- Wide temperature range: -40 to + 85°C

Description

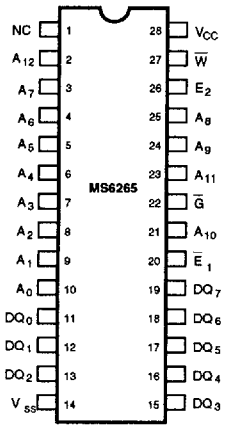
The MS6265 is a slow speed, very low data retention current, 64K bit static RAM, organized as 8192 x 8. The MS6265LL is designed to operate over industrial temperature range of -40°C to +85°C.

This SRAM is fully static in operation. Either of the chip enable controls ($\overline{E}1$ or E2) can be used to take the device to its low low data retention mode (I_{CCDR}).

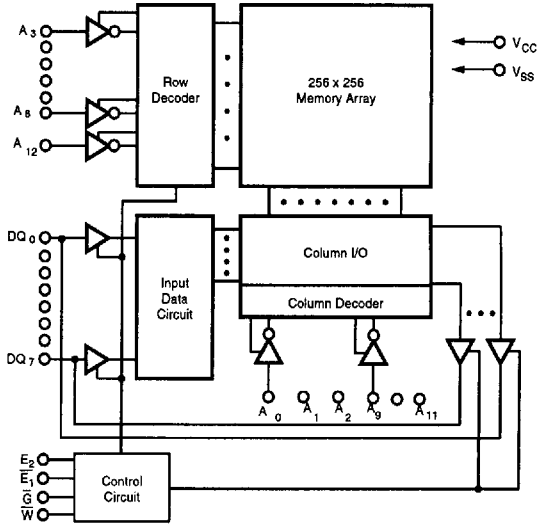
Write cycle occurs when chip enable $\overline{E}1$ is low, E2 is high, and write enable, $\overline{W}$, is low. Output enable control $\overline{G}$ has no control function in the write cycle.

Read Cycle occurs when chip enable $\overline{E}1$, is low, E2 is high, write enable $\overline{W}$ is high and output enable $\overline{G}$ is low.

Pin Configurations



Functional Block Diagram



Pin Descriptions

A_0 - A_{12} Address Inputs
These 13 address inputs select one of the 8192 X 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
$\overline{E}_2$ Chip Enable 2 Input
E_1 is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected (in a standby power mode). The DQ pins are in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. With the output enable active and the chip selected and write enable inactive, read data will be present on the DQ pins. The DQ pins will be in the high impedance (three state) output mode when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, $\overline{W}$ is HIGH and $\overline{G}$ LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

Vss Ground

TruthTable

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_N	Input Voltage		-0.3 to Vcc + 0.3	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-55 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		±40 (2)	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability and degrade performance characteristics.
2. Output should not be shorted for more than 30 seconds.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Special Commercial	-10°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Capacitance (1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_N = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

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DC Electrical Characteristics (over the operating range)

Parameter Name	Parameter	Test Conditions	MS6265 Min.	Typ. (1)	Max	Units
V_{IL}	Guaranteed Input Low Voltage (2)		−0.3	-	0.8	V
V_H	Guaranteed Input High Voltage (2)		2.2	-	Vcc + 0.3	V
I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CC}, $E_2 \geq$ Vcc - 0.2V, $\overline{E}_1 \leq 0.2V$	-	-	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_H$, V_N = 0V t o V_{CC}	-	-	1	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = −4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$ (3)	-	-	40	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	10	µA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ − 0.2V, $E_2 \leq 0.2$ $T_A \leq 70°C$	-	-	1	µA
		$V_N \geq$ VCC -0.2V OR $V_N \leq 0.2V$ $T_A \leq 85°C$	-	-	3	µA

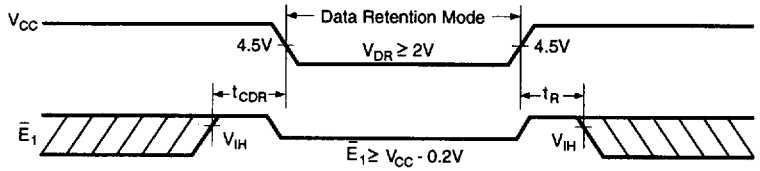
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention Characteristics (over the specified operating range)

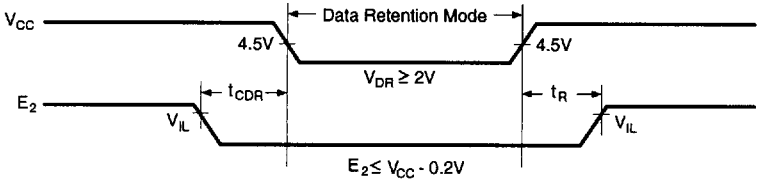
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ − 0.2V, $E_2 \leq 0.2V$, $V_N \geq V_{CC}$ − 0.2V or $V_N \leq 0.2V$		2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{DR}$ − 0.2V, $E_2 \leq 0.2V$, $V_N \geq V_{DR}$ − 0.2V or $V_N \leq 0.2V$	$T_A \leq 70°C$	-	-	0.6	µA(1)
			$T_A \leq 85°C$			2.0	µA(1)
I_{IL}	Input Leakage Current			-	-	2	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform		0	-	-	ns
t_R	Operation Recovery Time			t_{RC} (2)	-	-	ns

1. V_{DR} = 3V, T_A = Specified
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{E}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) ($\overline{E}_2$ Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

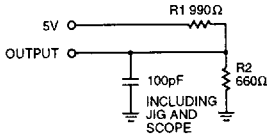


Figure 1a

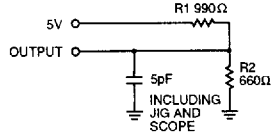


Figure 1b

Equivalent to:

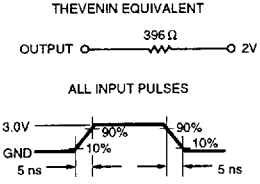


Figure 2

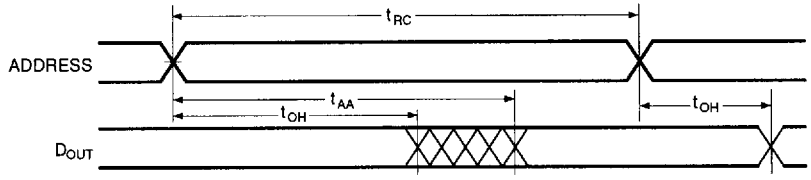
AC Electrical Characteristics (over the operating range)

Read Cycle

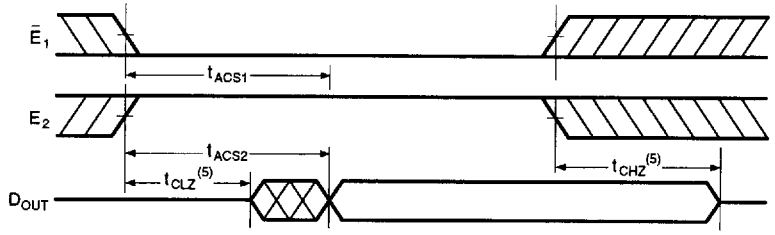
JEDEC Parameter Name	Parameter Name	Parameter	MS6265-10 Min.	MS6265-10 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	100	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	100	ns
t_{ELQV}	t_{ACS1}	Chip Enable Access Time	-	100	ns
t_{ELQV}	t_{ACS2}	Chip Enable Access Time	-	100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	40	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	10	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	30	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	20	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10	-	ns

Switching Waveforms (Read Cycle)

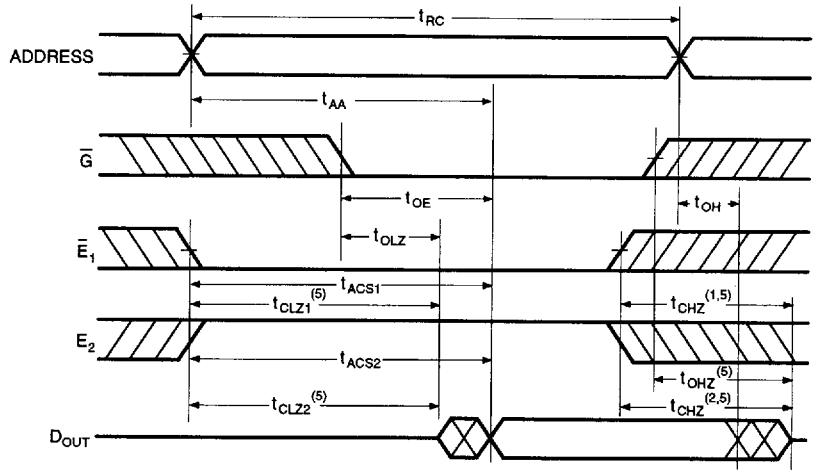
READ CYCLE 1(1,2,4)



READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

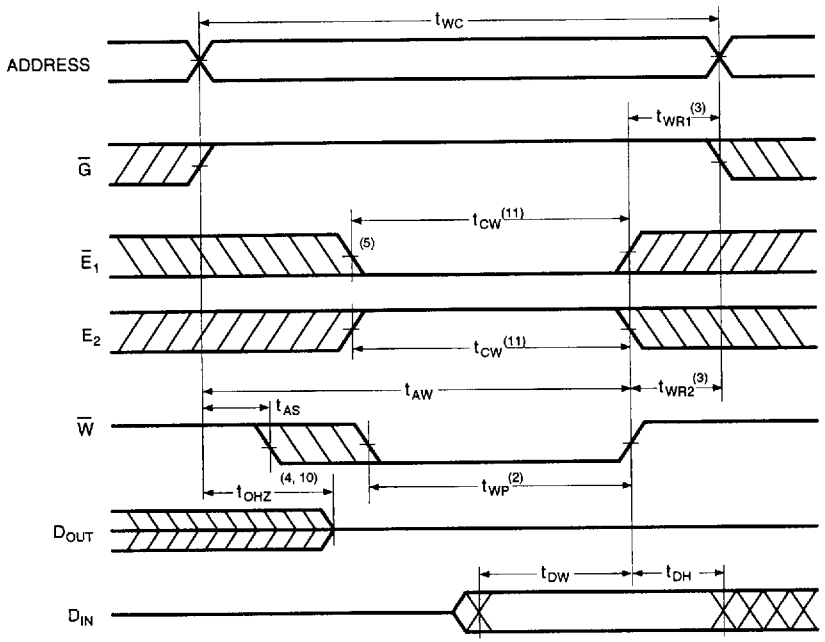
AC Electrical Characteristics (over the operating range)

Write Cycle

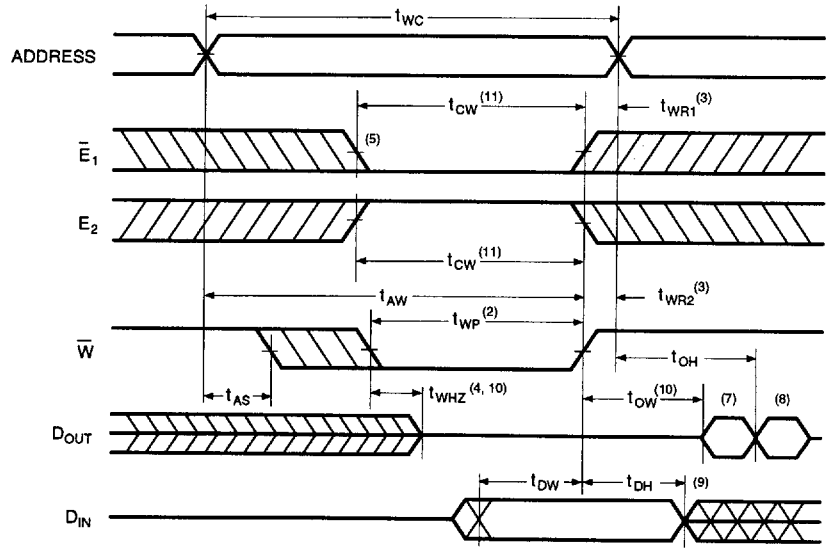
JEDEC Parameter Name	Parameter Name	Parameter	MS6265-10 Min.	MS6265-10 Max.	Unit
t_{AVAX}	t_{WC}	Write Cycle Time	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	90	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	20	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	90	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	60	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	10	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	50	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	10	-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1(1)



WRITE CYCLE 2[1,6]



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

Ordering Information

Speed (ns)	Ordering Part Number	Package	Temperature Range
100	MS6265-10NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
100	MS6265-10FC	28 Pin 330 mil Small Outline	0°C to +70°C
100	MS6265-10PC	28 Pin 600 mil Plastic DIP	0°C to +70°C
100	MS6265-10PI	28 Pin 600 mil Plastic DIP	-40°C to + 85°C
100	MS6265-10FI	20 Pin 330 mil Small Outline	-40°C to + 85°C
100	MS6265-10NI	28 Pin 300 mil Plastic DIP	-40°C to + 85°C