# DSP56304

## *Advance Information*
## 24-BIT DIGITAL SIGNAL PROCESSOR

Motorola designed the ROM-based DSP56304 to support multifunction wireless and embedded DSP applications. In addition to the large on-chip ROM spaces, the DSP56304 also has a ROM patch feature that facilitates updates to the on-chip mask Program ROM-based on-chip software. The DSP56304 includes a triple timer module, Host Interface (HI08), an Enhanced Synchronous Serial Interface (ESSI), and a Serial Communications Interface (SCI). The DSP56300 core family includes a Phase Lock Loop (PLL), External Memory Interface (EMI), Data Arithmetic Logic Unit (Data ALU), 24-bit addressing, instruction cache, and DMA. The DSP56304 offers 66/80 MIPS using an internal 66/80 MHz clock at 3.0–3.6 volts.
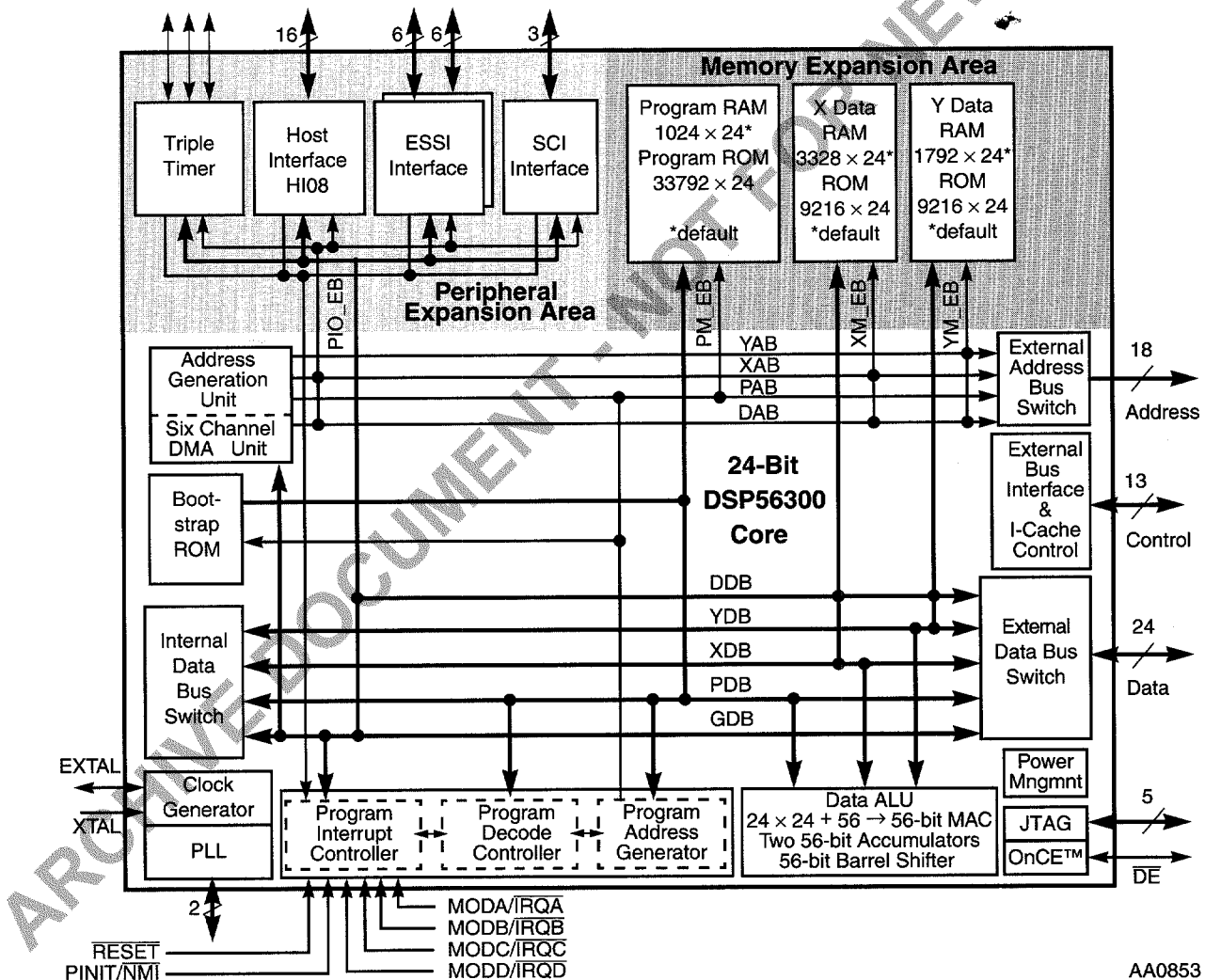


**Figure 1** DSP56304 Block Diagram

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**MOTOROLA**

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## Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$   Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)

"asserted"   Means that a high true (active high) signal is high or that a low true (active low) signal is low

"deasserted"   Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

| Signal/Symbol | Logic State | Signal State | Voltage |
|---|---|---|---|
| $\overline{\text{PIN}}$ | True | Asserted | $V_{IL}/V_{OL}$ |
| $\overline{\text{PIN}}$ | False | Deasserted | $V_{IH}/V_{OH}$ |
| PIN | True | Asserted | $V_{IH}/V_{OH}$ |
| PIN | False | Deasserted | $V_{IL}/V_{OL}$ |

Note:    Values for $V_{IL}$, $V_{OL}$, $V_{IH}$, and $V_{OH}$ are defined by individual product specifications.

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# FEATURES

## DSP56304 FEATURES

## High Performance DSP56300 Core

- 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC)
- 56-bit parallel barrel shifter
- 24-bit or 16-bit arithmetic support under software control
- Position independent code support
- Addressing modes optimized for DSP applications
- On-chip instruction cache controller
- On-chip memory-expandable hardware stack
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip concurrent six-channel DMA controller
- On-chip Phase Lock Loop (PLL) and clock generator
- On-Chip Emulation (OnCE™) module
- JTAG Test Access Port (TAP)
- Address Tracing mode reflects internal accesses at the external port

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## On-chip Memories

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable:

| Instruction Cache | Switch Mode | Program RAM Size | Instruction Cache Size | X Data RAM Size | Y Data RAM Size |
|---|---|---|---|---|---|
| disabled | disabled | 1024 × 24-bit | 0 | 3328 × 24-bit | 1792 × 24-bit |
| enabled | disabled | 0 | 1024 × 24-bit | 3328 × 24-bit | 1792 × 24-bit |
| disabled | enabled | 3584 × 24-bit | 0 | 2048 × 24-bit | 512 × 24-bit |
| enabled | enabled | 2560 × 24-bit | 1024 × 24-bit | 2048 × 24-bit | 512 × 24-bit |

- 33, 792 × 24-bit Program ROM with Patch mode update capability using instruction cache memory space

- 9,216 × 24-bit X data ROM and 9,216 × 24-bit Y data ROM

- 192 × 24-bit bootstrap ROM

## Off-chip Memory Expansion

- Data memory expansion to two 256 K × 24-bit word memory spaces (the usage of address attribute pins and/or DRAM interface may further extend the data memory expansion up to two 16 M × 24-bit words memory space)

- Program memory expansion to one 256 K × 24-bit word memory space (the usage of address attribute pins and/or DRAM interface may further extend the program memory expansion up to two 16 M × 24-bit words memory space)

- External memory expansion port

- Chip select logic requires no additional circuitry to interface to SRAMs and SSRAMs

- On-chip DRAM controller requires no additional circuitry to interface to DRAMs

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## On-chip Peripherals

- 8-bit parallel Host Interface (HI08), ISA-compatible bus interface, providing a cost-effective solution for applications not requiring the PCI bus

- Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)

- Serial Communications Interface (SCI) with baud rate generator

- Triple timer module

- Up to thirty-four programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled

## Reduced Power Dissipation

- Very low power CMOS design

- Wait and Stop low power standby modes

- Fully-static logic, operation frequency down to DC

- Optimized power management circuitry

## TARGET APPLICATIONS

The DSP56304 is intended for use in embedded multifunction DSP applications requiring large on-board ROM spaces, such as wireless products that combine standard cellular phone operation with options such as two-way digital paging and fax capability in one unit.

# PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56304 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

**Table 1** DSP56304 Documentation

| Document Name | Description of Contents | Order Number |
|---|---|---|
| DSP56300 Family Manual | Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set | DSP56300FM/AD |
| DSP56304 User's Manual | Detailed description of DSP56304 memory, peripherals, and interfaces | DSP56304UM/AD |
| DSP56304 Technical Data | DSP56304 pin and package descriptions, and electrical and timing specifications | DSP56304/D |

# SECTION 1

# SIGNAL/CONNECTION DESCRIPTIONS

## SIGNAL GROUPINGS

The input and output signals of the DSP56304 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**.

The DSP56304 is operated from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.
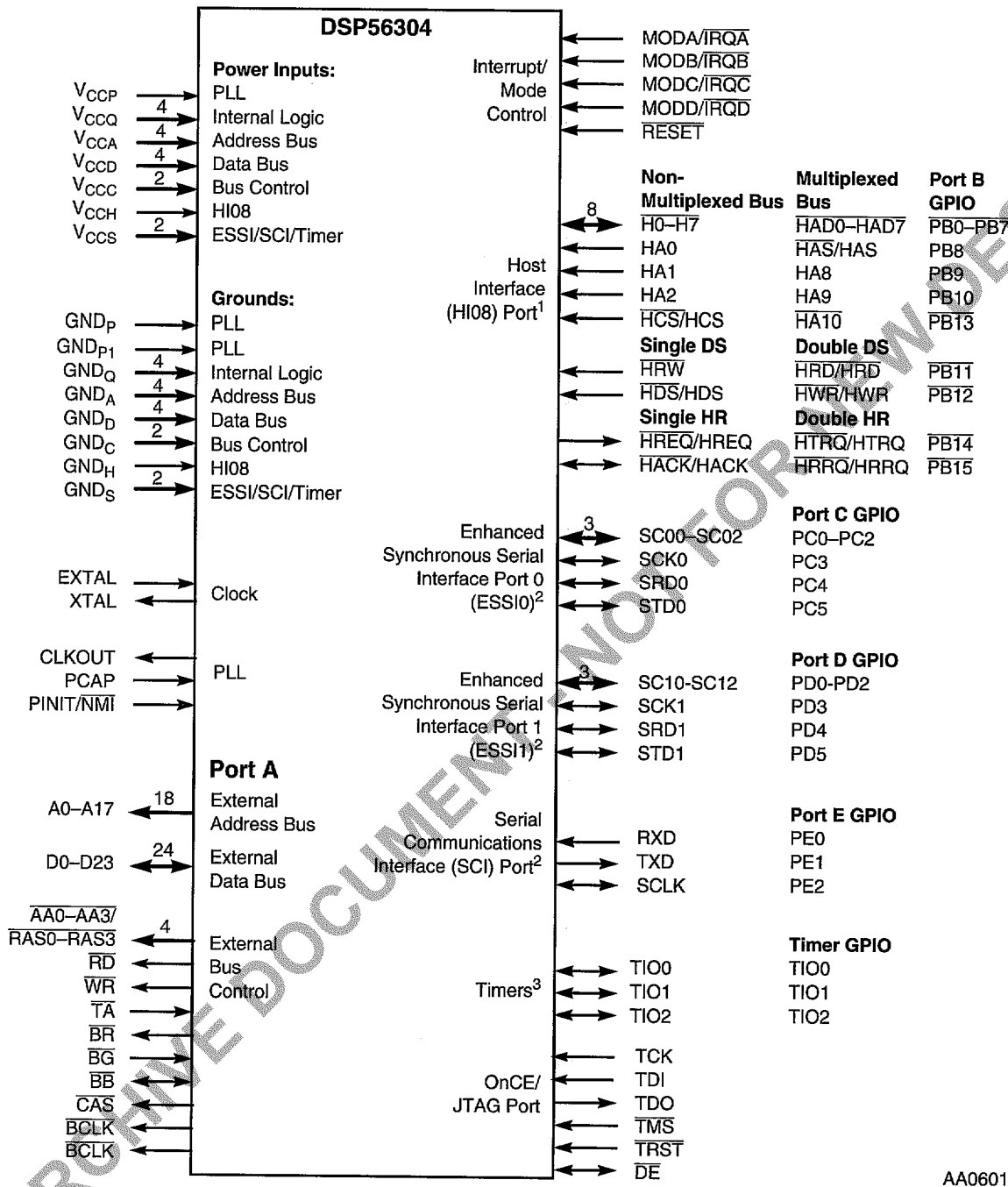
**Table 1-1** DSP56304 Functional Signal Groupings

| Functional Group | | Number of Signals | Detailed Description |
|---|---|---|---|
| Power ($V_{CC}$) | | 18 | **Table 1-2** |
| Ground (GND) | | 19 | **Table 1-3** |
| Clock | | 2 | **Table 1-4** |
| PLL | | 3 | **Table 1-5** |
| Address Bus | Port A[1] | 18 | **Table 1-6** |
| Data Bus | | 24 | **Table 1-7** |
| Bus Control | | 13 | **Table 1-8** |
| Interrupt and Mode Control | | 5 | **Table 1-9** |
| Host Interface (HI08) | Port B[2] | 16 | **Table 1-11** |
| Enhanced Synchronous Serial Interface (ESSI) | Ports C and D[3] | 12 | **Table 1-12 and Table 1-13** |
| Serial Communication Interface (SCI) | Port E[4] | 3 | **Table 1-14** |
| Timer | | 3 | **Table 1-15** |
| OnCE/JTAG Port | | 6 | **Table 1-16** |
| Note: 1. Port A signals define the External Memory Interface port, including the external address bus, data bus, and control signals. 2. Port B signals are the HI08 port signals multiplexed with the GPIO signals. 3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals. 4. Port E signals are the SCI port signals multiplexed with the GPIO signals. | | | |

**Figure 1-1** is a diagram of DSP56304 signals by functional group.

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**DSP56304**

**Power Inputs:**
$V_{CCP}$ — PLL — 4
$V_{CCQ}$ — Internal Logic — 4
$V_{CCA}$ — Address Bus — 4
$V_{CCD}$ — Data Bus — 2
$V_{CCC}$ — Bus Control
$V_{CCH}$ — HI08 — 2
$V_{CCS}$ — ESSI/SCI/Timer

**Grounds:**
$GND_P$ — PLL
$GND_{P1}$ — PLL — 4
$GND_Q$ — Internal Logic — 4
$GND_A$ — Address Bus — 4
$GND_D$ — Data Bus — 2
$GND_C$ — Bus Control
$GND_H$ — HI08 — 2
$GND_S$ — ESSI/SCI/Timer

EXTAL — Clock — XTAL

CLKOUT — PLL
PCAP
PINIT/$\overline{NMI}$

**Port A**

A0–A17 — 18 — External Address Bus

D0–D23 — 24 — External Data Bus

$\overline{AA0}$–$\overline{AA3}$/ $\overline{RAS0}$–$\overline{RAS3}$ — 4 — External Bus Control
$\overline{RD}$
$\overline{WR}$
$\overline{TA}$
$\overline{BR}$
$\overline{BG}$
$\overline{BB}$
$\overline{CAS}$
$\overline{BCLK}$
$\overline{BCLK}$

Interrupt/ Mode Control:
MODA/$\overline{IRQA}$
MODB/$\overline{IRQB}$
MODC/$\overline{IRQC}$
MODD/$\overline{IRQD}$
$\overline{RESET}$

Host Interface (HI08) Port[1]

| Non-Multiplexed Bus | Multiplexed Bus | Port B GPIO |
|---|---|---|
| H0–H7 (8) | HAD0–HAD7 | PB0–PB7 |
| HA0 | $\overline{HAS}$/HAS | PB8 |
| HA1 | HA8 | PB9 |
| HA2 | HA9 | PB10 |
| $\overline{HCS}$/HCS | HA10 | PB13 |
| **Single DS** | **Double DS** | |
| HRW | $\overline{HRD}$/HRD | PB11 |
| $\overline{HDS}$/HDS | $\overline{HWR}$/HWR | PB12 |
| **Single HR** | **Double HR** | |
| $\overline{HREQ}$/HREQ | $\overline{HTRQ}$/HTRQ | PB14 |
| $\overline{HACK}$/HACK | $\overline{HRRQ}$/HRRQ | PB15 |

Enhanced Synchronous Serial Interface Port 0 (ESSI0)[2]:
SC00–SC02 (3) — Port C GPIO: PC0–PC2
SCK0 — PC3
SRD0 — PC4
STD0 — PC5

Enhanced Synchronous Serial Interface Port 1 (ESSI1)[2]:
SC10–SC12 (3) — Port D GPIO: PD0–PD2
SCK1 — PD3
SRD1 — PD4
STD1 — PD5

Serial Communications Interface (SCI) Port[2]:
RXD — Port E GPIO: PE0
TXD — PE1
SCLK — PE2

Timers[3]:
TIO0 — Timer GPIO: TIO0
TIO1 — TIO1
TIO2 — TIO2

OnCE/ JTAG Port:
TCK
TDI
TDO
TMS
$\overline{TRST}$
$\overline{DE}$

AA0601

Note:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternately as GPIO signals (PB0–PB15). Signals with dual designations (e.g., $\overline{HAS}$/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC0–PC5), Port D GPIO signals (PD0–PD5), and Port E GPIO signals (PE0–PE2), respectively.
3. TIO0–TIO2 can be configured as GPIO signals.

**Figure 1-1** Signals Identified by Functional Group

**Preliminary Data**

# POWER

Table 1-2  Power Inputs

| Power Name | Description |
|---|---|
| $V_{CCP}$ | **PLL Power**—$V_{CCP}$ is $V_{CC}$ dedicated for Phase Lock Loop (PLL) use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the $V_{CC}$ power rail. There is one $V_{CCP}$ input. |
| $V_{CCQ}$ (4) | **Quiet Power**—$V_{CCQ}$ is an isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four $V_{CCQ}$ inputs. |
| $V_{CCA}$ (4) | **Address Bus Power**—$V_{CCA}$ is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four $V_{CCA}$ inputs. |
| $V_{CCD}$ (4) | **Data Bus Power**—$V_{CCD}$ is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four $V_{CCD}$ inputs. |
| $V_{CCC}$ (2) | **Bus Control Power**—$V_{CCC}$ is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two $V_{CCC}$ inputs. |
| $V_{CCH}$ | **Host Power**—$V_{CCH}$ is an isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one $V_{CCH}$ input. |
| $V_{CCS}$ (2) | **ESSI, SCI, and Timer Power**—$V_{CCS}$ is an isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two $V_{CCS}$ inputs. |
| Note: | These designations are package-dependent. Some packages connect all $V_{CC}$ inputs except $V_{CCP}$ to each other internally. On those packages, all power input, except $V_{CCP}$, are labeled $V_{CC}$. The numbers of connections indicated in this table are minimum values; the total $V_{CC}$ connections are package-dependent. |

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# GROUND

Table 1-3   Grounds

| Ground Name | Description |
|---|---|
| $GND_P$ | **PLL Ground**—$GND_P$ is ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. $V_{CCP}$ should be bypassed to $GND_P$ by a 0.47 µF capacitor located as close as possible to the chip package. There is one $GND_P$ connection. |
| $GND_{P1}$ | **PLL Ground 1**—$GND_{P1}$ is ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. There is one $GND_{P1}$ connection. |
| $GND_Q$ (4) | **Quiet Ground**—$GND_Q$ is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four $GND_Q$ connections. |
| $GND_A$ (4) | **Address Bus Ground**—$GND_A$ is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four $GND_A$ connections. |
| $GND_D$ (4) | **Data Bus Ground**—$GND_D$ is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four $GND_D$ connections. |
| $GND_C$ (2) | **Bus Control Ground**—$GND_C$ is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two $GND_C$ connections. |
| $GND_H$ | **Host Ground**—$GND_H$ is an isolated ground for the HI08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one $GND_H$ connection. |
| $GND_S$ (2) | **ESSI, SCI, and Timer Ground**—$GND_S$ is an isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two $GND_S$ connections. |
| Note: | These designations are package-dependent. Some packages connect all GND inputs, except $GND_P$ and $GND_{P1}$, to each other internally. On those packages, all ground connections, except $GND_P$ and $GND_{P1}$, are labeled GND. The numbers of connections indicated in this table are minimum values; the total GND connections are package-dependent. |

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# CLOCK

Table 1-4  Clock Signals

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| EXTAL | Input | Input | **External Clock/Crystal Input**—EXTAL interfaces the internal crystal oscillator input to an external crystal or an external clock. |
| XTAL | Output | Chip Driven | **Crystal Output**—XTAL connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected. |

# PHASE LOCK LOOP (PLL)

Table 1-5  Phase Lock Loop Signals

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| PCAP | Input | Input | **PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to $V_{CCP}$. <br><br> If the PLL is not used, PCAP may be tied to $V_{CC}$, GND, or left floating. |
| CLKOUT | Output | Chip-driven | **Clock Output**—CLKOUT provides an output clock synchronized to the internal core clock phase. <br><br> If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. <br><br> If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL. |

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**Table 1-5** Phase Lock Loop Signals (Continued)

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| PINIT/ $\overline{\text{NMI}}$ | Input | Input | **PLL Initial/Non-Maskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT. PINIT/$\overline{\text{NMI}}$ can tolerate 5 V. |

# EXTERNAL MEMORY EXPANSION PORT (PORT A)

**Note:** When the DSP56304 enters a low-power standby mode (Stop or Wait), it releases bus mastership and tri-states the relevant Port A signals: A0–A17, D0–D23, AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$, BCLK, $\overline{\text{BCLK}}$.

**Note:** If the hardware refresh of external DRAM is enabled, the Port A pins exit Wait state to perform the refresh, and then return to the Wait state again.

## EXTERNAL ADDRESS BUS

**Table 1-6** External Address Bus Signals

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|---|---|---|---|
| A0–A17 | Output | Tri-stated | **Address Bus**—When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed. |

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## EXTERNAL DATA BUS

Table 1-7  External Data Bus Signals

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|---|---|---|---|
| D0–D23 | Input/ Output | Tri-stated | **Data Bus**—When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated. |

## EXTERNAL BUS CONTROL

Table 1-8  External Bus Control Signals

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|---|---|---|---|
| AA0– AA3/ $\overline{\text{RAS0}}$– $\overline{\text{RAS3}}$ | Output | Tri-stated | **Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for Dynamic Random Access Memory (DRAM) interface. These signals are tri-statable outputs with programmable polarity. |
| $\overline{\text{RD}}$ | Output | Tri-stated | **Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D0–D23). Otherwise, $\overline{\text{RD}}$ is tri-stated. |
| $\overline{\text{WR}}$ | Output | Tri-stated | **Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D0–D23). Otherwise, the signals are tri-stated. |

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Table 1-8  External Bus Control Signals (Continued)

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|---|---|---|---|
| $\overline{TA}$ | Input | Ignored Input | **Transfer Acknowledge**—If the DSP56304 is the bus master and there is no external bus activity, or the DSP56304 is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a Data Transfer Acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2,..., infinity) may be added to the wait states inserted by the BCR by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{TA}$ input or by the Bus Control Register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles.<br><br>In order to use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access can not be extended by $\overline{TA}$ deassertion, otherwise improper operation may result. $\overline{TA}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register (OMR).<br><br>$\overline{TA}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result. |
| $\overline{BR}$ | Output | Output (driven high/deasserted) | **Bus Request**—$\overline{BR}$ is an active-low output, never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56304 is a bus master or a bus slave. Bus "parking" allows $\overline{BR}$ to be deasserted even though the DSP56304 is the bus master (see the description of bus "parking" in the $\overline{BB}$ signal description). The Bus Request Hole (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state. |

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Table 1-8  External Bus Control Signals (Continued)

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|---|---|---|---|
| $\overline{BG}$ | Input | Ignored Input | **Bus Grant**—$\overline{BG}$ is an active-low input. $\overline{BG}$ must be asserted/deasserted synchronous to CLKOUT for proper operation. $\overline{BG}$ is asserted by an external bus arbitration circuit when the DSP56304 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56304 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. |
| $\overline{BB}$ | Input/ Output | Input | **Bus Busy**—$\overline{BB}$ is a bidirectional active-low input/output and must be asserted and deasserted synchronous to CLKOUT. $\overline{BB}$ indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. This is called "bus parking" and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. The deassertion of $\overline{BB}$ is done by an "active pull-up" method (i.e., $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). $\overline{BB}$ requires an external pull-up resistor. |
| $\overline{CAS}$ | Output | Tri-stated | **Column Address Strobe**—When the DSP is the bus master, $\overline{CAS}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM Control Register is cleared, the signal is tri-stated. |
| BCLK | Output | Tri-stated | **Bus Clock**—When the DSP is the bus master, BCLK is an active-high output used by Synchronous Static Random Access Memory (SSRAM) to sample address, data, and control signals. BCLK is active either during SSRAM accesses or as a sampling signal when the program Address Tracing mode is enabled (by setting the ATE bit in the OMR). When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle. The BCLK rising edge may be used to sample the internal program memory access on the A0–A23 address lines. |
| $\overline{BCLK}$ | Output | Tri-stated | **Bus Clock Not**—When the DSP is the bus master, $\overline{BCLK}$ is an active-low output and is the inverse of the BCLK signal. Otherwise, the signal is tri-stated. |

**Preliminary Data**

# INTERRUPT AND MODE CONTROL

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

**Table 1-9**  Interrupt and Mode Control

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| $\overline{\text{RESET}}$ | Input | Input | **Reset**—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. Deassertion of $\overline{\text{RESET}}$ is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If $\overline{\text{RESET}}$ is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in "lock-step". When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after power up. $\overline{\text{RESET}}$ can tolerate 5 V. |
| MODA/$\overline{\text{IRQA}}$ | Input | Input | **Mode Select A/External Interrupt Request A**—MODA/$\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODA/$\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQA}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state. MODA/$\overline{\text{IRQA}}$ can tolerate 5 V. |

**Preliminary Data**

Table 1-9  Interrupt and Mode Control (Continued)

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| MODB/$\overline{\text{IRQB}}$ | Input | Input | **Mode Select B/External Interrupt Request B**—MODB/$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODB/$\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQB}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the Wait state.<br><br>MODB/$\overline{\text{IRQB}}$ can tolerate 5 V. |
| MODC/$\overline{\text{IRQC}}$ | Input | Input | **Mode Select C/External Interrupt Request C**—MODC/$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODC/$\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQC}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the Wait state.<br><br>MODC/$\overline{\text{IRQC}}$ can tolerate 5 V. |
| MODD/$\overline{\text{IRQD}}$ | Input | Input | **Mode Select D/External Interrupt Request D**—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to CLKOUT. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQD}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQD}}$ to exit the Wait state.<br><br>MODD/$\overline{\text{IRQD}}$ can tolerate 5 V. |

**Preliminary Data**

# HOST INTERFACE (HI08)

The HI08 provides a fast parallel data to 8-bit port, which may be connected directly to the host bus.

The HI08 supports a variety of standard buses, and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

## Host Port Usage Considerations

Careful synchronization is required when reading multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in the following table:

**Table 1-10**   Host Port Usage Considerations

| Action | Description |
|---|---|
| Asynchronous read of receive byte registers | When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag which indicates that data is available. This assures that the data in the receive byte registers will be valid. |
| Asynchronous write to transmit byte registers | The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the Host Receive (HRX) register. |
| Asynchronous write to host vector | The host interface programmer should change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This will guarantee that the DSP interrupt control logic will receive a stable vector. |

## Host Port Configuration

The functions of the signals associated with the HI08 vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register (HPCR). Refer to the *DSP56304 User's Manual* for detailed descriptions of this and the other configuration registers used with the HI08.

**Table 1-11** Host Interface

| Signal Name | Type | State During Reset or Stop[1] | Signal Description |
|---|---|---|---|
| H0–H7 | Input/Output | Disconnected | **Host Data**—When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Data bidirectional, tri-state bus. |
| HAD0–HAD7 | Input/Output | | **Host Address**—When HI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Address/Data bidirectional, multiplexed, tri-state bus. |
| PB0–PB7 | Input or Output | | **Port B 0–7**—When the HI08 is configured as GPIO through the HPCR, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register (HDDR).<br><br>This input is 5 V tolerant. |
| HA0 | Input | Disconnected | **Host Address Input 0**—When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 0 of the Host Address input bus. |
| $\overline{\text{HAS}}$/HAS | Input | | **Host Address Strobe**—When HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the Host Address Strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low ($\overline{\text{HAS}}$) following reset. |
| PB8 | Input or Output | | **Port B 8**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

Table 1-11  Host Interface (Continued)

| Signal Name | Type | State During Reset or Stop[1] | Signal Description |
|---|---|---|---|
| HA1 | Input | Disconnected | **Host Address Input 1**—When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 1 of the Host Address (HA1) input bus. |
| HA8 | Input | | **Host Address 8**—When HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the Host Address (HA8) input bus. |
| PB9 | Input or Output | | **Port B 9**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |
| HA2 | Input | Disconnected | **Host Address Input 2**—When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the Host Address (HA2) input bus. |
| HA9 | Input | | **Host Address 9**—When HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the Host Address (HA9) input bus. |
| PB10 | Input or Output | | **Port B 10**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

**Table 1-11** Host Interface (Continued)

| Signal Name | Type | State During Reset or Stop[1] | Signal Description |
|---|---|---|---|
| HRW | Input | Disconnected | **Host Read/Write**—When HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/Write (HRW) input. |
| $\overline{\text{HRD}}$/HRD | Input | | **Host Read Data**—When HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Host Read Data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset. |
| PB11 | Input or Output | | **Port B 11**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |
| $\overline{\text{HDS}}$/HDS | Input | Disconnected | **Host Data Strobe**—When HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Data Strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset. |
| $\overline{\text{HWR}}$/HWR | Input | | **Host Write Data**—When HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Host Write Data Strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset. |
| PB12 | Input or Output | | **Port B 12**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

**Table 1-11**  Host Interface (Continued)

| Signal Name | Type | State During Reset or Stop[1] | Signal Description |
|---|---|---|---|
| HCS | Input | Disconnected | **Host Chip Select**—When HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is the Host Chip Select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{\text{HCS}}$) after reset. |
| HA10 | Input | | **Host Address 10**—When HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the Host Address (HA10) input bus. |
| PB13 | Input or Output | | **Port B 13**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |
| $\overline{\text{HREQ}}$/ HREQ | Output | Disconnected | **Host Request**—When HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Request (HREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output. |
| $\overline{\text{HTRQ}}$/ HTRQ | Output | | **Transmit Host Request**—When HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Transmit Host Request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output. |
| PB14 | Input or Output | | **Port B 14**—When the HI08 is programmed to interface a multiplexed host bus and the signal is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

Table 1-11  Host Interface (Continued)

| Signal Name | Type | State During Reset or Stop[1] | Signal Description |
|---|---|---|---|
| $\overline{\text{HACK}}$/ HACK | Input | Disconnected | **Host Acknowledge**—When HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset. |
| $\overline{\text{HRRQ}}$/ HRRQ | Output | | **Receive Host Request**—When HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Receive Host Request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output. |
| PB15 | Input or Output | | **Port B 15**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.

This input is 5 V tolerant. |

Note:  1.  Wait state does not affect signal state.

# ENHANCED SYNCHRONOUS SERIAL INTERFACE 0 (ESSI0)

There are two synchronous serial interfaces (ESSI0 and ESSI1) that provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals which implement the Motorola Serial Peripheral Interface (SPI).

Table 1-12  Enhanced Synchronous Serial Interface 0 (ESSI0)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| SC00 | Input or Output | Input | Disconnected | **Serial Control 0**—The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal will be used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used either for Transmitter 1 output or for Serial I/O Flag 0. |
| PC0 | | | | **Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port Directions Register (PRR0). The signal can be configured as ESSI signal SC00 through the Port Control Register (PCR0). |
| | | | | This input is 5 V tolerant. |
| SC01 | Input/ Output | Input | Disconnected | **Serial Control 1**—The function of this signal is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1. |
| PC1 | Input or Output | | | **Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC01 through PCR0. |
| | | | | This input is 5 V tolerant. |

**Preliminary Data**

**Table 1-12**  Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | **Reset** | **Stop** | |
| SC02 | Input/ Output | Input | Disconnected | **Serial Control Signal 2**—SC02 is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). |
| PC2 | Input or Output | | | **Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC02 through PCR0.<br><br>This input is 5 V tolerant. |
| SCK0 | Input/ Output | Input | Disconnected | **Serial Clock**—SCK0 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the ESSI interface. The SCK0 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes.<br><br>Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (i.e., the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. |
| PC3 | Input or Output | | | **Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SCK0 through PCR0.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

**Table 1-12**  Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| SRD0 | Input/ Output | Input | Disconnected | **Serial Receive Data**—SRD0 receives serial data and transfers the data to the ESSI receive shift register. SRD0 is an input when data is being received. |
| PC4 | Input or Output | | | **Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SRD0 through PCR0.<br><br>This input is 5 V tolerant. |
| STD0 | Input/ Output | Input | Disconnected | **Serial Transmit Data**—STD0 is used for transmitting data from the serial transmit shift register. STD0 is an output when data is being transmitted. |
| PC5 | Input or Output | | | **Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal STD0 through PCR0.<br><br>This input is 5 V tolerant. |
| Note: 1.  Wait state does not affect signal state. | | | | |

**Preliminary Data**

# ENHANCED SYNCHRONOUS SERIAL INTERFACE 1 (ESSI1)

Table 1-13  Enhanced Synchronous Serial Interface 1 (ESSI1)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| SC10 | Input or Output | Input | Disconnected | **Serial Control 0**—The function of SC10 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal will be used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used either for Transmitter 1 output or for Serial I/O Flag 0. |
| PD0 | | | | **Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port Directions Register (PRR1). The signal can be configured as an ESSI signal SC10 through the Port Control Register (PCR1). |
| | | | | This input is 5 V tolerant. |
| SC11 | Input/ Output | Input | Disconnected | **Serial Control 1**—The function of this signal is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1. |
| PD1 | Input or Output | | | **Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC11 through PCR1. |
| | | | | This input is 5 V tolerant. |

**Table 1-13**  Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| SC12 | Input/Output | Input | Disconnected | **Serial Control Signal 2**—SC12 is used for frame sync I/O. SC12 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in Synchronous operation). |
| PD2 | Input or Output | | | **Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC12 through PCR1.

This input is 5 V tolerant. |
| SCK1 | Input/Output | Input | Disconnected | **Serial Clock**—SCK1 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the ESSI interface. The SCK1 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes.

Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. |
| PD3 | Input or Output | | | **Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SCK1 through PCR1.

This input is 5 V tolerant. |

**Preliminary Data**

**Table 1-13** Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| SRD1 | Input/ Output | Input | Disconnected | **Serial Receive Data**—SRD1 receives serial data and transfers the data to the ESSI receive shift register. SRD1 is an input when data is being received. |
| PD4 | Input or Output | | | **Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1.<br><br>This input is 5 V tolerant. |
| STD1 | Input/ Output | Input | Disconnected | **Serial Transmit Data**—STD1 is used for transmitting data from the serial transmit shift register. STD1 is an output when data is being transmitted. |
| PD5 | Input or Output | | | **Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1.<br><br>This input is 5 V tolerant. |
| Note: 1. Wait state does not affect signal state. | | | | |

# SERIAL COMMUNICATION INTERFACE (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication to other DSPs, microprocessors, or peripherals such as modems.

**Table 1-14**  Serial Communication Interface (SCI)

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | **Reset** | **Stop** | |
| RXD | Input | Input | Disconnected | **Serial Receive Data**—This input receives byte oriented serial data and transfers it to the SCI receive shift register. |
| PE0 | Input or Output | | | **Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). <br><br>This input is 5 V tolerant. |
| TXD | Output (may be open drain) | Input | Disconnected | **Serial Transmit Data**—This signal transmits data from SCI transmit data register. |
| PE1 | Input or Output | | | **Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. <br><br>This input is 5 V tolerant. |
| SCLK | Input/ Output | Input | Disconnected | **Serial Clock**—This is the bidirectional Schmitt-trigger input signal providing the input or output clock used by the transmitter and/or the receiver. |
| PE2 | Input or Output | | | **Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal SCLK through the SCI PCR. <br><br>This input is 5 V tolerant. |
| Note:   1.   Wait state does not affect signal state. | | | | |

**Preliminary Data**

# TIMERS

Three identical and independent timers are implemented in the DSP56304. Each timer can use internal or external clocking, and can interrupt the DSP56304 after a specified number of events (clocks), or can signal an external device after counting a specific number of internal events.

**Table 1-15**  Triple Timer Signals

| Signal Name | Type | State During[1] | | Signal Description |
|---|---|---|---|---|
| | | Reset | Stop | |
| TIO0 | Input or Output | Input | Disconnected | **Timer 0 Schmitt-Trigger Input/Output**—When Timer 0 functions as an external event counter or in Measurement mode, TIO0 is used as input. When Timer 0 functions in Watchdog, Timer, or Pulse Modulation mode, TIO0 is used as output.<br><br>The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 0 Control/Status Register (TCSR0).<br><br>This input is 5 V tolerant. |
| TIO1 | Input or Output | Input | Disconnected | **Timer 1 Schmitt-Trigger Input/Output**—When Timer 1 functions as an external event counter or in Measurement mode, TIO1 is used as input. When Timer 1 functions in Watchdog, Timer, or Pulse Modulation mode, TIO1 is used as output.<br><br>The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 1 Control/Status Register (TCSR1).<br><br>This input is 5 V tolerant. |
| TIO2 | Input or Output | Input | Disconnected | **Timer 2 Schmitt-Trigger Input/Output**—When Timer 2 functions as an external event counter or in Measurement mode, TIO2 is used as input. When Timer 2 functions in Watchdog, Timer, or Pulse Modulation mode, TIO2 is used as output.<br><br>The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 2 Control/Status Register (TCSR2).<br><br>This input is 5 V tolerant. |

Note:   1.   Wait state does not affect signal state.

**Preliminary Data**

# OnCE/JTAG INTERFACE

Table 1-16  OnCE/JTAG Interface

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| TCK | Input | Input | **Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic.<br><br>This input is 5 V tolerant. |
| TDI | Input | Input | **Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.<br><br>This input is 5 V tolerant. |
| TDO | Output | Tri-stated | **Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK. |
| TMS | Input | Input | **Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.<br><br>This input is 5 V tolerant. |
| $\overline{\text{TRST}}$ | Input | Input | **Test Reset**—$\overline{\text{TRST}}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted after power up.<br><br>This input is 5 V tolerant. |

**Preliminary Data**

Table 1-16   OnCE/JTAG Interface (Continued)

| Signal Name | Type | State During Reset | Signal Description |
|---|---|---|---|
| $\overline{DE}$ | Input/ Output | Input | **Debug Event**—$\overline{DE}$ is an open-drain, bidirectional, active-low signal providing, as an input, a means of entering the Debug mode of operation from an external command controller, and, as an output, a means of acknowledging that the chip has entered the Debug mode. This signal, when asserted as an input, causes the DSP56300 core to finish the current instruction being executed, save the instruction pipeline information, enter the Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters the Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{DE}$ has an internal pull-up resistor. |
| | | | This is not a standard part of the JTAG Test Access Port (TAP) Controller. The signal connects directly to the OnCE module to initiate Debug mode directly or to provide a direct external indication that the chip has entered the Debug mode. All other interface with the OnCE module must occur through the JTAG port. |
| | | | This input is 5 V tolerant. |

**Preliminary Data**

# SECTION 2

# SPECIFICATIONS

## INTRODUCTION

The DSP56304 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56304 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

## MAXIMUM RATINGS

### CAUTION

**This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$).**

**Note:** In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

**Preliminary Data**

Table 2-1  Maximum Ratings

| Rating[1] | Symbol | Value[1,2] | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +4.0 | V |
| All input voltages excluding "5 V tolerant" inputs[3] | $V_{IN}$ | GND − 0.3 to $V_{CC}$ + 0.3 | V |
| All "5 V tolerant" input voltages[3] | $V_{IN5}$ | GND − 0.3 to $V_{CC}$ + 3.95 | V |
| Current drain per pin excluding $V_{CC}$ and GND | I | 10 | mA |
| Operating temperature range | $T_J$ | −40 to +100 | °C |
| Storage temperature | $T_{STG}$ | −55 to +150 | °C |

Note:
1. GND = 0 V, $V_{CC}$ = 3.3 V ± 0.3 V, $T_J$ = −40°C to +100°C, CL = 50 pF + 2 TTL Loads.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. CAUTION: All "5 V Tolerant" input voltages cannot be more than 3.95 V greater than the supply voltage; this restriction applies to "power on", as well as during normal operation. In any case, the input voltages can not be more than 5.75 V. "5 V Tolerant" inputs are inputs that tolerate 5 V.

# THERMAL CHARACTERISTICS

Table 2-2  Thermal Characteristics

| Characteristic | Symbol | TQFP Value | PBGA[3] Value | PBGA[4] Value | Unit |
|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance | $R_{\theta JA}$ or $\theta_{JA}$ | 55.7 | 57 | 28 | °C/W |
| Junction-to-case thermal resistance | $R_{\theta JC}$ or $\theta_{JC}$ | 11.4 | 15 | — | °C/W |
| Thermal characterization parameter | $\Psi_{JT}$ | 6.8 | 8 | — | °C/W |

Note:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values; testing is not complete. See note 1 for test board conditions.
4. These are simulated values; testing is not complete. The test board has two, 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

**Preliminary Data**

# DC ELECTRICAL CHARACTERISTICS

**Table 2-3** DC Electrical Characteristics[6]

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| Input high voltage<br>• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$<br>• MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/<br>$\overline{NMI}$ and all JTAG/ESSI/SCI/<br>Timer/HI08 pins<br>• EXTAL[8] | $V_{IH}$<br>$V_{IHP}$<br><br><br>$V_{IHX}$ | 2.0<br>2.0<br><br><br>0.8 | —<br>—<br><br><br>— | $V_{CC}$<br>$V_{CC} + 3.95$<br><br><br>$V_{CC}$ | V<br>V<br><br><br>V |
| Input low voltage<br>• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[1]/<br>$\overline{IRQ}$[1], $\overline{RESET}$, PINIT<br>• All JTAG/ESSI/SCI/Timer/<br>HI08 pins<br>• EXTAL[8] | $V_{IL}$<br><br>$V_{ILP}$<br><br>$V_{ILX}$ | −0.3<br><br>−0.3<br><br>−0.3 | —<br><br>—<br><br>— | 0.8<br><br>0.8<br><br>0.2 | V<br><br>V<br><br>V |
| Input leakage current | $I_{IN}$ | −10 | — | 10 | µA |
| High impedance (off-state) input current (@ 2.4 V / 0.4 V) | $I_{TSI}$ | −10 | — | 10 | µA |
| Output high voltage<br>• TTL ($I_{OH} = -0.4$ mA)[5,7]<br>• CMOS ($I_{OH} = -10$ µA)[5] | $V_{OH}$ | $V_{CC} - 0.4$<br>$V_{CC} - 0.01$ | —<br>— | —<br>— | <br>V<br>V |
| Output low voltage<br>• TTL ($I_{OL} = 3.0$ mA, open-drain pins $I_{OL} = 6.7$ mA)[5,7]<br>• CMOS ($I_{OL} = 10$ µA)[5] | $V_{OL}$ | —<br><br>— | —<br><br>— | 0.4<br><br>0.01 | <br>V<br><br>V |
| Internal supply current[2]:<br>• In Normal mode<br><br>• In Wait mode[3]<br><br>• In Stop mode[4] | <br>$I_{CCI}$<br><br>$I_{CCW}$<br><br>$I_{CCS}$ | <br>—<br><br>—<br><br>— | <br>66 MHz: 84<br>80 MHz: 102<br>66 MHz: 5<br>80 MHz: 6<br>66 MHz: 100<br>80 MHz: 100 | <br>66 MHz: 120<br>80 MHz: 145<br>66 MHz: 7<br>80 MHz: 9<br>66 MHz: 150<br>80 MHz: 150 | <br>mA<br>mA<br>mA<br>mA<br>µA<br>µA |
| PLL supply current in Stop mode[5] | | — | 1 | 2.5 | mA |
| Input capacitance[5] | $C_{IN}$ | — | — | 10 | pF |

**Preliminary Data**

**Table 2-3** DC Electrical Characteristics[6] (Continued)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|

Note:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins
2. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with $V_{CC} = 3.0$ V at $T_J = 100°C$. Maximum internal supply current is measured with $V_{CC} = 3.6$ V at $T_J = 100°C$.
3. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL and XTAL signals are disabled during Stop state.
4. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
5. Periodically sampled and not 100% tested
6. $V_{CC} = 3.3$ V ± 0.3 V; $T_J = -40°C$ to +100 °C, $C_L = 50$ pF + 2 TTL Loads
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the extreme values for $V_{IHX}$ (0.8 $V_{CC}$) or $V_{ILX}$ (0.2 $V_{CC}$) may cause increased DC current. To achieve the lowest current, maintain the minimum $V_{IHX}$ above 0.9 $V_{CC}$ and the maximum $V_{ILX}$ below 0.1 $V_{CC}$.

# AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in the AC electrical characteristics section are tested with a $V_{IL}$ maximum of 0.3 V and a $V_{IH}$ minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in **Note 6** of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56304 output levels are measured with the production test machine $V_{OL}$ and $V_{OH}$ reference levels set at 0.8 V and 2.0 V, respectively.

# INTERNAL CLOCKS

**Table 2-4** Internal Clocks, CLKOUT

| Characteristics | Symbol | Expression[1,2] | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| Internal operation frequency and CLKOUT with PLL enabled | f | — | $(Ef \times MF)/(PDF \times DF)$ | — |

**Preliminary Data**

**Table 2-4** Internal Clocks, CLKOUT

| Characteristics | Symbol | Expression[1,2] | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| Internal operation frequency and CLKOUT with PLL disabled | $f$ | — | $Ef/2$ | — |
| Internal clock and CLKOUT high period <br>• With PLL disabled | $T_H$ | — | $ET_C$ | — |
| • With PLL enabled and $MF \leq 4$ | | $0.49 \times ET_C \times PDF \times DF/MF$ | — | $0.51 \times ET_C \times PDF \times DF/MF$ |
| • With PLL enabled and $MF > 4$ | | $0.47 \times ET_C \times PDF \times DF/MF$ | — | $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock and CLKOUT low period <br>• With PLL disabled | $T_L$ | — | $ET_C$ | — |
| • With PLL enabled and $MF \leq 4$ | | $0.49 \times ET_C \times PDF \times DF/MF$ | — | $0.51 \times ET_C \times PDF \times DF/MF$ |
| • With PLL enabled and $MF > 4$ | | $0.47 \times ET_C \times PDF \times DF/MF$ | — | $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock and CLKOUT cycle time with PLL enabled | $T_C$ | — | $ET_C \times PDF \times DF/MF$ | — |
| Internal clock and CLKOUT cycle time with PLL disabled | $T_C$ | — | $2 \times ET_C$ | — |
| Instruction cycle time | $I_{CYC}$ | — | $T_C$ | — |

Note:
1. DF = Division Factor
   Ef = External frequency
   $ET_C$ = External clock cycle
   MF = Multiplication Factor
   PDF = Predivision Factor
   $T_C$ = internal clock cycle
2. See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

**Preliminary Data**

# EXTERNAL CLOCK OPERATION

The DSP56304 system clock may be derived from the on–chip crystal oscillator, as shown in **Figure 1** on the cover page, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically not connected to the board or socket (see **Figure 2-2**).
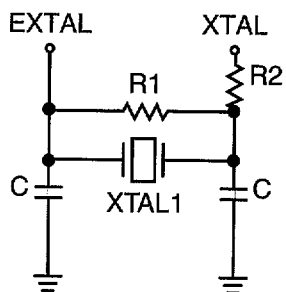


**Fundamental Frequency**
**Fork Crystal Oscillator**

**Suggested Component Values:**

$f_{OSC}$ = 32.768 kHz
R1 = 3.9 M$\Omega$ ± 10%
C = 22 pF ± 20%
R2 = 200 k$\Omega$ ± 10%

Calculations were done for a 32.768 kHz crystal with the following parameters:
a load capacitance ($C_L$) of 12.5 pF,
a shunt capacitance ($C_0$) of 1.8 pF,
a series resistance of 40 k$\Omega$, and
a drive level of 1 $\mu$W.
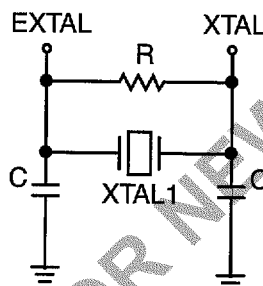
**Fundamental Frequency**
**Crystal Oscillator**

**Suggested Component Values:**

$f_{OSC}$ = 4 MHz        $f_{OSC}$ = 20 MHz
R = 680 k$\Omega$ ± 10%   R = 680 k$\Omega$ ± 10%
C = 56 pF ± 20%      C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
a $C_L$ of 30/20 pF,
a $C_0$ of 7/6 pF,
a series resistance of 100/20 $\Omega$, and
a drive level of 2 mW.

**Figure 2-1** Crystal Oscillator Circuits

Note:    The midpoint is 0.5 ($V_{IHC}$ + $V_{ILC}$).
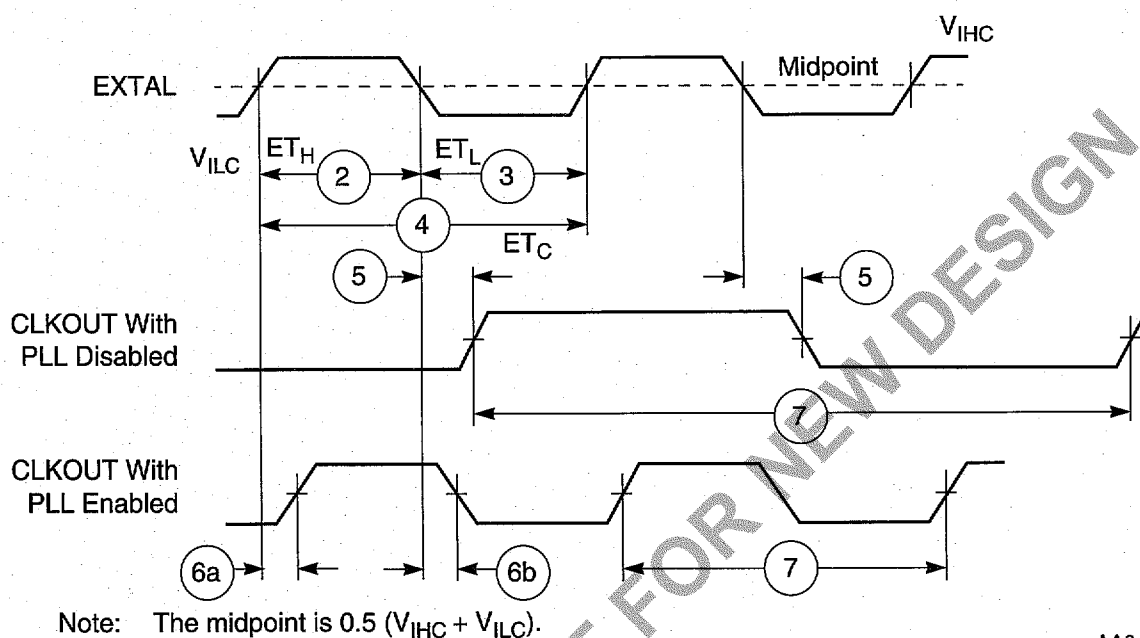
AA0459

**Figure 2-2** External Clock Timing

**Table 2-5**  Clock Operation

| No. | Characteristics | Symbol | 66 MHz | | 80 MHz | |
|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max |
| 1 | Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of the external clock should be 3 ns maximum. | Ef | 0 | 66.0 | 0 | 80.0 |
| 2 | Clock input high[1,2] • With PLL disabled (46.7%–53.3% duty cycle[6]) | $ET_H$ | 7.08 ns | ∞ | 5.84 ns | ∞ |
| | • With PLL enabled (42.5%–57.5% duty cycle[6]) | | 6.44 ns | 157.0 μs | 5.31 ns | 157.0 μs |
| 3 | Clock input low[1,2] • With PLL disabled (46.7%–53.3% duty cycle[6]) | $ET_L$ | 7.08 ns | ∞ | 5.84 ns | ∞ |
| | • With PLL enabled (42.5%–57.5% duty cycle[6]) | | 6.44 ns | 157.0 μs | 5.31 ns | 157.0 μs |
| 4 | Clock cycle time[2] • With PLL disabled | $ET_C$ | 30.3 ns | ∞ | 25.0 ns | ∞ |
| | • With PLL enabled | | 15.15 ns | 273.1 μs | 12.50 ns | 273.1 μs |
| 5 | CLKOUT change from EXTAL fall with PLL disabled | | 4.3 ns | 11.0 ns | 4.3 ns | 11.0 ns |

**Preliminary Data**

**Table 2-5** Clock Operation (Continued)

| No. | Characteristics | Symbol | 66 MHz | | 80 MHz | |
|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max |
| 6 | CLKOUT from EXTAL with PLL enabled[3,5]<br>  a.  MF = 1, PDF = 1, Ef > 15 MHz<br>  b.  MF = 2 or 4, PDF = 1, Ef > 15 MHz, or,<br>     MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz | | 0.0 ns<br>0.0 ns | 1.8 ns<br>1.8 ns | 0.0 ns<br>0.0 ns | 1.8 ns<br>1.8 ns |
| 7 | Instruction cycle time = $I_{CYC}$ = $T_C$[4]<br>(See **Table 2-4**.) (46.7%–53.3% duty cycle)<br>  •  With PLL disabled<br><br>  •  With PLL enabled | $I_{CYC}$ | <br><br>30.3 ns<br><br>15.15 ns | <br><br>∞<br><br>8.53 µs | <br><br>25.0 ns<br><br>12.50 ns | <br><br>∞<br><br>8.53 µs |

Note:
1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum $V_{CO}$ and maximum MF.
3. Periodically sampled and not 100% tested
4. The maximum value for PLL enabled is given for minimum $V_{CO}$ and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

# PHASE LOCK LOOP (PLL) CHARACTERISTICS

**Table 2-6** PLL Characteristics

| Characteristics | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $V_{CO}$ frequency when PLL enabled<br>$(MF \times E_f \times 2 / PDF)$ | 30 | 132 | 30 | 160 | MHz |
| PLL external capacitor<br>(PCAP pin to $V_{CCP}$)<br>($C_{PCAP}$[1])<br>  •  @ MF ≤ 4 | $(MF \times 425) - 125$ | $(MF \times 590) - 175$ | $(MF \times 425) - 125$ | $(MF \times 590) - 175$ | pF |
|   •  @ MF > 4 | $MF \times 520$ | $MF \times 920$ | $MF \times 520$ | $MF \times 920$ | pF |

Note: $C_{PCAP}$ is the value of the PLL capacitor (connected between the PCAP pin and $V_{CCP}$). The recommended value in pF for $C_{PCAP}$ can be computed from one of the following equations:

$(500 \times MF) - 150$, for MF ≤ 4, or

$690 \times MF$, for MF > 4.

**Preliminary Data**

# RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

**Table 2-7** Reset, Stop, Mode Select, and Interrupt Timing[6]

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 8 | Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3] | — | — | 26.0 | — | 26.0 | ns |
| 9 | Required $\overline{\text{RESET}}$ duration[4] | | | | | | |
| | • Power on, external clock generator, PLL disabled | $50 \times ET_C$ | 760.0 | — | 625.0 | — | ns |
| | • Power on, external clock generator, PLL enabled | $1000 \times ET_C$ | 15.2 | — | 12.5 | — | ms |
| | • Power on, internal oscillator | $75000 \times ET_C$ | 1.14 | — | 1.0 | — | ms |
| | • During STOP, XTAL disabled (PCTL Bit 16 = 0) | $75000 \times ET_C$ | 1.14 | — | 1.0 | — | ms |
| | • During STOP, XTAL enabled (PCTL Bit 16 = 1) | $2.5 \times T_C$ | 38.0 | — | 31.3 | — | ns |
| | • During normal operation | $2.5 \times T_C$ | 38.0 | — | 31.3 | — | ns |
| 10 | Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] | | | | | | |
| | • Minimum | **66 MHz:** $3.25 \times T_C + 2.0$ | 51.0 | — | — | — | ns |
| | | **80 MHz:** $3.25 \times T_C + 2.0$ | — | — | 42.6 | — | ns |
| | • Maximum | **66 MHz:** $20.25\, T_C + 11.0$ | — | 318.0 | — | — | ns |
| | | **80 MHz:** $20.25\, T_C + 9.95$ | — | — | — | 263.1 | ns |
| 11 | Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 | | | | | | |
| | • Minimum | | 9.0 | — | 7.4 | — | ns |
| | • Maximum | $T_C$ | — | 15.2 | — | 12.5 | ns |
| 12 | Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output | | | | | | |
| | • Minimum | $3.25 \times T_C + 1.0$ | 50.0 | — | 41.6 | — | ns |
| | • Maximum | $20.25\, T_C + 5.0$ | — | 312.0 | — | 258.1 | ns |
| 13 | Mode select setup time | | 30.0 | — | 30.0 | — | ns |

**Preliminary Data**

**Table 2-7** Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|--------|--------|--------|------|
| | | | Min | Max | Min | Max | |
| 14 | Mode select hold time | | 0.0 | — | 0.0 | — | ns |
| 15 | Minimum edge-triggered interrupt request assertion width | | 10.0 | — | 8.25 | — | ns |
| 16 | Minimum edge-triggered interrupt request deassertion width | | 10.0 | — | 8.25 | — | ns |
| 17 | Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory access address out valid | | | | | | |
| | • Caused by first interrupt instruction fetch | $4.25 \times T_C + 2.0$ | 66.0 | — | 55.1 | — | ns |
| | • Caused by first interrupt instruction execution | $7.25 \times T_C + 2.0$ | 112.0 | — | 92.6 | — | ns |
| 18 | Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution | $10 \times T_C + 5.0$ | 157.0 | — | 130.0 | — | ns |
| 19 | Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1] | **66 MHz**[8]: $3.75 \times T_C + WS \times T_C - 14$ | — | | | | ns |
| | | **80 MHz**[8]: $3.75 \times T_C + WS \times T_C - 12.4$ | | | — | | ns |
| 20 | Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1] | **66 MHz**[8]: $3.25 \times T_C + WS \times T_C - 14$ | — | | | | ns |
| | | **80 MHz**[8]: $3.25 \times T_C + WS \times T_C - 12.4$ | | | — | | ns |

**Preliminary Data**

**Table 2-7** Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 21 | Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1] | | | | | | |
| | • SSRAM for all WS | **66 MHz[8]:** $(3.75 + WS) \times T_C - 14$ | — | | | | ns |
| | | **80 MHz[8]:** $(3.75 + WS) \times T_C - 12.4$ | | | — | | ns |
| | • DRAM for all WS | **66 MHz[8]:** $(3.5 + WS) \times T_C - 14$ | — | | | | ns |
| | | **80 MHz[8]:** $(3.5 + WS) \times T_C - 12.4$ | | | — | | ns |
| | • SRAM WS = 1 | **66 MHz[8]:** $(WS + 3.5) \times T_C - 14$ | — | | | | ns |
| | | **80 MHz[8]:** $(WS + 3.5) \times T_C - 12.4$ | | | — | | ns |
| | • SRAM WS = 2, 3 | **66 MHz[8]:** $(WS + 3) \times T_C - 14$ | — | | | | ns |
| | | **80 MHz[8]:** $(WS + 3) \times T_C - 12.4$ | | | — | | ns |
| | • SRAM WS ≥ 4 | **66 MHz[8]:** $(2.5 + WS) \times T_C - 14$ | — | | | | ns |
| | | **80 MHz[8]:** $(2.5 + WS) \times T_C - 12.4$ | | | — | | ns |
| 22 | Synchronous interrupt setup time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to the CLKOUT Transition 2 | | 9.0 | $T_C$ | 7.4 | $T_C$ | ns |

**Preliminary Data**

**Table 2-7**   Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|--------|--------|--------|------|
| | | | Min | Max | Min | Max | |
| 23 | Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state | | | | | | |
| | • Minimum | $9.25 \times T_C + 1.0$ | 141.0 | — | 116.6 | — | ns |
| | • Maximum | $24.75 \times T_C + 5.0$ | — | 380.0 | — | 314.4 | ns |
| 24 | Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state | | 9.0 | — | 7.4 | — | ns |
| 25 | Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] | | | | | | |
| | • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0) | $PLC \times ET_C \times PDF + (128\,K - PLC/2) \times T_C$ | 2.0 | 64.1 | 1.6 | 52.8 | ms |
| | • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1) | $PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$ | 352.3 ns | 62.1 ms | 290.6 ns | 51.2 ms | |
| | • PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay) | $(8.25 \pm 0.5) \times T_C$ | 117.4 | 132.6 | 96.9 | 109.4 | ns |
| 26 | Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] | | | | | | |
| | • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0) | $PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$ | 64.1 | — | 52.8 | — | ms |
| | • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1) | $PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$ | 62.1 | — | 51.2 | — | ms |
| | • PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay) | $5.5 \times T_C$ | 83.4 | — | 68.8 | — | ns |

**Preliminary Data**

**Table 2-7**  Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 27 | Interrupt Requests Rate | | | | | | |
| | • HI08, ESSI, SCI, Timer | $12T_C$ | — | 181.8 | — | 150.0 | ns |
| | • DMA | $8T_C$ | — | 121.2 | — | 100.0 | ns |
| | • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) | $8T_C$ | — | 121.2 | — | 100.0 | ns |
| | • $\overline{IRQ}$, $\overline{NMI}$ (level trigger) | $12T_C$ | — | 181.8 | — | 150.0 | ns |
| 28 | DMA Requests Rate | | | | | | |
| | • Data read from HI08, ESSI, SCI | $6T_C$ | — | 90.9 | — | 75.0 | ns |
| | • Data write to HI08, ESSI, SCI | $7T_C$ | — | 106.1 | — | 87.5 | ns |
| | • Timer | $2T_C$ | — | 30.3 | — | 25.0 | ns |
| | • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) | $3T_C$ | — | 45.5 | — | 37.5 | ns |
| 29 | Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid | $4.25 \times T_C + 2.0$ | 66.0 | — | 55.1 | — | ns |

Note: 1. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

**Table 2-7** Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |

2. This timing depends on several settings:

For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (OMR Bit 6 = 0) will provide the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.

For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery time will be minimal (OMR Bit 6 setting is ignored).

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.

PLC value for PLL disable is 0.

The maximum value for $ET_C$ is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, $T_C$, $T_H$, and $T_L$ will not be constant, and their width may vary, so timing may vary as well.

3. Periodically sampled and not 100% tested

4. For an external clock generator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, $V_{CC}$ is valid, and the EXTAL input is active and valid.

For internal oscillator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted and $V_{CC}$ is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

When the $V_{CC}$ is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

5. If PLL does not lose lock
6. $V_{CC} = 3.3$ V ± 0.3 V; $T_J = -40°C$ to +100°C, $C_L = 50$ pF + 2 TTL Loads
7. WS = number of wait states (measured in clock cycles, number of $T_C$)
8. Use expression to compute maximum value.

**Preliminary Data**

**Figure 2-3** Reset Timing



**Figure 2-4** Synchronous Reset Timing
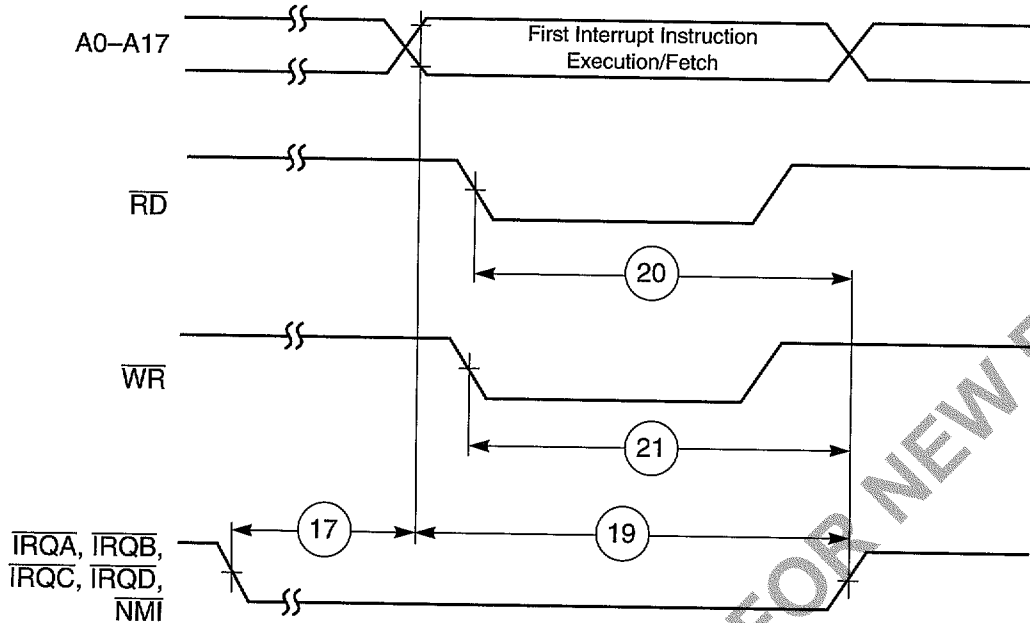
a) First Interrupt Instruction Execution
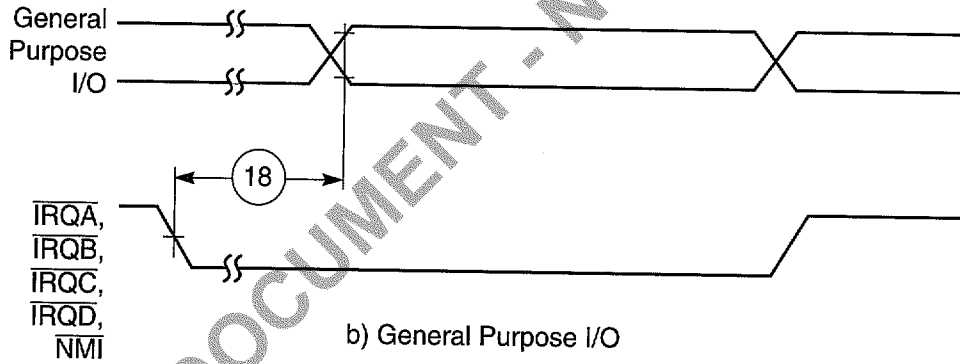
b) General Purpose I/O

AA0462

**Figure 2-5** External Fast Interrupt Timing
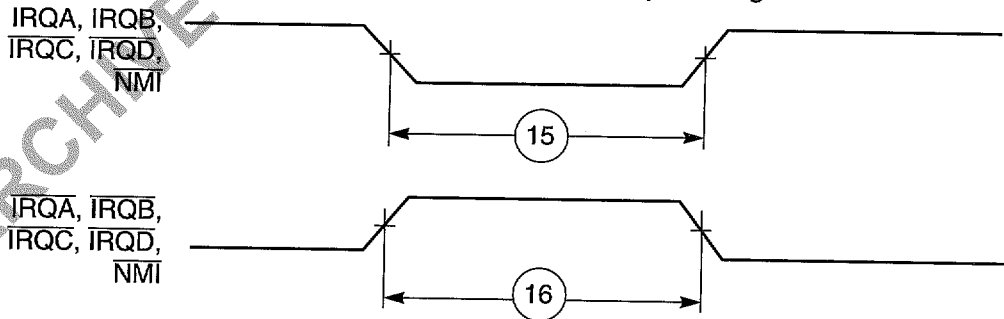


AA0463

**Figure 2-6** External Interrupt Timing (Negative Edge-Triggered)

**Preliminary Data**
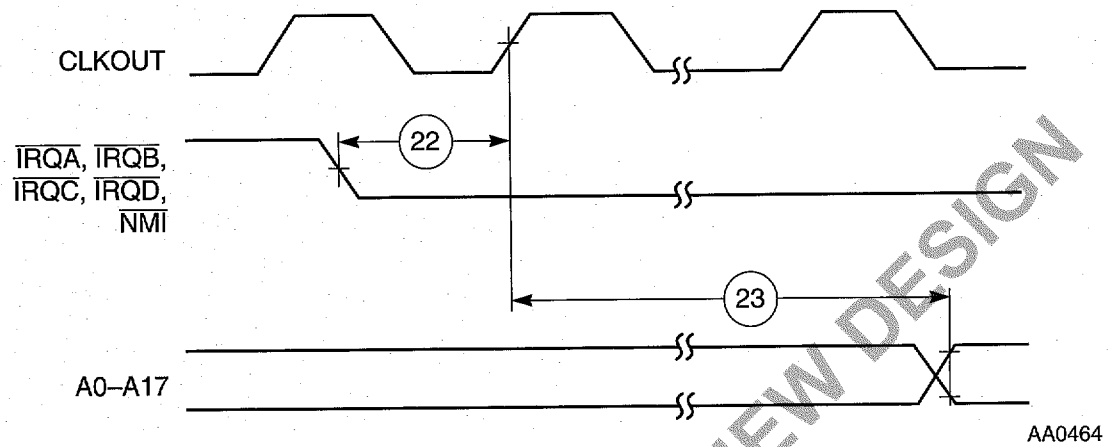
AA0464

**Figure 2-7** Synchronous Interrupt from Wait State Timing
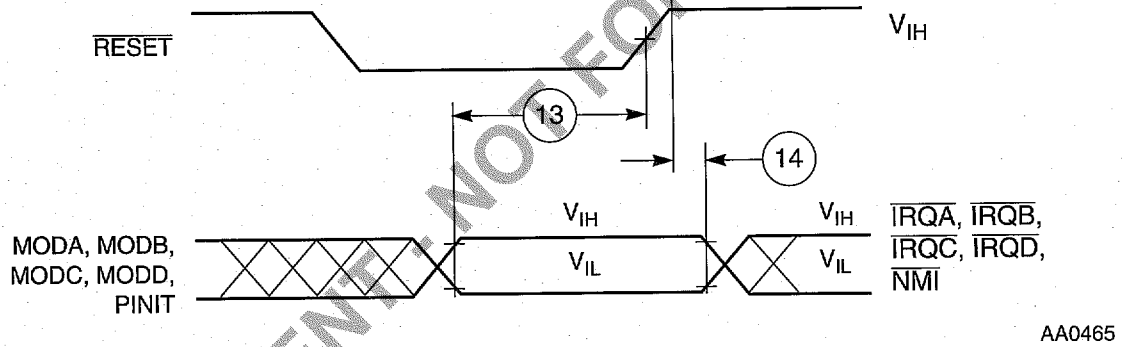


AA0465

**Figure 2-8** Operating Mode Select Timing
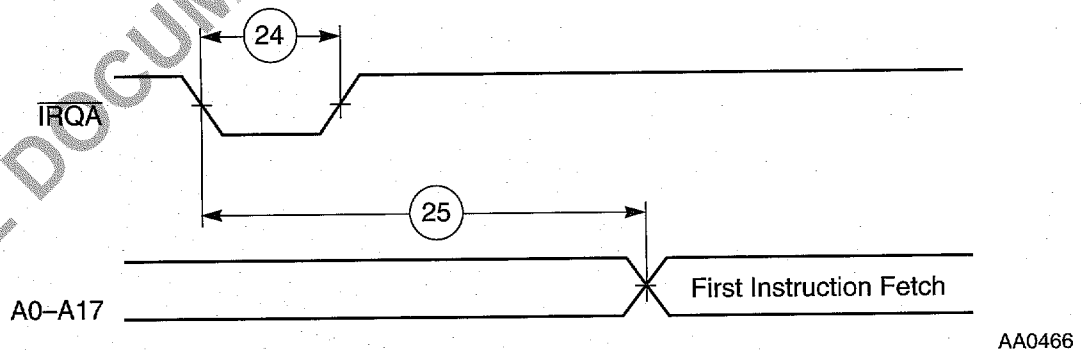


AA0466

**Figure 2-9** Recovery from Stop State Using $\overline{\text{IRQA}}$

**Preliminary Data**
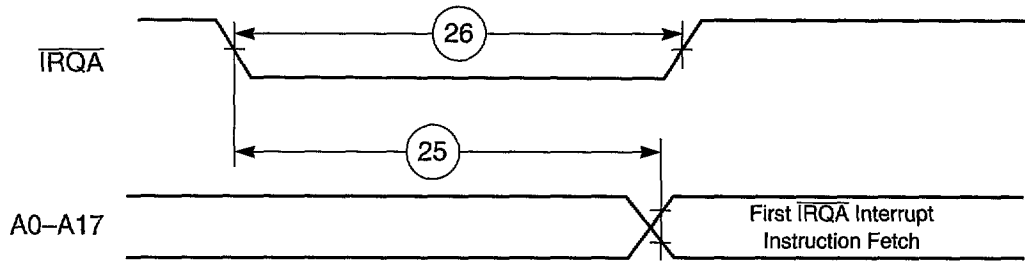
**Figure 2-10** Recovery from Stop State Using IRQA Interrupt Service
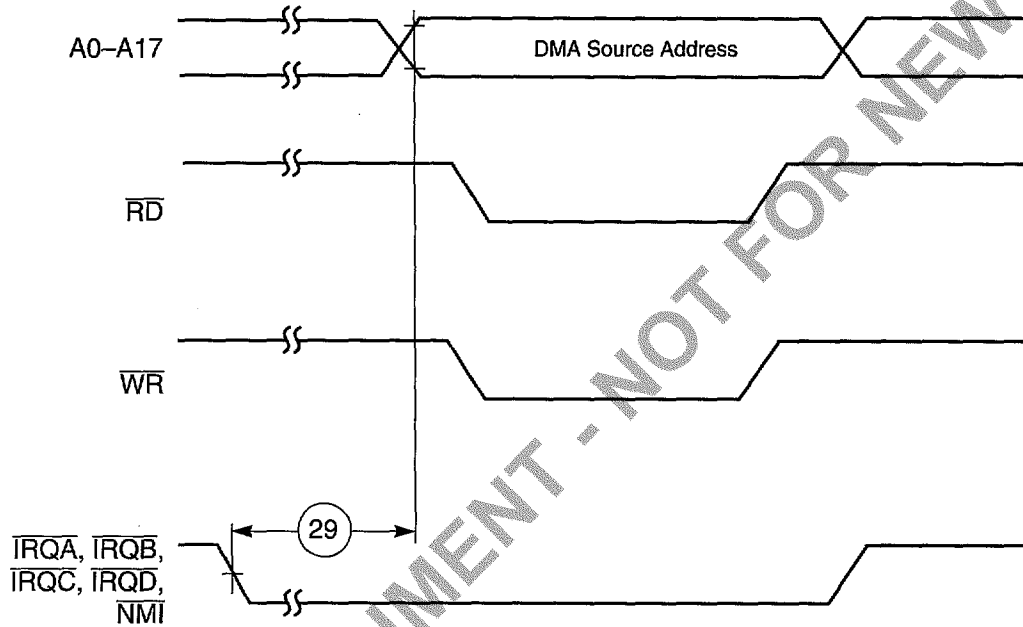


a) First Interrupt Instruction Execution

**Figure 2-11** External Memory Access (DMA Source) Timing

**Preliminary Data**

# EXTERNAL MEMORY INTERFACE (PORT A)

**Table 2-8**  SRAM Read and Write Accesses

| No. | Characteristics | Symbol | Expression[1] | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|---------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 100 | Address valid and AA assertion pulse width | $t_{RC}$, $t_{WC}$ | $(WS + 1) \times T_C - 4.0$ $[1 \leq WS \leq 3]$ | 26.3 | — | 21.0 | — | ns |
| | | | $(WS + 2) \times T_C - 4.0$ $[4 \leq WS \leq 7]$ | 86.9 | — | 71.0 | — | ns |
| | | | $(WS + 3) \times T_C - 4.0$ $[WS \geq 8]$ | 162.7 | — | 133.5 | — | ns |
| 101 | Address and AA valid to $\overline{WR}$ assertion | $t_{AS}$ | **66 MHz:** $0.25 \times T_C - 3.7$ $[WS = 1]$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ $[WS = 1]$ | — | — | 0.1 | — | ns |
| | | | $0.75 \times T_C - 4.0$ $[2 \leq WS \leq 3]$ | 7.4 | — | 5.4 | — | ns |
| | | | $1.25 \times T_C - 4.0$ $[WS \geq 4]$ | 14.9 | — | 11.6 | — | ns |
| 102 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $1.5 \times T_C - 4.5$ $[WS = 1]$ | 18.2 | — | 14.8 | — | ns |
| | | | $WS \times T_C - 4.0$ $[2 \leq WS \leq 3]$ | 26.3 | — | 21.0 | — | ns |
| | | | $(WS - 0.5) \times T_C - 4.0$ $[WS \geq 4]$ | 49.0 | — | 39.8 | — | ns |
| 103 | $\overline{WR}$ deassertion to address not valid | $t_{WR}$ | **66 MHz:** $0.25 \times T_C - 3.8$ $[1 \leq WS \leq 3]$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$ | — | — | 0.0 | — | ns |
| | | | $1.25 \times T_C - 4.0$ $[4 \leq WS \leq 7]$ | 14.9 | — | 11.6 | — | ns |
| | | | $2.25 \times T_C - 4.0$ $[WS \geq 8]$ | 30.1 | — | 24.1 | — | ns |

**Preliminary Data**

**Table 2-8**  SRAM Read and Write Accesses  (Continued)

| No. | Characteristics | Symbol | Expression[1] | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|-----|-----|-----|-----|------|
| | | | | Min | Max | Min | Max | |
| 104 | Address and AA valid to input data valid | $t_{AA}$, $t_{AC}$ | **66 MHz:** $(WS + 0.75) \times T_C - 10.0$ $[WS \geq 1]$ | — | 16.5 | — | — | ns |
| | | | **80 MHz:** $(WS + 0.75) \times T_C - 9.5$ $[WS \geq 1]$ | — | — | — | 12.4 | ns |
| 105 | $\overline{RD}$ assertion to input data valid | $t_{OE}$ | **66 MHz:** $(WS + 0.25) \times T_C - 10.0$ $[WS \geq 1]$ | — | 8.9 | — | — | ns |
| | | | **80 MHz:** $(WS + 0.25) \times T_C - 9.5$ $[WS \geq 1]$ | — | — | — | 6.1 | ns |
| 106 | $\overline{RD}$ deassertion to data not valid (data hold time) | $t_{OHZ}$ | | 0.0 | — | 0.0 | — | ns |
| 107 | Address valid to $\overline{WR}$ deassertion | $t_{AW}$ | $(WS + 0.75) \times T_C - 4.0$ $[WS \geq 1]$ | 22.5 | — | 17.9 | — | ns |
| 108 | Data valid to $\overline{WR}$ deassertion (data setup time) | $t_{DS}$ ($t_{DW}$) | **66 MHz:** $(WS - 0.25) \times T_C - 3.9$ $[WS \geq 1]$ | 7.5 | — | — | — | ns |
| | | | **80 MHz:** $(WS - 0.25) \times T_C - 3.3$ $[WS \geq 1]$ | — | — | 6.1 | — | ns |
| 109 | Data hold time from $\overline{WR}$ deassertion | $t_{DH}$ | **66 MHz:** $0.25 \times T_C - 3.7$ $[1 \leq WS \leq 3]$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$ | — | — | 0.1 | — | ns |
| | | | $1.25 \times T_C - 3.7$ $[4 \leq WS \leq 7]$ | 15.2 | — | 11.8 | — | ns |
| | | | $2.25 \times T_C - 3.7$ $[WS \geq 8]$ | 30.4 | — | 24.3 | — | ns |

**Preliminary Data**

Table 2-8 SRAM Read and Write Accesses (Continued)

| No. | Characteristics | Symbol | Expression[1] | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|---------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 110 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 3.7$ [WS = 1] | 7.7 | — | 5.7 | — | ns |
| | | | $0.25 \times T_C - 3.7$ [$2 \le WS \le 3$] | 0.1 | — | -0.6 | — | ns |
| | | | $-0.25 \times T_C - 3.7$ [WS $\ge$ 4] | -7.5 | — | -6.8 | — | ns |
| 111 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C + 0.2$ [$1 \le WS \le 3$] | — | 4.0 | — | 3.3 | ns |
| | | | $1.25 \times T_C + 0.2$ [$4 \le WS \le 7$] | — | 19.1 | — | 15.8 | ns |
| | | | $2.25 \times T_C + 0.2$ [WS $\ge$ 8] | — | 34.3 | — | 28.3 | ns |
| 112 | Previous $\overline{RD}$ deassertion to data active (write) | | $1.25 \times T_C - 4.0$ [$1 \le WS \le 3$] | 14.9 | — | 11.6 | — | ns |
| | | | $2.25 \times T_C - 4.0$ [$4 \le WS \le 7$] | 30.1 | — | 24.1 | — | ns |
| | | | $3.25 \times T_C - 4.0$ [WS $\ge$ 8] | 45.2 | — | 36.6 | — | ns |
| 113 | $\overline{RD}$ deassertion time | | $0.75 \times T_C - 4.0$ [$1 \le WS \le 3$] | 7.4 | — | 5.4 | — | ns |
| | | | $1.75 \times T_C - 4.0$ [$4 \le WS \le 7$] | 22.5 | — | 17.9 | — | ns |
| | | | $2.75 \times T_C - 4.0$ [WS $\ge$ 8] | 37.7 | — | 30.4 | — | ns |
| 114 | $\overline{WR}$ deassertion time | | $0.5 \times T_C - 3.5$ [WS = 1] | 4.1 | — | 2.8 | — | ns |
| | | | $T_C - 3.5$ [$2 \le WS \le 3$] | 11.7 | — | 9.0 | — | ns |
| | | | $2.5 \times T_C - 3.5$ [$4 \le WS \le 7$] | 34.4 | — | 27.8 | — | ns |
| | | | $3.5 \times T_C - 3.5$ [WS $\ge$ 8] | 49.5 | — | 40.3 | — | ns |
| 115 | Address valid to $\overline{RD}$ assertion | | $0.5 \times T_C - 4$ | 3.5 | — | 2.3 | — | ns |
| 116 | $\overline{RD}$ assertion pulse width | | $(WS + 0.25) \times T_C - 3.8$ | 15.1 | — | 11.8 | — | ns |

**Preliminary Data**

Table 2-8  SRAM Read and Write Accesses  (Continued)

| No. | Characteristics | Symbol | Expression[1] | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|---------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 117 | $\overline{RD}$ deassertion to address not valid | | $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$ | 0.7 | — | 0.1 | — | ns |
| | | | $1.25 \times T_C - 3.0$ $[4 \leq WS \leq 7]$ | 15.9 | — | 12.6 | — | ns |
| | | | $2.25 \times T_C - 3.0$ $[WS \geq 8]$ | 31.0 | — | 25.1 | — | ns |

Note:  1.  WS is the number of wait states specified in the BCR.
2.  $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads
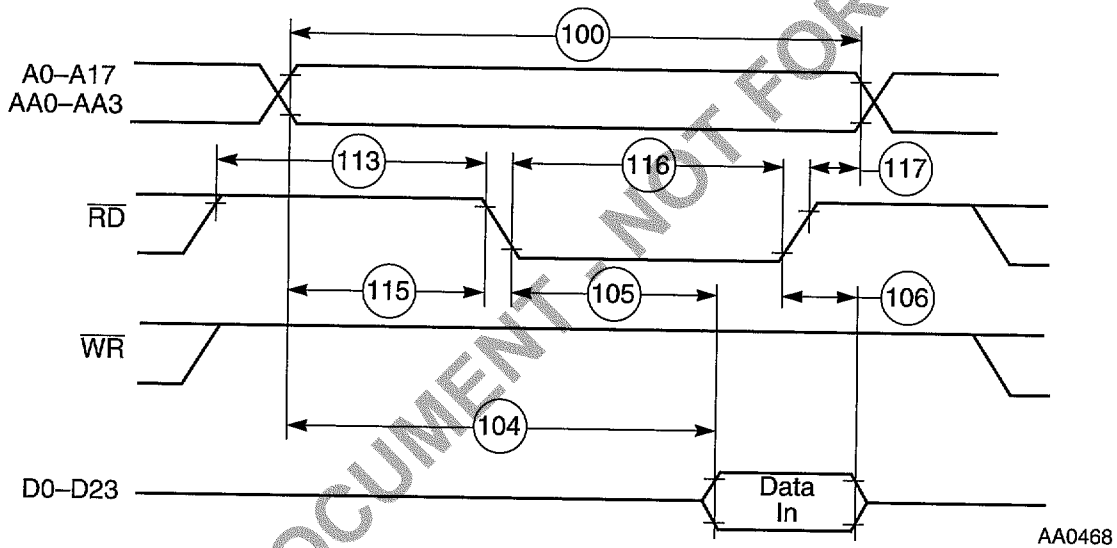


**Figure 2-12** SRAM Read Access
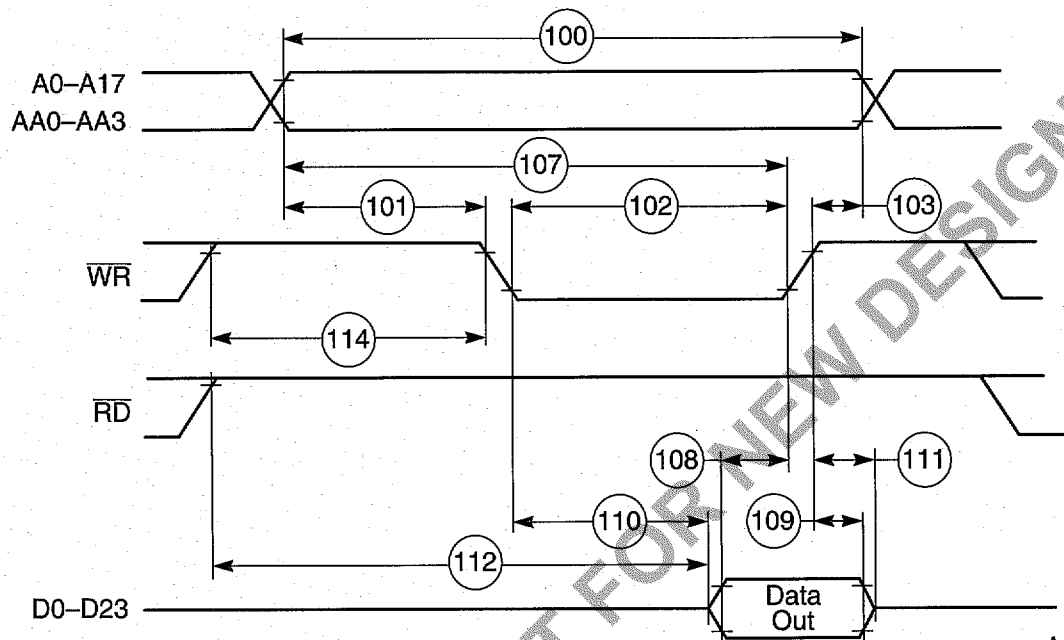
**Figure 2-13** SRAM Write Access

**Table 2-9** SSRAM Read and Write Access

| No. | Characteristics | Symbol | Expression[2] | 50 MHz[1] | | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|---------------|-----------|-----|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | Min | Max | |
| 118 | BCLK high to BCLK high (cycle time) | $t_{KHKH}$ | $(WS + 1) \times T_C$ | 20.0 | — | 15.1 | — | 12.5 | — | ns |
| 119 | BCLK high time | $t_{KHKL}$ | **50 MHz:** $0.5 \times T_C - 5.5$ **66 MHz:** $0.5 \times T_C - 4.8$ **80 MHz:** $0.5 \times T_C - 4.2$ | 4.5 | — | 2.8 | — | 1.5 | — | ns ns ns |
| 120 | BCLK low time | $t_{KLKH}$ | **50 MHz and 66 MHz:** $(WS + 0.5) \times T_C - 2.5$ **80 MHz:** $(WS + 0.5) \times T_C - 2.3$ | 7.5 | — | 5.1 | — | 4.0 | — | ns ns |
| 121 | BCLK high to input data valid | $t_{KHQV}$ | $(WS + 1) \times T_C - 7.5$ | — | 12.5 | — | 7.7 | — | 5.0 | ns |
| 122 | $\overline{RD}$ assertion to input data valid | $t_{GLQV}$ | $(WS + 1) \times T_C - 7.5$ | — | 12.5 | — | 7.7 | — | 5.0 | ns |

**Preliminary Data**

**Table 2-9** SSRAM Read and Write Access (Continued)

| No. | Characteristics | Symbol | Expression[2] | 50 MHz[1] | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| 123 | $\overline{RD}$ deassertion to input data invalid | $t_{GHQX}$ | | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| 124 | Address and AA setup time to clock high | $t_{AVKH}$ | $0.5 \times T_C - 4.0$ | 6.0 | — | 3.6 | — | 2.8 | — | ns |
| 125 | $\overline{WR}$ setup time to clock high | $t_{SWVKH}$ | $0.5 \times T_C - 4.0$ | 6.0 | — | 3.6 | — | 2.8 | — | ns |
| 126 | Data out setup time to clock high | $t_{DVKH}$ | $(WS + 0.5) \times T_C - 4.0$ | 6.0 | — | 3.6 | — | 2.8 | — | ns |
| 127 | BCLK high to address and AA invalid (hold time) | $t_{KHAX}$ | $(WS + 0.5) \times T_C - 1.0$ | 9.0 | — | 6.6 | — | 5.3 | — | ns |
| 128 | BCLK high to $\overline{WR}$ deassertion (hold time) | $t_{KHSWX}$ | $(WS + 0.5) \times T_C - 1.0$ | 9.0 | — | 6.6 | — | 5.3 | — | ns |
| 129 | BCLK high to input data invalid (data hold time) | $t_{KHQX2}$ | | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| 130 | BCLK high to output data invalid (data hold time) BCLK high to data high impedance | $t_{KHDX}$ | $0.5 \times T_C - 1.0$ | 9.0 | — | 6.6 | — | 5.3 | — | ns |

Note: 1. Using available SSRAM, the DSP56304 can be run at 50 MHz with zero wait states.
2. WS is the number of wait states specified in the BCR.
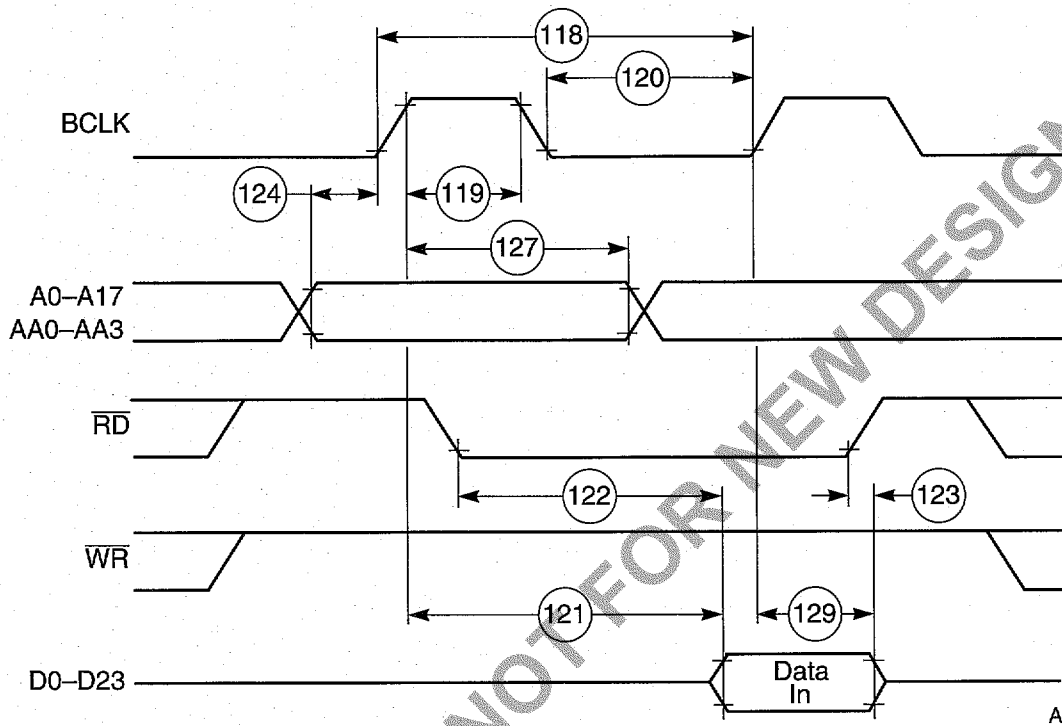
**Preliminary Data**

**Figure 2-14** SSRAM Read Access
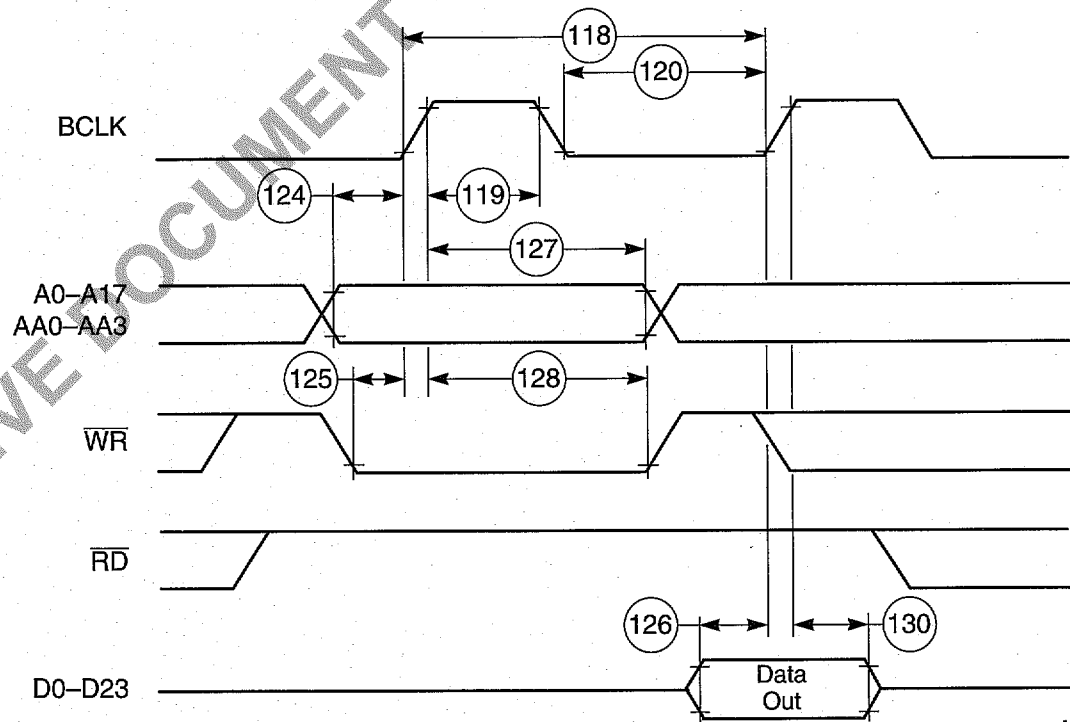


**Figure 2-15** SSRAM Write Access

**Preliminary Data**
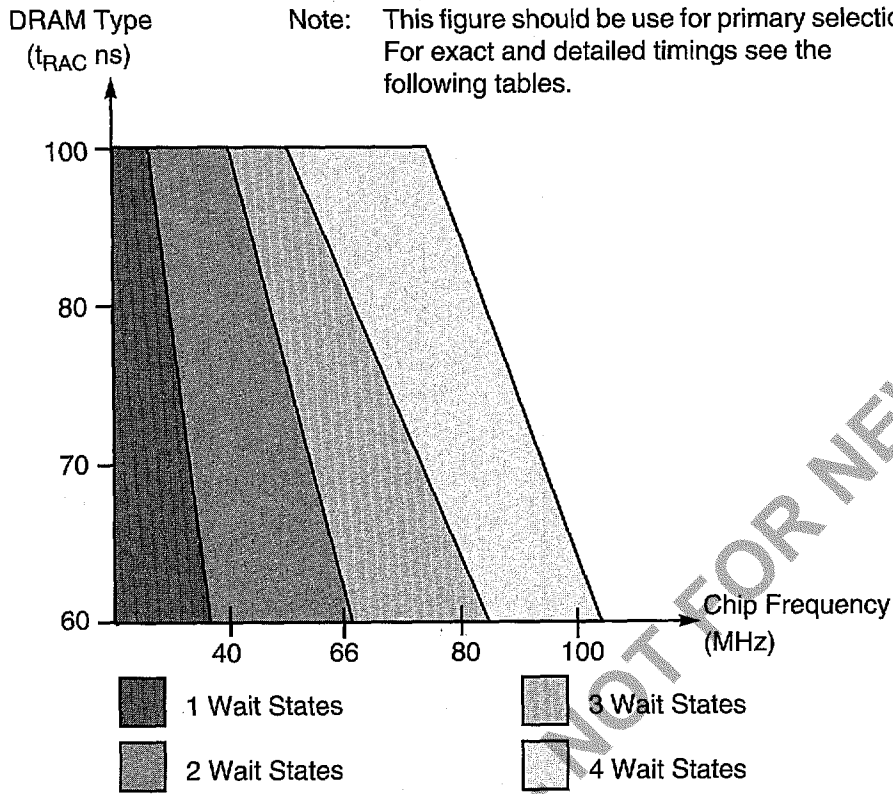
**Figure 2-16** DRAM Page Mode Wait States Selection Guide

**Table 2-10** DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 20 MHz[6] | | 30 MHz[6] | | Unit |
|-----|-----------------|--------|------------|-----------|-----|-----------|-----|------|
| | | | | Min | Max | Min | Max | |
| 131 | Page mode cycle time | $t_{PC}$ | $1.25 \times T_C$ | 62.5 | — | 41.7 | — | ns |
| 132 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | $T_C - 7.5$ | — | 42.5 | — | 25.8 | ns |
| 133 | Column address valid to data valid (read) | $t_{AA}$ | $1.5 \times T_C - 7.5$ | — | 67.5 | — | 42.5 | ns |
| 134 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 135 | Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $0.75 \times T_C - 4.0$ | 33.5 | — | 21.0 | — | ns |
| 136 | Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion | $t_{RHCP}$ | $2 \times T_C - 4.0$ | 96.0 | — | 62.7 | — | ns |
| 137 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $0.75 \times T_C - 4.0$ | 33.5 | — | 21.0 | — | ns |

**Preliminary Data**

**Table 2-10** DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 20 MHz[6] | | 30 MHz[6] | | Unit |
|-----|-----------------|--------|------------|-----|-----|-----|-----|------|
| | | | | Min | Max | Min | Max | |
| 138 | Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[4] | $t_{CRP}$ | | | | | | |
| | • BRW[1:0] = 00 | | $1.75 \times T_C - 6.0$ | 81.5 | — | 52.3 | — | ns |
| | • BRW[1:0] = 01 | | $3.25 \times T_C - 6.0$ | 156.5 | — | 102.2 | — | ns |
| | • BRW[1:0] = 10 | | $4.25 \times T_C - 6.0$ | 206.5 | — | 135.5 | — | ns |
| | • BRW[1:0] = 11 | | $6.25 \times T_C - 6.0$ | 306.5 | — | 202.1 | — | ns |
| 139 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $0.5 \times T_C - 4.0$ | 21.0 | — | 12.7 | — | ns |
| 140 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $0.5 \times T_C - 4.0$ | 21.0 | — | 12.7 | — | ns |
| 141 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $0.75 \times T_C - 4.0$ | 33.5 | — | 21.0 | — | ns |
| 142 | Last column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $2 \times T_C - 4.0$ | 96.0 | — | 62.7 | — | ns |
| 143 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $0.75 \times T_C - 3.8$ | 33.7 | — | 21.2 | — | ns |
| 144 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $0.25 \times T_C - 3.7$ | 8.8 | — | 4.6 | — | ns |
| 145 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $0.5 \times T_C - 4.2$ | 20.8 | — | 12.5 | — | ns |
| 146 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $1.5 \times T_C - 4.5$ | 70.5 | — | 45.5 | — | ns |
| 147 | Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $1.75 \times T_C - 4.3$ | 83.2 | — | 54.0 | — | ns |
| 148 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $1.75 \times T_C - 4.3$ | 83.2 | — | 54.0 | — | ns |
| 149 | Data valid to $\overline{CAS}$ assertion (Write) | $t_{DS}$ | $0.25 \times T_C - 4.0$ | 8.5 | — | 4.3 | — | ns |
| 150 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $0.75 \times T_C - 4.0$ | 33.5 | — | 21.0 | — | ns |
| 151 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $T_C - 4.3$ | 45.7 | — | 29.0 | — | ns |
| 152 | Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $1.5 \times T_C - 4.0$ | 71.0 | — | 46.0 | — | ns |

**Preliminary Data**

**Table 2-10**  DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 20 MHz[6] | | 30 MHz[6] | | Unit |
|-----|-----------------|--------|------------|-----|-----|-----|-----|------|
| | | | | Min | Max | Min | Max | |
| 153 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | $T_C - 7.5$ | — | 42.5 | — | 25.8 | ns |
| 154 | $\overline{RD}$ deassertion to data not valid [5] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 155 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 37.2 | — | 24.7 | — | ns |
| 156 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 12.5 | — | 8.3 | ns |

Note:
1. The number of wait states for page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., $t_{PC}$ equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
5. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.
6. Reduced DSP clock speed allows use of Page Mode DRAM with one wait state (See **Figure 2-16**.).

**Table 2-11**  DRAM Page Mode Timings, Two Wait States[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|-----|-----|-----|-----|------|
| | | | | Min | Max | Min | Max | |
| 131 | Page mode cycle time | $t_{PC}$ | $2.75 \times T_C$ | 41.7 | — | 34.4 | — | ns |
| 132 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $1.5 \times T_C - 7.5$ | — | 15.2 | — | — | ns |
| | | | **80 MHz:** $1.5 \times T_C - 6.5$ | — | — | — | 12.3 | ns |
| 133 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $2.5 \times T_C - 7.5$ | — | 30.4 | — | — | ns |
| | | | **80 MHz:** $2.5 \times T_C - 6.5$ | — | — | — | 24.8 | ns |
| 134 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 135 | Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 136 | Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion | $t_{RHCP}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |

**Preliminary Data**

**Table 2-11** DRAM Page Mode Timings, Two Wait States[1, 2, 3] (Continued)

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 137 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $1.5 \times T_C - 4.0$ | 18.7 | — | 14.8 | — | ns |
| 138 | Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] | $t_{CRP}$ | | | | | | |
| | • BRW[1:0] = 00 | | $2.0 \times T_C - 6.0$ | 24.4 | — | 19.0 | — | ns |
| | • BRW[1:0] = 01 | | $3.5 \times T_C - 6.0$ | 47.2 | — | 37.8 | — | ns |
| | • BRW[1:0] = 10 | | $4.5 \times T_C - 6.0$ | 62.4 | — | 50.3 | — | ns |
| | • BRW[1:0] = 11 | | $6.5 \times T_C - 6.0$ | 92.8 | — | 75.3 | — | ns |
| 139 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $1.25 \times T_C - 4.0$ | 14.9 | — | 11.6 | — | ns |
| 140 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $T_C - 4.0$ | 11.2 | — | 8.5 | — | ns |
| 141 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 142 | Last column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $3 \times T_C - 4.0$ | 41.5 | — | 33.5 | — | ns |
| 143 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $1.25 \times T_C - 3.8$ | 15.1 | — | 11.8 | — | ns |
| 144 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $0.5 \times T_C - 3.7$ | 3.9 | — | 2.6 | — | ns |
| 145 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $1.5 \times T_C - 4.2$ | 18.5 | — | 14.6 | — | ns |
| 146 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $2.5 \times T_C - 4.5$ | 33.4 | — | 26.8 | — | ns |
| 147 | Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $2.75 \times T_C - 4.3$ | 37.4 | — | 30.1 | — | ns |
| 148 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $2.5 \times T_C - 4.3$ | 33.6 | — | 27.0 | — | ns |

**Preliminary Data**

**Table 2-11** DRAM Page Mode Timings, Two Wait States[1, 2, 3] (Continued)

| No. | Characteristics | Symbol | Expression | 66 MHz Min | 66 MHz Max | 80 MHz Min | 80 MHz Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 149 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | **66 MHz:** $0.25 \times T_C - 3.7$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ | | — | 0.1 | — | ns |
| 150 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 151 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $T_C - 4.3$ | 10.9 | — | 8.2 | — | ns |
| 152 | Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $2.5 \times T_C - 4.0$ | 33.9 | — | 27.3 | — | ns |
| 153 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | $1.75 \times T_C - 7.5$ | — | 19.0 | — | 15.4 | ns |
| 154 | $\overline{RD}$ deassertion to data not valid[6] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 155 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |
| 156 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note:
1. The number of wait states for page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56304.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., $t_{PC}$ equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.

**Preliminary Data**

**Table 2-12** DRAM Page Mode Timings, Three Wait States[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 131 | Page mode cycle time | $t_{PC}$ | $3.5 \times T_C$ | 53.0 | — | 43.8 | | ns |
| 132 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $2 \times T_C - 7.5$ | — | 22.8 | — | — | ns |
| | | | **80 MHz:** $2 \times T_C - 6.5$ | — | | — | 18.5 | ns |
| 133 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $3 \times T_C - 7.5$ | — | 37.9 | — | — | ns |
| | | | **80 MHz:** $3 \times T_C - 6.5$ | — | | — | 31.0 | ns |
| 134 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 135 | Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $2.5 \times T_C - 4.0$ | 33.9 | — | 27.3 | — | ns |
| 136 | Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion | $t_{RHCP}$ | $4.5 \times T_C - 4.0$ | 64.2 | — | 52.3 | — | ns |
| 137 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $2 \times T_C - 4.0$ | 26.3 | — | 21.0 | — | ns |
| 138 | Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] | $t_{CRP}$ | | | | | | |
| | • BRW[1:0] = 00 | | $2.25 \times T_C - 6.0$ | 28.2 | — | 22.2 | — | ns |
| | • BRW[1:0] = 01 | | $3.75 \times T_C - 6.0$ | 51.0 | — | 40.9 | — | ns |
| | • BRW[1:0] = 10 | | $4.75 \times T_C - 6.0$ | 66.2 | — | 53.4 | — | ns |
| | • BRW[1:0] = 11 | | $6.75 \times T_C - 6.0$ | 96.6 | — | 78.4 | — | ns |
| 139 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $1.5 \times T_C - 4.0$ | 18.7 | — | 14.8 | — | ns |
| 140 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $T_C - 4.0$ | 11.2 | — | 8.5 | — | ns |
| 141 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $2.5 \times T_C - 4.0$ | 33.9 | — | 27.3 | — | ns |
| 142 | Last column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $4 \times T_C - 4.0$ | 56.6 | — | 46.0 | — | ns |

**Preliminary Data**

**Table 2-12** DRAM Page Mode Timings, Three Wait States[1, 2, 3] (Continued)

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 143 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $1.25 \times T_C - 3.8$ | 15.1 | — | 11.8 | — | ns |
| 144 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $0.75 \times T_C - 3.7$ | 7.7 | — | 5.7 | — | ns |
| 145 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $2.25 \times T_C - 4.2$ | 29.9 | — | 23.9 | — | ns |
| 146 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $3.5 \times T_C - 4.5$ | 48.5 | — | 39.3 | — | ns |
| 147 | Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $3.75 \times T_C - 4.3$ | 52.5 | — | 42.6 | — | ns |
| 148 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $3.25 \times T_C - 4.3$ | 44.9 | — | 36.3 | — | ns |
| 149 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | $0.5 \times T_C - 4.0$ | 3.6 | — | 2.3 | — | ns |
| 150 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $2.5 \times T_C - 4.0$ | 33.9 | — | 27.3 | — | ns |
| 151 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $1.25 \times T_C - 4.3$ | 14.6 | — | 11.3 | — | ns |
| 152 | Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $3.5 \times T_C - 4.0$ | 49.0 | — | 39.8 | — | ns |
| 153 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | **66 MHz:** $2.5 \times T_C - 7.5$ | — | 30.4 | — | — | ns |
| | | | **80 MHz:** $2.5 \times T_C - 6.5$ | — | — | — | 24.8 | ns |
| 154 | $\overline{RD}$ deassertion to data not valid[6] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 155 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |
| 156 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note: 1. The number of wait states for page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56304.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., $t_{PC}$ equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.

**Preliminary Data**

**Table 2-13**  DRAM Page Mode Timings, Four Wait States[1, 2, 3]

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|--------|--------|--------|--------|------|
| | | | | Min | Max | Min | Max | |
| 131 | Page mode cycle time | $t_{PC}$ | $4.5 \times T_C$ | 68.2 | — | 56.3 | — | ns |
| 132 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $2.75 \times T_C - 7.5$ | — | 34.2 | — | — | ns |
| | | | **80 MHz:** $2.75 \times T_C - 6.5$ | — | | — | 27.9 | ns |
| 133 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $3.75 \times T_C - 7.5$ | — | 49.3 | — | — | ns |
| | | | **80 MHz:** $3.75 \times T_C - 6.5$ | — | — | — | 40.4 | ns |
| 134 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 135 | Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $3.5 \times T_C - 4.0$ | 49.0 | — | 39.8 | — | ns |
| 136 | Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion | $t_{RHCP}$ | $6 \times T_C - 4.0$ | 86.9 | — | 71.0 | — | ns |
| 137 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $2.5 \times T_C - 4.0$ | 33.9 | — | 27.3 | — | ns |
| 138 | Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] | $t_{CRP}$ | | | | | | |
| | • BRW[1:0] = 00 | | $2.75 \times T_C - 6.0$ | 35.8 | — | 28.4 | — | ns |
| | • BRW[1:0] = 01 | | $4.25 \times T_C - 6.0$ | 58.6 | — | 47.2 | — | ns |
| | • BRW[1:0] = 10 | | $5.25 \times T_C - 6.0$ | 73.8 | — | 59.7 | — | ns |
| | • BRW[1:0] = 11 | | $6.25 \times T_C - 6.0$ | 89.0 | — | 72.2 | — | ns |
| 139 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $2 \times T_C - 4.0$ | 26.3 | — | 21.0 | — | ns |
| 140 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $T_C - 4.0$ | 11.2 | — | 8.5 | — | ns |

**Preliminary Data**

Table 2-13   DRAM Page Mode Timings, Four Wait States[1, 2, 3] (Continued)

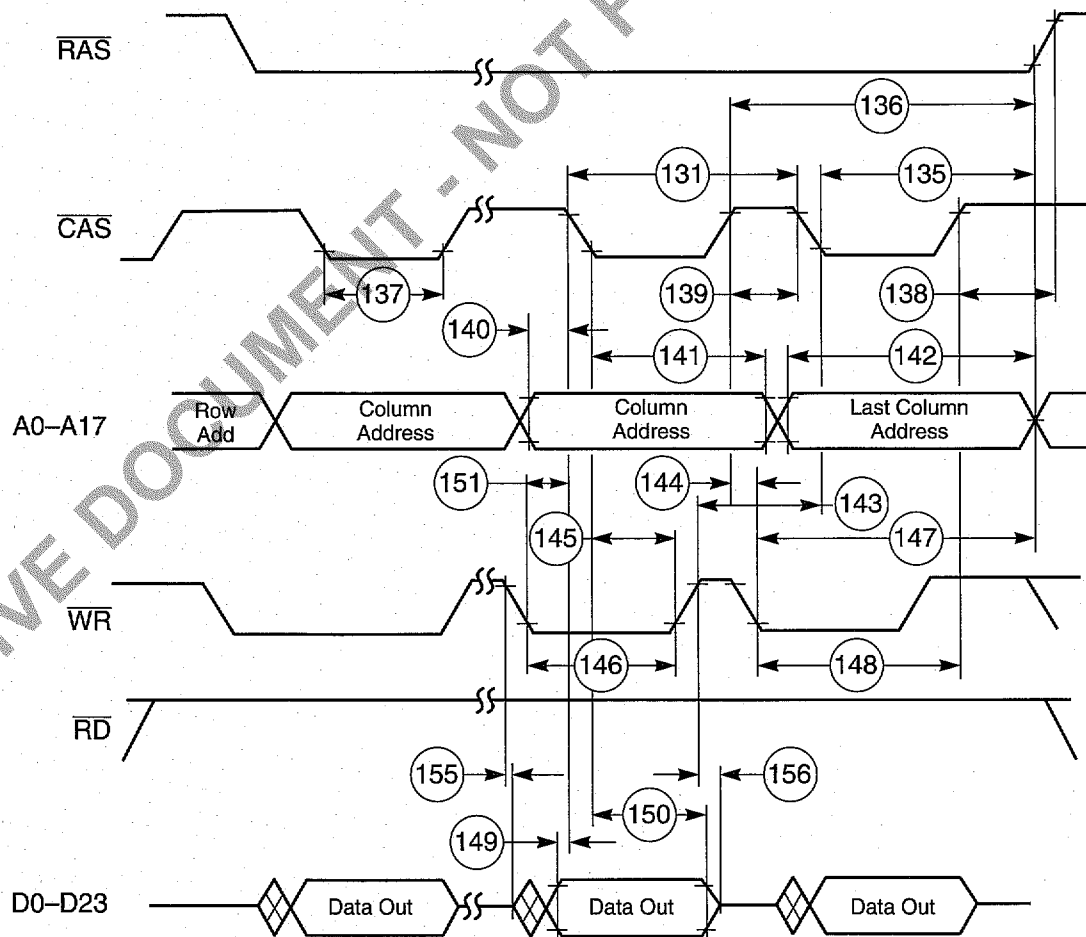| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|----------------|--------|-----------|--------|--------|--------|--------|------|
| | | | | Min | Max | Min | Max | |
| 141 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $3.5 \times T_C - 4.0$ | 49.0 | — | 39.8 | — | ns |
| 142 | Last column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $5 \times T_C - 4.0$ | 71.8 | — | 58.5 | — | ns |
| 143 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $1.25 \times T_C - 3.8$ | 15.1 | — | 11.8 | — | ns |
| 144 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $1.25 \times T_C - 3.7$ | 15.2 | — | 11.9 | — | ns |
| 145 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $3.25 \times T_C - 4.2$ | 45.0 | — | 36.4 | — | ns |
| 146 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $4.5 \times T_C - 4.5$ | 63.7 | — | 51.8 | — | ns |
| 147 | Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $4.75 \times T_C - 4.3$ | 67.7 | — | 55.1 | — | ns |
| 148 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $3.75 \times T_C - 4.3$ | 52.5 | — | 42.6 | — | ns |
| 149 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | $0.5 \times T_C - 4.0$ | 3.6 | — | 2.3 | — | ns |
| 150 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $3.5 \times T_C - 4.0$ | 49.0 | — | 39.8 | — | ns |
| 151 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $1.25 \times T_C - 4.3$ | 14.6 | — | 11.3 | — | ns |
| 152 | Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $4.5 \times T_C - 4.0$ | 64.2 | — | 52.3 | — | ns |
| 153 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | **66 MHz:** $3.25 \times T_C - 7.5$ | — | 41.7 | — | — | ns |
| | | | **80 MHz:** $3.25 \times T_C - 6.5$ | — | — | — | 34.1 | ns |
| 154 | $\overline{RD}$ deassertion to data not valid[6] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 155 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |

**Preliminary Data**

**Table 2-13** DRAM Page Mode Timings, Four Wait States[1, 2, 3] (Continued)

| No. | Characteristics | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 156 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note:
1. The number of wait states for page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56304.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., $t_{PC}$ equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.



**Figure 2-17** DRAM Page Mode Write Accesses

**Preliminary Data**
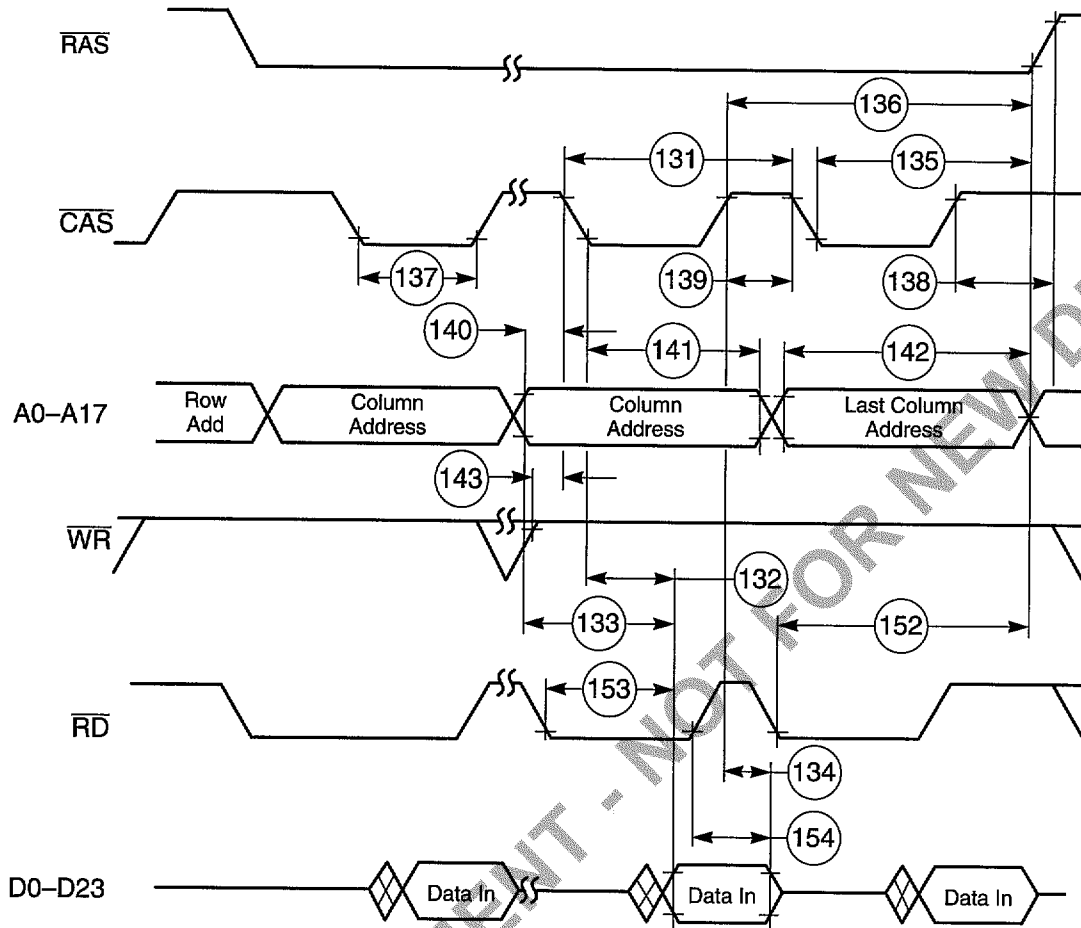
**Figure 2-18** DRAM Page Mode Read Accesses
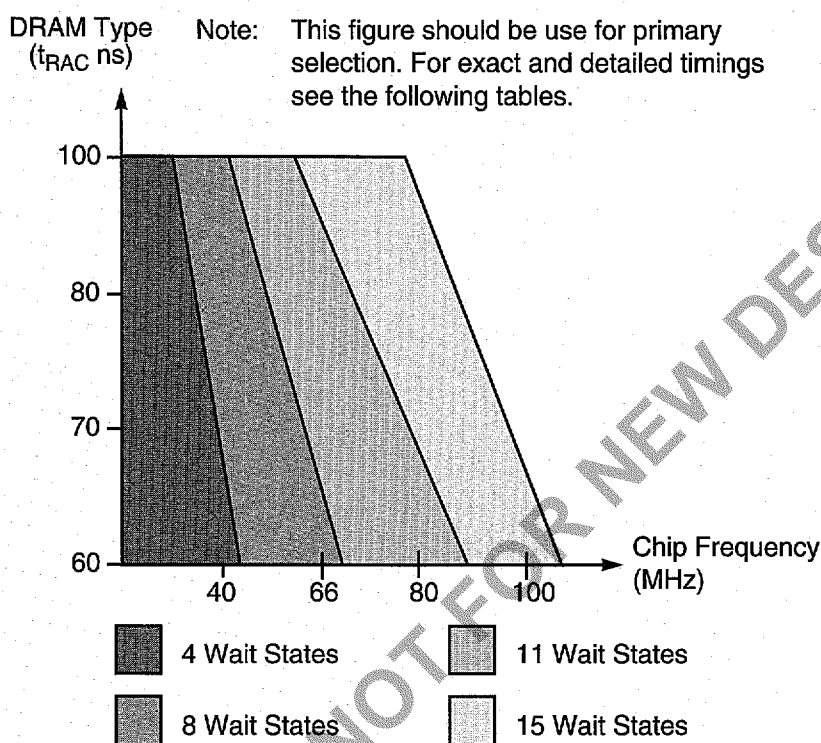
**Figure 2-19** DRAM Out-of-Page Wait States Selection Guide

**Table 2-14** DRAM Out-of-Page and Refresh Timings, Four Wait States[1,2]

| No. | Characteristics[3] | Symbol | Expression | 20 MHz[4] | | 30 MHz[4] | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 157 | Random read or write cycle time | $t_{RC}$ | $5 \times T_C$ | 250.0 | — | 166.7 | — | ns |
| 158 | $\overline{RAS}$ assertion to data valid (read) | $t_{RAC}$ | $2.75 \times T_C - 7.5$ | — | 130.0 | — | 84.2 | ns |
| 159 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | $1.25 \times T_C - 7.5$ | — | 55.0 | — | 34.2 | ns |
| 160 | Column address valid to data valid (read) | $t_{AA}$ | $1.5 \times T_C - 7.5$ | — | 67.5 | — | 42.5 | ns |
| 161 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 162 | $\overline{RAS}$ deassertion to $\overline{RAS}$ assertion | $t_{RP}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 163 | $\overline{RAS}$ assertion pulse width | $t_{RAS}$ | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |

**Preliminary Data**

**Table 2-14** DRAM Out-of-Page and Refresh Timings, Four Wait States[1,2] (Continued)

| No. | Characteristics[3] | Symbol | Expression | 20 MHz[4] | | 30 MHz[4] | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 164 | $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 165 | $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion | $t_{CSH}$ | $2.75 \times T_C - 4.0$ | 133.5 | — | 87.7 | — | ns |
| 166 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |
| 167 | $\overline{RAS}$ assertion to $\overline{CAS}$ assertion | $t_{RCD}$ | $1.5 \times T_C \pm 2$ | 73.0 | 77.0 | 48.0 | 52.0 | ns |
| 168 | $\overline{RAS}$ assertion to column address valid | $t_{RAD}$ | $1.25 \times T_C \pm 2$ | 60.5 | 64.5 | 39.7 | 43.7 | ns |
| 169 | $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion | $t_{CRP}$ | $2.25 \times T_C - 4.0$ | 108.5 | — | 71.0 | — | ns |
| 170 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 171 | Row address valid to $\overline{RAS}$ assertion | $t_{ASR}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 172 | $\overline{RAS}$ assertion to row address not valid | $t_{RAH}$ | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |
| 173 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $0.25 \times T_C - 4.0$ | 8.5 | — | 4.3 | — | ns |
| 174 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 175 | $\overline{RAS}$ assertion to column address not valid | $t_{AR}$ | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |
| 176 | Column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $2 \times T_C - 4.0$ | 96.0 | — | 62.7 | — | ns |
| 177 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $1.5 \times T_C - 3.8$ | 71.2 | — | 46.2 | — | ns |
| 178 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $0.75 \times T_C - 3.7$ | 33.8 | — | 21.3 | — | ns |
| 179 | $\overline{RAS}$ deassertion to $\overline{WR}$ assertion | $t_{RRH}$ | $0.25 \times T_C - 3.7$ | 8.8 | — | 4.6 | — | ns |
| 180 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $1.5 \times T_C - 4.2$ | 70.8 | — | 45.8 | — | ns |

**Preliminary Data**

Table 2-14  DRAM Out-of-Page and Refresh Timings, Four Wait States[1,2] (Continued)

| No. | Characteristics[3] | Symbol | Expression | 20 MHz[4] | | 30 MHz[4] | | Unit |
|-----|-------------------|--------|------------|-----|-----|-----|-----|------|
| | | | | Min | Max | Min | Max | |
| 181 | $\overline{RAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCR}$ | $3 \times T_C - 4.2$ | 145.8 | — | 95.8 | — | ns |
| 182 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $4.5 \times T_C - 4.5$ | 220.5 | — | 145.5 | — | ns |
| 183 | $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $4.75 \times T_C - 4.3$ | 233.2 | — | 154.0 | — | ns |
| 184 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $4.25 \times T_C - 4.3$ | 208.2 | — | 137.4 | — | ns |
| 185 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | $2.25 \times T_C - 4.0$ | 108.5 | — | 71.0 | — | ns |
| 186 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 187 | $\overline{RAS}$ assertion to data not valid (write) | $t_{DHR}$ | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |
| 188 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $3 \times T_C - 4.3$ | 145.7 | — | 95.7 | — | ns |
| 189 | $\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh) | $t_{CSR}$ | $0.5 \times T_C - 4.0$ | 21.0 | — | 12.7 | — | ns |
| 190 | $\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh) | $t_{RPC}$ | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |
| 191 | $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $4.5 \times T_C - 4.0$ | 221.0 | — | 146.0 | — | ns |
| 192 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | $4 \times T_C - 7.5$ | — | 192.5 | — | 125.8 | ns |
| 193 | $\overline{RD}$ deassertion to data not valid[3] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 194 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 37.2 | — | 24.7 | — | ns |
| 195 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 12.5 | — | 8.3 | ns |

Note:  1.  The number of wait states for out of page access is specified in the DCR.
2.  The refresh period is specified in the DCR.
3.  $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.
4.  Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (See **Figure 2-19**.).

**Preliminary Data**

Table 2-15  DRAM Out-of-Page and Refresh Timings, Eight Wait States[1,2]

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 157 | Random read or write cycle time | $t_{RC}$ | $9 \times T_C$ | 136.4 | — | 112.5 | — | ns |
| 158 | $\overline{RAS}$ assertion to data valid (read) | $t_{RAC}$ | **66 MHz:** $4.75 \times T_C - 7.5$ | — | 64.5 | — | — | ns |
| | | | **80 MHz:** $4.75 \times T_C - 6.5$ | — | — | — | 52.9 | ns |
| 159 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $2.25 \times T_C - 7.5$ | — | 26.6 | — | — | ns |
| | | | **80 MHz:** $2.25 \times T_C - 6.5$ | — | — | — | 21.6 | ns |
| 160 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $3 \times T_C - 7.5$ | — | 40.0 | — | — | ns |
| | | | **80 MHz:** $3 \times T_C - 6.5$ | — | — | — | 31.0 | ns |
| 161 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 162 | $\overline{RAS}$ deassertion to $\overline{RAS}$ assertion | $t_{RP}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |
| 163 | $\overline{RAS}$ assertion pulse width | $t_{RAS}$ | $5.75 \times T_C - 4.0$ | 83.1 | — | 67.9 | — | ns |
| 164 | $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |
| 165 | $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion | $t_{CSH}$ | $4.75 \times T_C - 4.0$ | 68.0 | — | 55.4 | — | ns |
| 166 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $2.25 \times T_C - 4.0$ | 30.1 | — | 24.1 | — | ns |
| 167 | $\overline{RAS}$ assertion to $\overline{CAS}$ assertion | $t_{RCD}$ | $2.5 \times T_C \pm 2$ | 35.9 | 39.9 | 29.3 | 33.3 | ns |
| 168 | $\overline{RAS}$ assertion to column address valid | $t_{RAD}$ | $1.75 \times T_C \pm 2$ | 24.5 | 28.5 | 19.9 | 23.9 | ns |
| 169 | $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion | $t_{CRP}$ | $4.25 \times T_C - 4.0$ | 59.8 | — | 49.1 | — | ns |
| 170 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $2.75 \times T_C - 4.0$ | 37.7 | — | 30.4 | — | ns |

**Preliminary Data**

**Table 2-15** DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|--------|---------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 171 | Row address valid to $\overline{\text{RAS}}$ assertion | $t_{ASR}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |
| 172 | $\overline{\text{RAS}}$ assertion to row address not valid | $t_{RAH}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 173 | Column address valid to $\overline{\text{CAS}}$ assertion | $t_{ASC}$ | $0.75 \times T_C - 4.0$ | 7.4 | — | 5.4 | — | ns |
| 174 | $\overline{\text{CAS}}$ assertion to column address not valid | $t_{CAH}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |
| 175 | $\overline{\text{RAS}}$ assertion to column address not valid | $t_{AR}$ | $5.75 \times T_C - 4.0$ | 83.1 | — | 67.9 | — | ns |
| 176 | Column address valid to $\overline{\text{RAS}}$ deassertion | $t_{RAL}$ | $4 \times T_C - 4.0$ | 56.6 | — | 46.0 | — | ns |
| 177 | $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion | $t_{RCS}$ | $2 \times T_C - 3.8$ | 26.5 | — | 21.2 | — | ns |
| 178 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion | $t_{RCH}$ | $1.25 \times T_C - 3.7$ | 15.2 | — | 11.9 | — | ns |
| 179 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$ assertion | $t_{RRH}$ | **66 MHz:** $0.25 \times T_C - 3.7$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ | — | — | 0.1 | — | ns |
| 180 | $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion | $t_{WCH}$ | $3 \times T_C - 4.2$ | 41.3 | — | 33.3 | — | ns |
| 181 | $\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion | $t_{WCR}$ | $5.5 \times T_C - 4.2$ | 79.1 | — | 64.6 | — | ns |
| 182 | $\overline{\text{WR}}$ assertion pulse width | $t_{WP}$ | $8.5 \times T_C - 4.5$ | 124.3 | — | 101.8 | — | ns |
| 183 | $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion | $t_{RWL}$ | $8.75 \times T_C - 4.3$ | 128.3 | — | 105.1 | — | ns |
| 184 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion | $t_{CWL}$ | $7.75 \times T_C - 4.3$ | 113.1 | — | 92.6 | — | ns |
| 185 | Data valid to $\overline{\text{CAS}}$ assertion (write) | $t_{DS}$ | $4.75 \times T_C - 4.0$ | 68.0 | — | 55.4 | — | ns |

**Preliminary Data**

**Table 2-15** DRAM Out-of-Page and Refresh Timings, Eight Wait States[1,2] (Continued)

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|--------|---------------|--------|--------|--------|--------|------|
| | | | | Min | Max | Min | Max | |
| 186 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $3.25 \times T_C - 4.0$ | 45.2 | — | 36.6 | — | ns |
| 187 | $\overline{RAS}$ assertion to data not valid (write) | $t_{DHR}$ | $5.75 \times T_C - 4.0$ | 83.1 | — | 67.9 | — | ns |
| 188 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $5.5 \times T_C - 4.3$ | 79.0 | — | 64.5 | — | ns |
| 189 | $\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh) | $t_{CSR}$ | $1.5 \times T_C - 4.0$ | 18.7 | — | 14.8 | — | ns |
| 190 | $\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh) | $t_{RPC}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 191 | $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $8.5 \times T_C - 4.0$ | 124.8 | — | 102.3 | — | ns |
| 192 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | **66 MHz:** $7.5 \times T_C - 7.5$ | — | 106.1 | | | ns |
| | | | **80 MHz:** $7.5 \times T_C - 6.5$ | | | — | 87.3 | ns |
| 193 | $\overline{RD}$ deassertion to data not valid[4] | $t_{GZ}$ | 0.0 | 0.0 | — | 0.0 | — | ns |
| 194 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |
| 195 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56304.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.

**Preliminary Data**

**Table 2-16** DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2]

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 157 | Random read or write cycle time | $t_{RC}$ | $12 \times T_C$ | 181.8 | — | 150.0 | — | ns |
| 158 | $\overline{RAS}$ assertion to data valid (read) | $t_{RAC}$ | **66 MHz:** $6.25 \times T_C - 7.5$ | — | 87.2 | — | — | ns |
| | | | **80 MHz:** $6.25 \times T_C - 6.5$ | — | — | — | 71.6 | ns |
| 159 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $3.75 \times T_C - 7.5$ | — | 49.3 | — | — | ns |
| | | | **80 MHz:** $3.75 \times T_C - 6.5$ | — | — | — | 40.4 | ns |
| 160 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $4.5 \times T_C - 7.5$ | — | 60.7 | — | — | ns |
| | | | **80 MHz:** $4.5 \times T_C - 6.5$ | — | — | — | 49.8 | ns |
| 161 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | | 0.0 | — | 0.0 | — | ns |
| 162 | $\overline{RAS}$ deassertion to $\overline{RAS}$ assertion | $t_{RP}$ | $4.25 \times T_C - 4.0$ | 60.4 | — | 49.1 | — | ns |
| 163 | $\overline{RAS}$ assertion pulse width | $t_{RAS}$ | $7.75 \times T_C - 4.0$ | 113.4 | — | 92.9 | — | ns |
| 164 | $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $5.25 \times T_C - 4.0$ | 75.5 | — | 61.6 | — | ns |
| 165 | $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion | $t_{CSH}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |
| 166 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $3.75 \times T_C - 4.0$ | 52.8 | — | 42.9 | — | ns |
| 167 | $\overline{RAS}$ assertion to $\overline{CAS}$ assertion | $t_{RCD}$ | $2.5 \times T_C \pm 2$ | 35.9 | 39.9 | 29.3 | 33.3 | ns |
| 168 | $\overline{RAS}$ assertion to column address valid | $t_{RAD}$ | $1.75 \times T_C \pm 2$ | 24.5 | 28.5 | 19.9 | 23.9 | ns |
| 169 | $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion | $t_{CRP}$ | $5.75 \times T_C - 4.0$ | 83.1 | — | 67.9 | — | ns |
| 170 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $4.25 \times T_C - 4.0$ | 60.4 | — | 49.1 | — | ns |

**Preliminary Data**

**Table 2-16** DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 171 | Row address valid to $\overline{RAS}$ assertion | $t_{ASR}$ | $4.25 \times T_C - 4.0$ | 60.4 | — | 49.1 | — | ns |
| 172 | $\overline{RAS}$ assertion to row address not valid | $t_{RAH}$ | $1.75 \times T_C - 4.0$ | 22.5 | — | 17.9 | — | ns |
| 173 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $0.75 \times T_C - 4.0$ | 7.4 | — | 5.4 | — | ns |
| 174 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $5.25 \times T_C - 4.0$ | 75.5 | — | 61.6 | — | ns |
| 175 | $\overline{RAS}$ assertion to column address not valid | $t_{AR}$ | $7.75 \times T_C - 4.0$ | 113.4 | — | 92.9 | — | ns |
| 176 | Column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $6 \times T_C - 4.0$ | 86.9 | — | 71.0 | — | ns |
| 177 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $3.0 \times T_C - 3.8$ | 41.7 | — | 33.7 | — | ns |
| 178 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $1.75 \times T_C - 3.7$ | 22.8 | — | 18.2 | — | ns |
| 179 | $\overline{RAS}$ deassertion to $\overline{WR}$ assertion | $t_{RRH}$ | **66 MHz:** $0.25 \times T_C - 3.7$ | 0.1 | — | 0.1 | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ | 0.1 | — | 0.1 | — | ns |
| 180 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $5 \times T_C - 4.2$ | 71.6 | — | 58.3 | — | ns |
| 181 | $\overline{RAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCR}$ | $7.5 \times T_C - 4.2$ | 109.4 | — | 89.6 | — | ns |
| 182 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $11.5 \times T_C - 4.5$ | 169.7 | — | 139.3 | — | ns |
| 183 | $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $11.75 \times T_C - 4.3$ | 173.7 | — | 142.7 | — | ns |
| 184 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $10.25 \times T_C - 4.3$ | 151.0 | — | 130.1 | — | ns |
| 185 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | $5.75 \times T_C - 4.0$ | 83.1 | — | 67.9 | — | ns |

**Preliminary Data**

**Table 2-16** DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

| No. | Characteristics[4] | Symbol | Expression[3] | 66 MHz | | 80 MHz | | Unit |
|-----|---------------------|--------|---------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 186 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $5.25 \times T_C - 4.0$ | 75.5 | — | 61.6 | — | ns |
| 187 | $\overline{RAS}$ assertion to data not valid (write) | $t_{DHR}$ | $7.75 \times T_C - 4.0$ | 113.4 | — | 92.9 | — | ns |
| 188 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $6.5 \times T_C - 4.3$ | 94.2 | — | 77.0 | — | ns |
| 189 | $\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh) | $t_{CSR}$ | $1.5 \times T_C - 4.0$ | 18.7 | — | 14.8 | — | ns |
| 190 | $\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh) | $t_{RPC}$ | $2.75 \times T_C - 4.0$ | 37.7 | — | 30.4 | — | ns |
| 191 | $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $11.5 \times T_C - 4.0$ | 170.2 | — | 139.8 | — | ns |
| 192 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | **66 MHz:** $10 \times T_C - 7.5$ | — | 144.0 | — | — | ns |
| | | | **80 MHz:** $10 \times T_C - 6.5$ | — | — | — | 118.5 | ns |
| 193 | $\overline{RD}$ deassertion to data not valid[4] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 194 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |
| 195 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note: 
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56304.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.

**Preliminary Data**

Table 2-17   DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

| No. | Characteristics[3] | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|--------------------|--------|------------|--------|--------|--------|--------|------|
| | | | | Min | Max | Min | Max | |
| 157 | Random read or write cycle time | $t_{RC}$ | $16 \times T_C$ | 242.4 | — | 200.0 | — | ns |
| 158 | $\overline{RAS}$ assertion to data valid (read) | $t_{RAC}$ | **66 MHz:** $8.25 \times T_C - 7.5$ | — | 117.5 | — | — | ns |
| | | | **80 MHz:** $8.25 \times T_C - 6.5$ | — | — | — | 96.6 | ns |
| 159 | $\overline{CAS}$ assertion to data valid (read) | $t_{CAC}$ | **66 MHz:** $4.75 \times T_C - 7.5$ | — | 64.5 | — | — | ns |
| | | | **80 MHz:** $4.75 \times T_C - 6.5$ | — | — | — | 52.9 | ns |
| 160 | Column address valid to data valid (read) | $t_{AA}$ | **66 MHz:** $5.5 \times T_C - 7.5$ | — | 75.8 | — | — | ns |
| | | | **80 MHz:** $5.5 \times T_C - 6.5$ | — | — | — | 62.3 | ns |
| 161 | $\overline{CAS}$ deassertion to data not valid (read hold time) | $t_{OFF}$ | $0.0$ | 0.0 | — | 0.0 | — | ns |
| 162 | $\overline{RAS}$ deassertion to $\overline{RAS}$ assertion | $t_{RP}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |
| 163 | $\overline{RAS}$ assertion pulse width | $t_{RAS}$ | $9.75 \times T_C - 4.0$ | 143.7 | — | 117.9 | — | ns |
| 164 | $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion | $t_{RSH}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |
| 165 | $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion | $t_{CSH}$ | $8.25 \times T_C - 4.0$ | 121.0 | — | 99.1 | — | ns |
| 166 | $\overline{CAS}$ assertion pulse width | $t_{CAS}$ | $4.75 \times T_C - 4.0$ | 68.0 | — | 55.4 | — | ns |
| 167 | $\overline{RAS}$ assertion to $\overline{CAS}$ assertion | $t_{RCD}$ | $3.5 \times T_C \pm 2$ | 51.0 | 55.0 | 41.8 | 45.8 | ns |
| 168 | $\overline{RAS}$ assertion to column address valid | $t_{RAD}$ | $2.75 \times T_C \pm 2$ | 39.7 | 43.7 | 32.4 | 36.4 | ns |
| 169 | $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion | $t_{CRP}$ | $7.75 \times T_C - 4.0$ | 113.4 | — | 92.9 | — | ns |
| 170 | $\overline{CAS}$ deassertion pulse width | $t_{CP}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |

**Preliminary Data**

Table 2-17   DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1,2] (Continued)

| No. | Characteristics[3] | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 171 | Row address valid to $\overline{RAS}$ assertion | $t_{ASR}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |
| 172 | $\overline{RAS}$ assertion to row address not valid | $t_{RAH}$ | $2.75 \times T_C - 4.0$ | 37.7 | — | 30.4 | — | ns |
| 173 | Column address valid to $\overline{CAS}$ assertion | $t_{ASC}$ | $0.75 \times T_C - 4.0$ | 7.4 | — | 5.4 | — | ns |
| 174 | $\overline{CAS}$ assertion to column address not valid | $t_{CAH}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |
| 175 | $\overline{RAS}$ assertion to column address not valid | $t_{AR}$ | $9.75 \times T_C - 4.0$ | 143.7 | — | 117.9 | — | ns |
| 176 | Column address valid to $\overline{RAS}$ deassertion | $t_{RAL}$ | $7 \times T_C - 4.0$ | 102.1 | — | 83.5 | — | ns |
| 177 | $\overline{WR}$ deassertion to $\overline{CAS}$ assertion | $t_{RCS}$ | $5 \times T_C - 3.8$ | 72.0 | — | 58.7 | — | ns |
| 178 | $\overline{CAS}$ deassertion to $\overline{WR}$ assertion | $t_{RCH}$ | $1.75 \times T_C - 3.7$ | 22.8 | — | 18.1 | — | ns |
| 179 | $\overline{RAS}$ deassertion to $\overline{WR}$ assertion | $t_{RRH}$ | **66 MHz:** $0.25 \times T_C - 3.7$ | 0.1 | — | — | — | ns |
| | | | **80 MHz:** $0.25 \times T_C - 3.0$ | — | — | 0.1 | — | ns |
| 180 | $\overline{CAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCH}$ | $6 \times T_C - 4.2$ | 86.7 | — | 70.8 | — | ns |
| 181 | $\overline{RAS}$ assertion to $\overline{WR}$ deassertion | $t_{WCR}$ | $9.5 \times T_C - 4.2$ | 139.7 | — | 114.6 | — | ns |
| 182 | $\overline{WR}$ assertion pulse width | $t_{WP}$ | $15.5 \times T_C - 4.5$ | 230.3 | — | 189.3 | — | ns |
| 183 | $\overline{WR}$ assertion to $\overline{RAS}$ deassertion | $t_{RWL}$ | $15.75 \times T_C - 4.3$ | 234.3 | — | 192.6 | — | ns |
| 184 | $\overline{WR}$ assertion to $\overline{CAS}$ deassertion | $t_{CWL}$ | $14.25 \times T_C - 4.3$ | 211.6 | — | 180.1 | — | ns |
| 185 | Data valid to $\overline{CAS}$ assertion (write) | $t_{DS}$ | $8.75 \times T_C - 4.0$ | 128.6 | — | 105.4 | — | ns |
| 186 | $\overline{CAS}$ assertion to data not valid (write) | $t_{DH}$ | $6.25 \times T_C - 4.0$ | 90.7 | — | 74.1 | — | ns |

**Preliminary Data**

**Table 2-17**  DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

| No. | Characteristics[3] | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 187 | $\overline{RAS}$ assertion to data not valid (write) | $t_{DHR}$ | $9.75 \times T_C - 4.0$ | 143.7 | — | 117.9 | — | ns |
| 188 | $\overline{WR}$ assertion to $\overline{CAS}$ assertion | $t_{WCS}$ | $9.5 \times T_C - 4.3$ | 139.6 | — | 114.5 | — | ns |
| 189 | $\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh) | $t_{CSR}$ | $1.5 \times T_C - 4.0$ | 18.7 | — | 14.8 | — | ns |
| 190 | $\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh) | $t_{RPC}$ | $4.75 \times T_C - 4.0$ | 68.0 | — | 55.4 | — | ns |
| 191 | $\overline{RD}$ assertion to $\overline{RAS}$ deassertion | $t_{ROH}$ | $15.5 \times T_C - 4.0$ | 230.8 | — | 189.8 | — | ns |
| 192 | $\overline{RD}$ assertion to data valid | $t_{GA}$ | **66 MHz:** $14 \times T_C - 7.5$ | — | 204.6 | — | — | ns |
| | | | **80 MHz:** $14 \times T_C - 6.5$ | — | — | — | 168.5 | ns |
| 193 | $\overline{RD}$ deassertion to data not valid[3] | $t_{GZ}$ | | 0.0 | — | 0.0 | — | ns |
| 194 | $\overline{WR}$ assertion to data active | | $0.75 \times T_C - 0.3$ | 11.1 | — | 9.1 | — | ns |
| 195 | $\overline{WR}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 3.8 | — | 3.1 | ns |

Note:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is $t_{OFF}$ and not $t_{GZ}$.
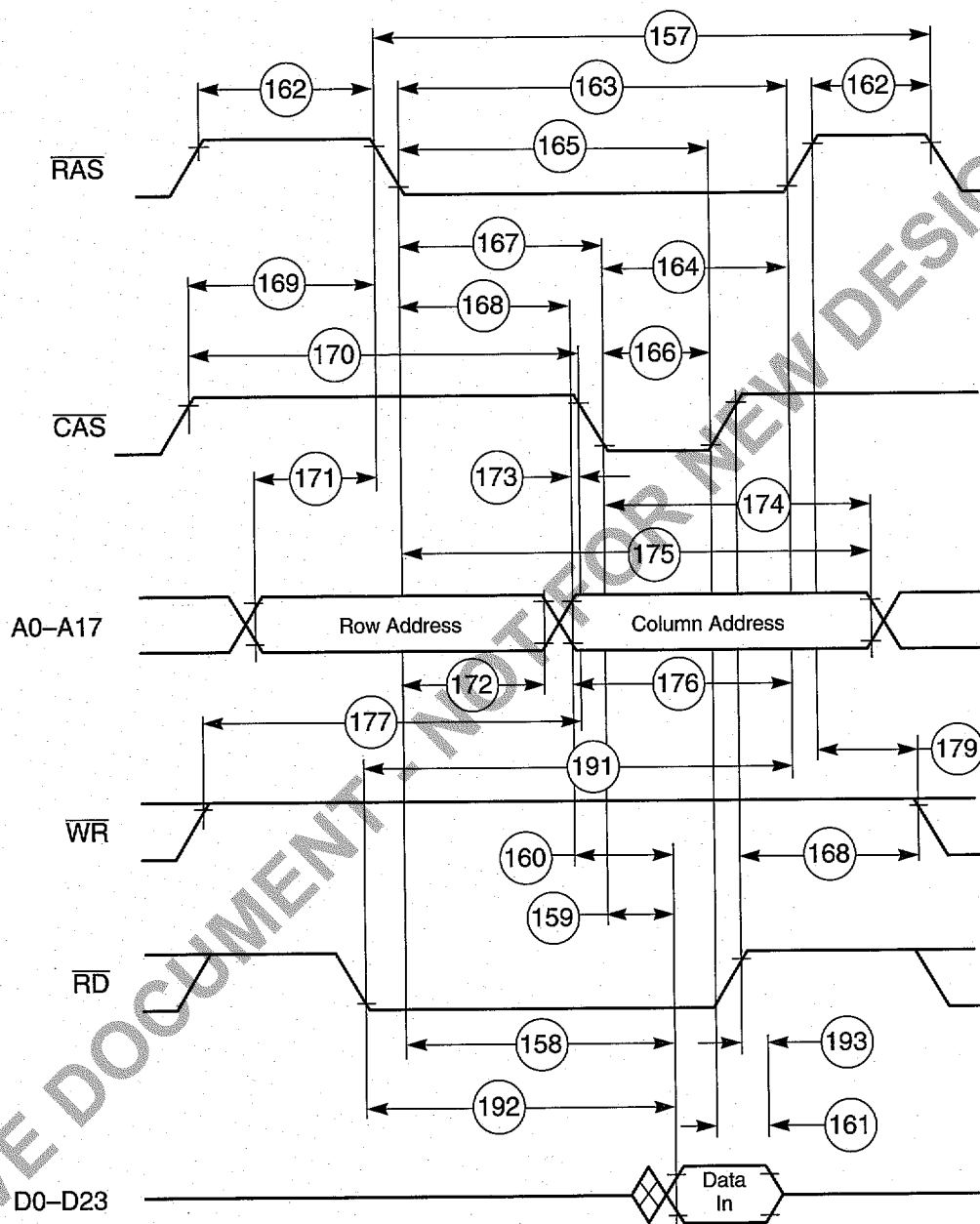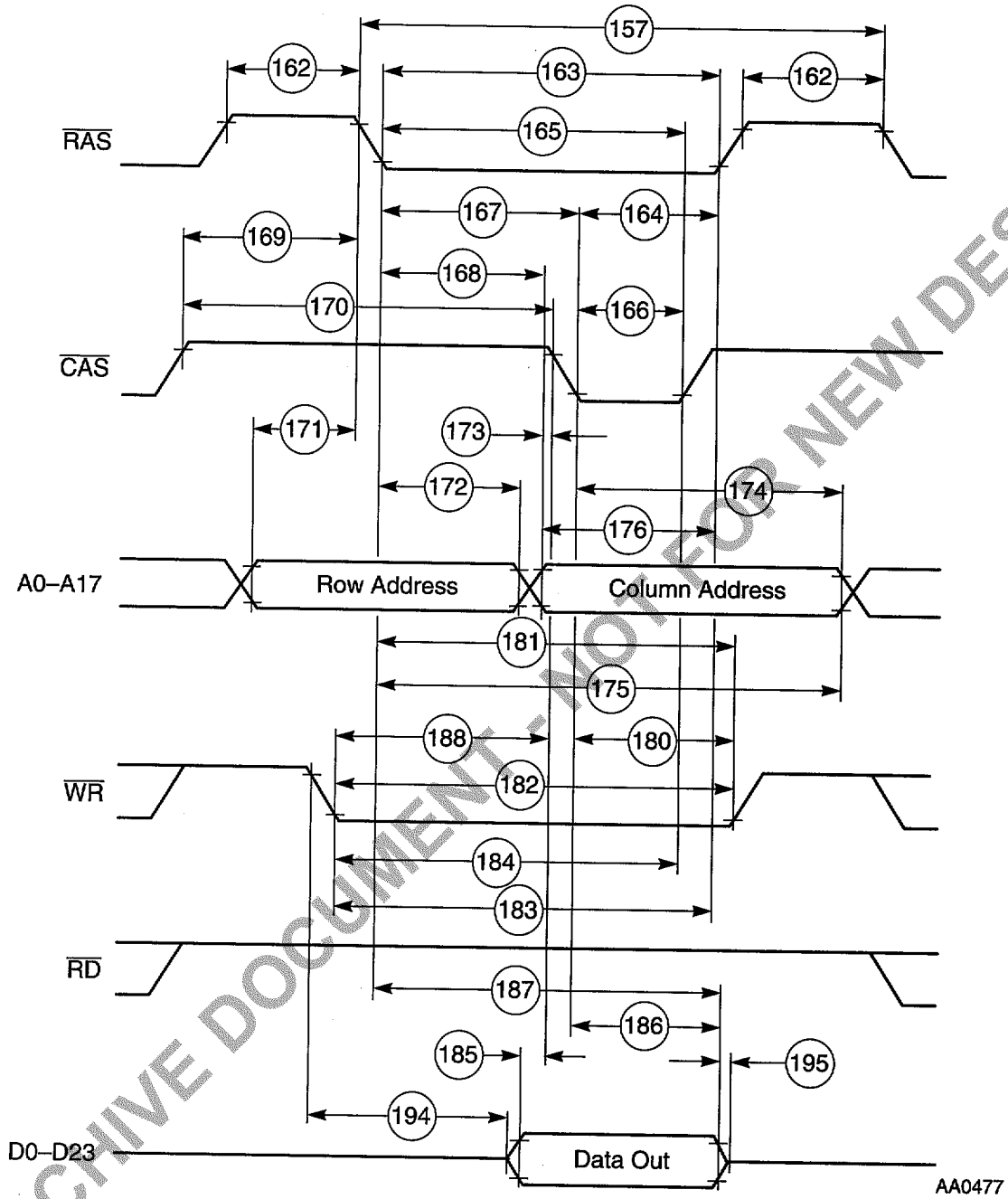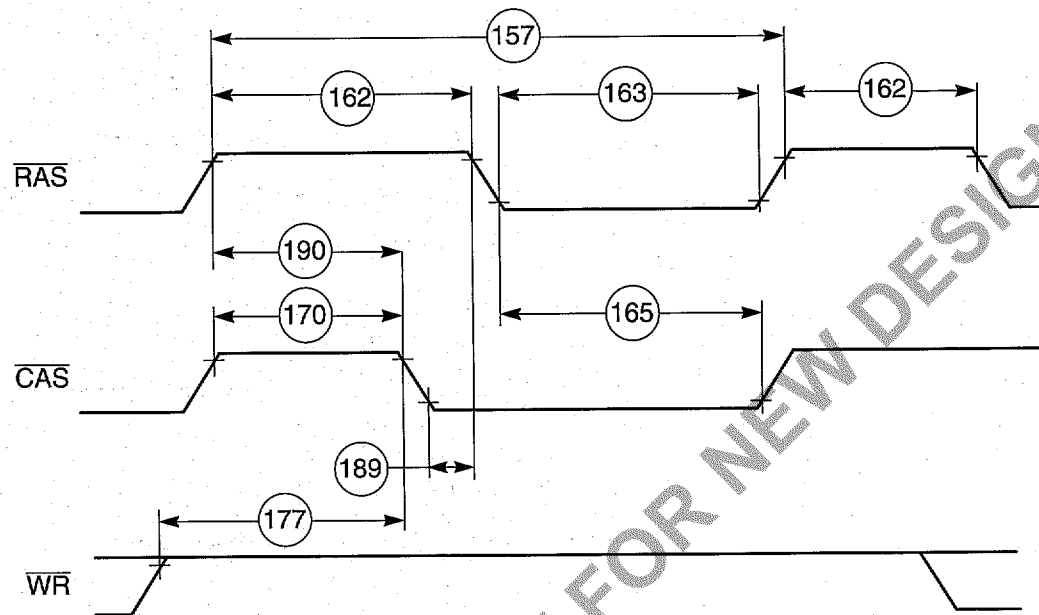
**Figure 2-20** DRAM Out-of-Page Read Access

AA0476

**Figure 2-21** DRAM Out-of-Page Write Access

**Figure 2-22** DRAM Refresh Access

**Table 2-18** External Bus Synchronous Timings (SRAM Access)[4]

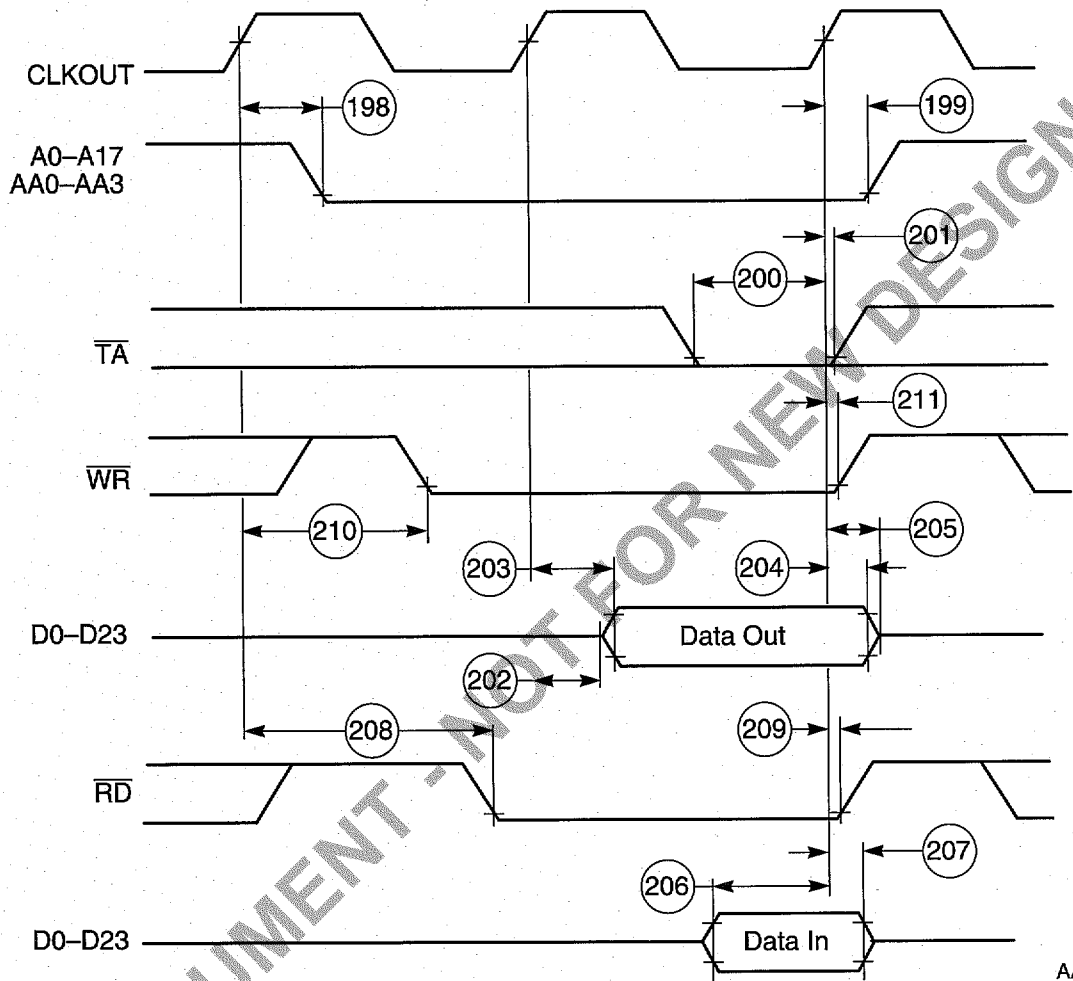| No. | Characteristics | Expression[1, 2] | 66 MHz | | 80 MHz | | Unit |
|-----|----------------|------------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 198 | CLKOUT high to address, and AA valid | **66 MHz:** $0.25 \times T_C + 5.0$ | — | 8.8 | — | — | ns |
| | | **80 MHz:** $0.25 \times T_C + 4.5$ | — | — | — | 7.6 | ns |
| 199 | CLKOUT high to address, and AA invalid | $0.25 \times T_C$ | 3.8 | — | 3.1 | — | ns |
| 200 | $\overline{\text{TA}}$ valid to CLKOUT high (setup time) | | 6.0 | — | 5.0 | — | ns |
| 201 | CLKOUT high to $\overline{\text{TA}}$ invalid (hold time) | | 0.0 | — | 0.0 | — | ns |
| 202 | CLKOUT high to data out active | $0.25 \times T_C$ | 3.8 | — | 3.1 | — | ns |
| 203 | CLKOUT high to data out valid | **66 MHz:** $0.25 \times T_C + 5.0$ | 4.8 | 8.8 | — | — | ns |
| | | **80 MHz:** $0.25 \times T_C + 4.5$ | — | — | 4.1 | 7.6 | ns |
| 204 | CLKOUT high to data out invalid | $0.25 \times T_C$ | 3.8 | — | 3.1 | — | ns |

**Preliminary Data**

**Table 2-18**  External Bus Synchronous Timings (SRAM Access)[4] (Continued)

| No. | Characteristics | Expression[1,2] | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|-----------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 205 | CLKOUT high to data out high impedance | **66 MHz:** $0.25 \times T_C + 1.0$ | — | 4.8 | — | — | ns |
| | | **80 MHz:** $0.25 \times T_C + 0.5$ | — | — | — | 3.6 | ns |
| 206 | Data in valid to CLKOUT high (setup) | | 5.0 | — | 5.0 | — | ns |
| 207 | CLKOUT high to data in invalid (hold) | | 0.0 | — | 0.0 | — | ns |
| 208 | CLKOUT high to $\overline{RD}$ assertion | **66 MHz:** $0.75 \times T_C + 5.0$ | 12.4 | 16.4 | — | — | ns |
| | | **80 MHz:** $0.75 \times T_C + 4.5$ | — | — | 10.4 | 13.9 | ns |
| 209 | CLKOUT high to $\overline{RD}$ deassertion | | 0.0 | 5.0 | 0.0 | 4.5 | ns |
| 210 | CLKOUT high to $\overline{WR}$ assertion[3] | **66 MHz:** $0.5 \times T_C + 5.3$ [WS = 1 or WS ≥ 4] | 8.9 | 12.9 | — | — | ns |
| | | **80 MHz:** $0.5 \times T_C + 4.8$ [WS = 1 or WS ≥ 4] | — | — | 7.6 | 11.1 | ns |
| | | [2 ≤ WS ≤ 3] | 1.3 | 5.3 | 1.3 | 4.8 | ns |
| 211 | CLKOUT high to $\overline{WR}$ deassertion | | 0.0 | 4.8 | 0.0 | 4.3 | ns |
| Note: | 1. WS is the number of wait states specified in the BCR. 2. The asynchronous delays specified in the expressions are valid for DSP56304. 3. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT. 4. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings. | | | | | | |

**Preliminary Data**

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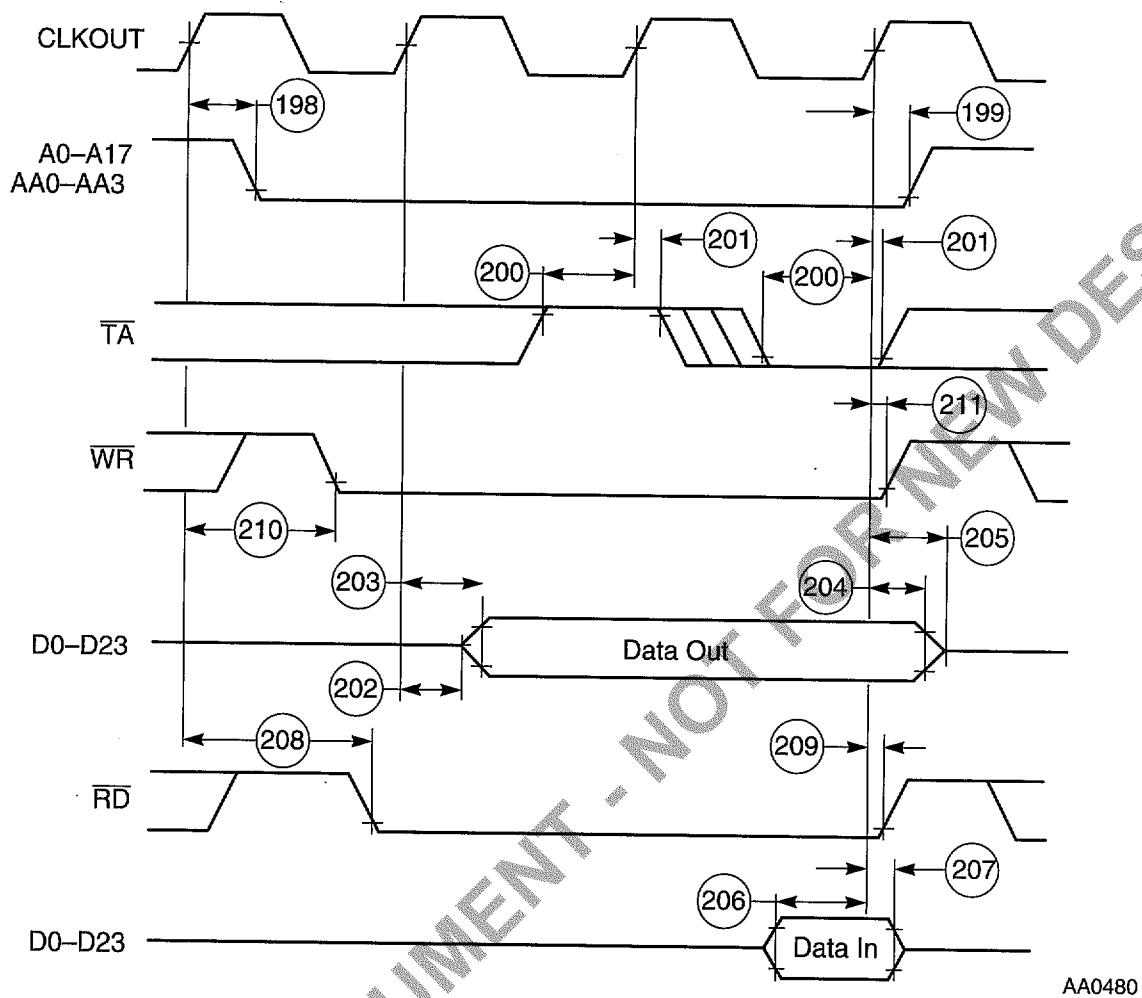**Figure 2-23** Synchronous Bus Timings SRAM 1 WS (BCR Controlled)

**Figure 2-24** Synchronous Bus Timings SRAM 2 WS ($\overline{TA}$ Controlled)

**Table 2-19**  Arbitration Bus Timings

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 212 | CLKOUT high to $\overline{BR}$ assertion/ deassertion | | 1.0 | 5.0 | 1.0 | 4.5 | ns |
| 213 | $\overline{BG}$ asserted/deasserted to CLKOUT high (setup) | | 6.0 | — | 5.0 | — | ns |
| 214 | CLKOUT high to $\overline{BG}$ deasserted/asserted (hold) | | 0.0 | — | 0.0 | — | ns |
| 215 | $\overline{BB}$ deassertion to CLKOUT high (input setup) | | 6.0 | — | 5.0 | — | ns |

**Preliminary Data**

**Table 2-19** Arbitration Bus Timings (Continued)

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|--------|--------|--------|------|
| | | | Min | Max | Min | Max | |
| 216 | CLKOUT high to $\overline{BB}$ assertion (input hold) | | 0.0 | — | 0.0 | — | ns |
| 217 | CLKOUT high to $\overline{BB}$ assertion (output) | | 1.0 | 5.0 | 1.0 | 4.5 | ns |
| 218 | CLKOUT high to $\overline{BB}$ deassertion (output) | | 1.0 | 5.0 | 1.0 | 4.5 | ns |
| 219 | $\overline{BB}$ high to $\overline{BB}$ high impedance (output) | | — | 2.7 | — | 2.2 | ns |
| 220 | CLKOUT high to address and controls active | $0.25 \times T_C$ | 3.8 | — | 3.1 | — | ns |
| 221 | CLKOUT high to address and controls high impedance | **66 MHz:** $0.25 \times T_C + 1.0$ | — | 4.8 | — | — | ns |
| | | **80 MHz:** $0.25 \times T_C + 0.5$ | — | — | — | 3.6 | ns |
| 222 | CLKOUT high to AA active | $0.25 \times T_C$ | 3.8 | — | 3.1 | — | ns |
| 223 | CLKOUT high to AA deassertion | **66 MHz:** $0.25 \times T_C + 5.0$ | 4.8 | 8.8 | — | — | ns |
| | | **80 MHz:** $0.25 \times T_C + 4.5$ | — | — | 4.1 | 7.6 | ns |
| 224 | CLKOUT high to AA high impedance | **66 MHz:** $0.75 \times T_C + 1.0$ | — | 12.4 | — | — | ns |
| | | **80 MHz:** $0.75 \times T_C + 0.5$ | — | — | — | 9.9 | ns |

Note:    The asynchronous delays specified in the expressions are valid for DSP56304.
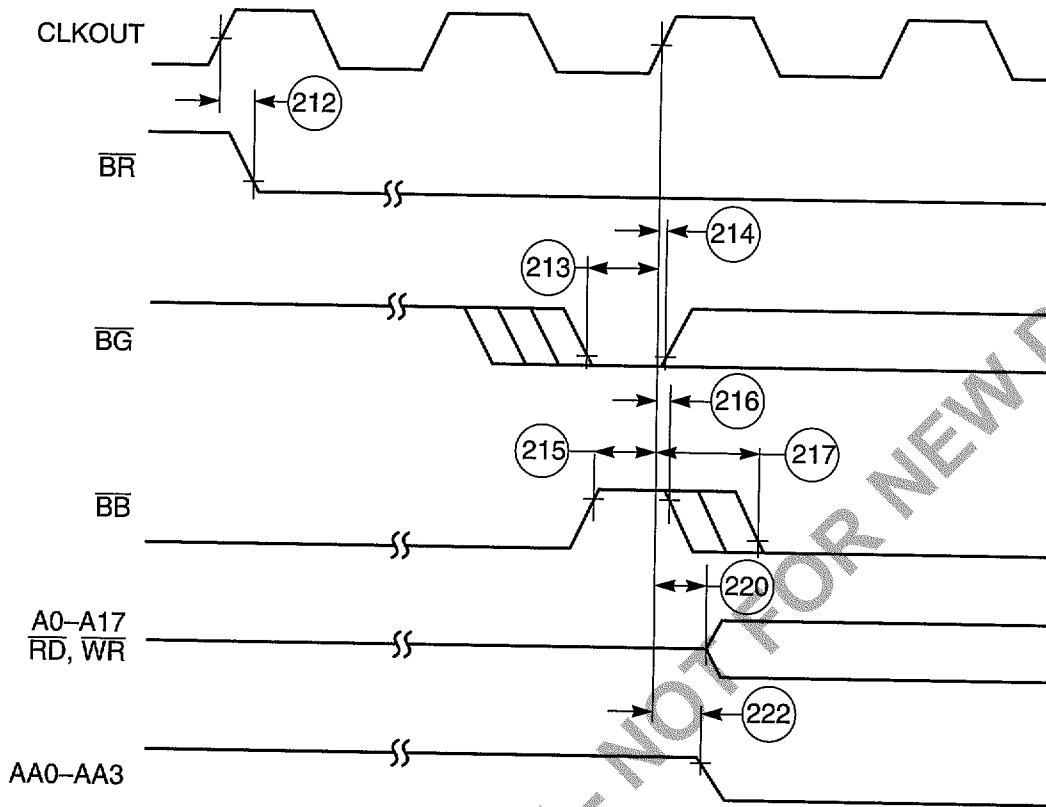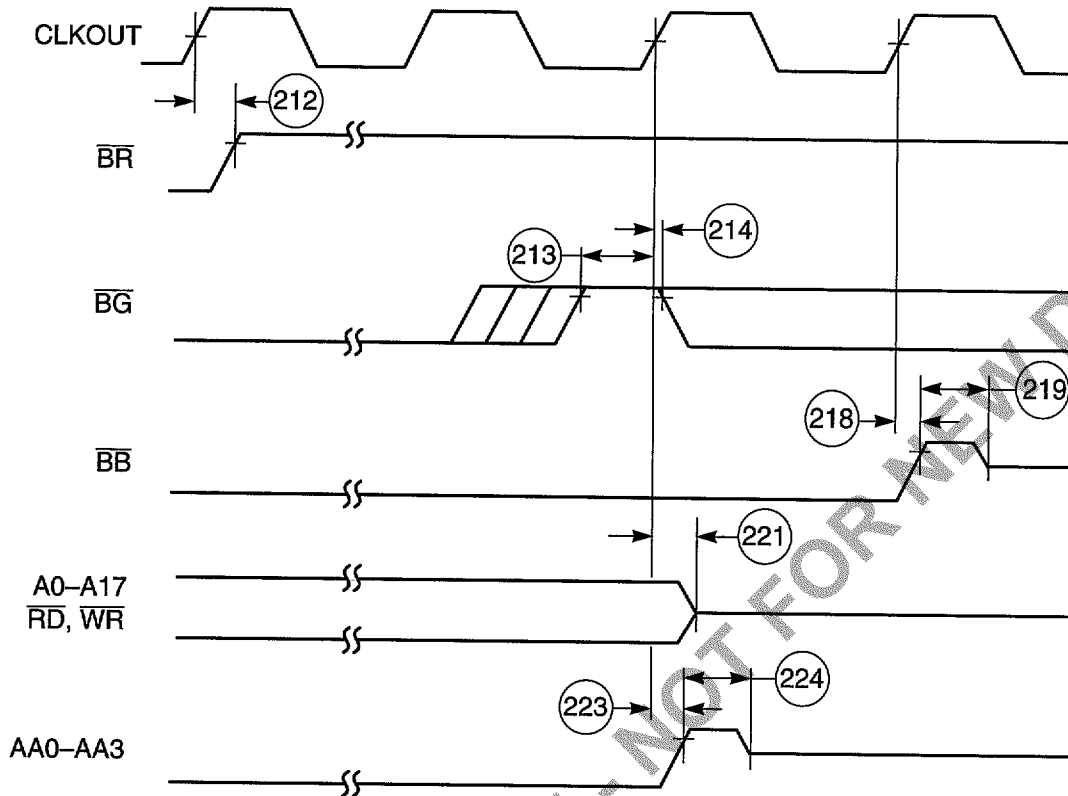
**Figure 2-25** Bus Acquisition Timings
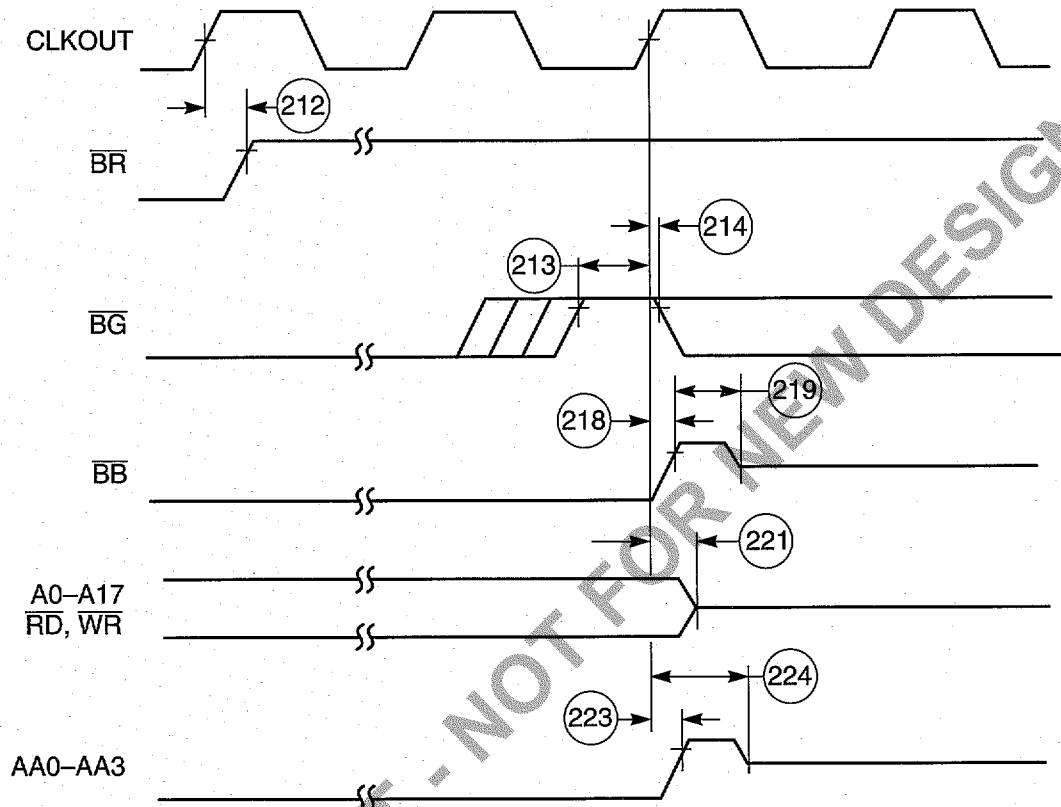
AA0482

**Figure 2-26** Bus Release Timings Case 1 (BRT Bit in OMR Cleared)

AA0483

**Figure 2-27** Bus Release Timings Case 2 (BRT Bit in OMR Set)

# HOST INTERFACE TIMING

**Table 2-20** Host Interface Timing[1, 2]

| No. | Characteristic[10] | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 300 | Access cycle time | $4 \times T_C$ | 60.6 | — | 50.0 | — | ns |
| 317 | Read data strobe assertion width[5] HACK assertion width | **66 MHz:** $T_C + 15.0$ | 30.2 | — | — | — | ns |
| | | **80 MHz:** $T_C + 12.4$ | — | — | 24.9 | — | ns |
| 318 | Read data strobe deassertion width[5] HACK deassertion width | | 15.0 | — | 12.4 | — | ns |
| 319 | Read data strobe deassertion width between two consecutive "Last Data Register" reads, or two consecutive CVR reads, or two consecutive ICR, or two consecutive ISR reads[3, 5, 8] | **66 MHz:** $2.5 \times T_C + 10.0$ | 47.9 | — | — | — | ns |
| | | **80 MHz:** $2.5 \times T_C + 8.3$ | — | — | 39.5 | — | ns |
| 320 | Write data strobe assertion width[6] | | 20.0 | — | 16.5 | — | ns |
| 321 | Write data strobe deassertion width[6] | **66 MHz:** $2.5 \times T_C + 10.0$ | 47.9 | — | — | — | ns |
| | | **80 MHz:** $2.5 \times T_C + 8.3$ | — | — | 39.5 | — | ns |
| 322 | HAS assertion width | | 15.0 | — | 12.4 | — | ns |
| 323 | HAS deassertion to data strobe assertion[4] | | 0.0 | — | 0.0 | — | ns |
| 324 | Host data input setup time before write data strobe deassertion[6] | | 15.0 | — | 12.4 | — | ns |
| 325 | Host data input hold time after write data strobe deassertion[6] | | 5.0 | — | 4.1 | — | ns |
| 326 | Read data strobe assertion to output data active from high impedance[5] HACK assertion to output data active from high impedance | | 5.0 | — | 4.1 | — | ns |
| 327 | Read data strobe assertion to output data valid[5] HACK assertion to output data valid | | — | 30.0 | — | 24.8 | ns |
| 328 | Read data strobe deassertion to output data high impedance[5] HACK deassertion to output data high impedance | | — | 15.0 | — | 12.4 | ns |

**Preliminary Data**

**Table 2-20**  Host Interface Timing[1, 2] (Continued)

| No. | Characteristic[10] | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|---------------------|------------|--------|--------|--------|--------|------|
| | | | Min | Max | Min | Max | |
| 329 | Output data hold time after read data strobe deassertion[5]<br>Output data hold time after HACK deassertion | | 5.0 | — | 4.1 | — | ns |
| 330 | HCS assertion to read data strobe deassertion[5] | **66 MHz:**<br>$T_C + 15.0$ | 30.2 | — | — | — | ns |
| | | **80 MHz:**<br>$T_C + 12.4$ | — | — | 24.9 | — | ns |
| 331 | HCS assertion to write data strobe deassertion[6] | | 15.0 | — | 12.4 | — | ns |
| 332 | HCS assertion to output data valid | | — | 25.0 | — | 20.6 | ns |
| 333 | HCS hold time after data strobe deassertion[4] | | 0.0 | — | 0.0 | — | ns |
| 334 | Address (AD7–AD0) setup time before HAS deassertion (HMUX=1) | | 7.0 | — | 5.8 | — | ns |
| 335 | Address (AD7–AD0) hold time after HAS deassertion (HMUX=1) | | 5.0 | — | 4.1 | — | ns |
| 336 | A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[4] | | 10.0 | — | 8.3 | — | ns |
| 337 | A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[4] | | 5.0 | — | 4.1 | — | ns |
| 338 | Delay from read data strobe deassertion to host request assertion for "Last Data Register" read[5, 7, 8] | **66 MHz:**<br>$2 \times T_C + 25.0$ | 55.3 | — | — | — | ns |
| | | **80 MHz:**<br>$2 \times T_C + 20.6$ | — | — | 45.6 | — | ns |
| 339 | Delay from write data strobe deassertion to host request assertion for "Last Data Register" write[6, 7, 8] | **66 MHz:**<br>$1.5 \times T_C + 25.0$ | 47.7 | — | — | — | ns |
| | | **80 MHz:**<br>$1.5 \times T_C + 20.6$ | — | — | 39.4 | — | ns |
| 340 | Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=0)[4, 7, 8] | | — | 25.0 | — | 20.6 | ns |

**Preliminary Data**

Table 2-20  Host Interface Timing[1, 2] (Continued)

| No. | Characteristic[10] | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 341 | Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=1, open drain host request)[4, 7, 8, 9] | | — | 300.0 | — | 300.0 | ns |

Note:  1.  See **Host Port Usage Considerations** on page 1-12.
2.  In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3.  This timing must be adhered to only if two consecutive reads from one of these registers are executed.
4.  The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (DS) in the Single Data Strobe mode.
5.  The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6.  The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7.  The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8.  The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Little Endian mode (HBE = 0), or RXH/TXH in the Big Endian mode (HBE = 1).
9.  In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10.  $V_{CC} = 3.3\ V \pm 0.3\ V$, $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL loads
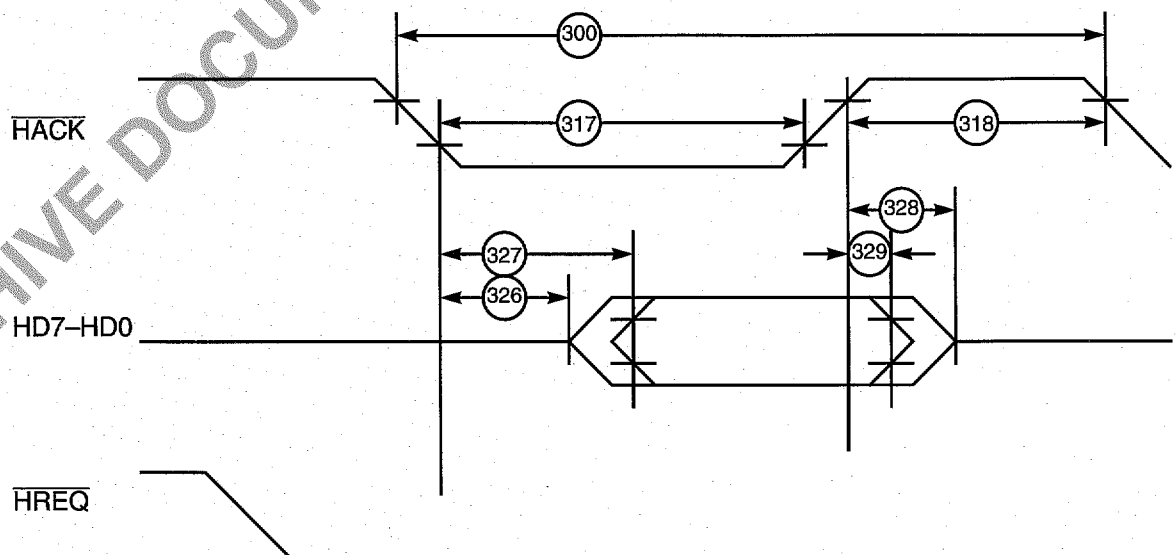


**Figure 2-28**  Host Interrupt Vector Register (IVR) Read Timing Diagram

**Preliminary Data**
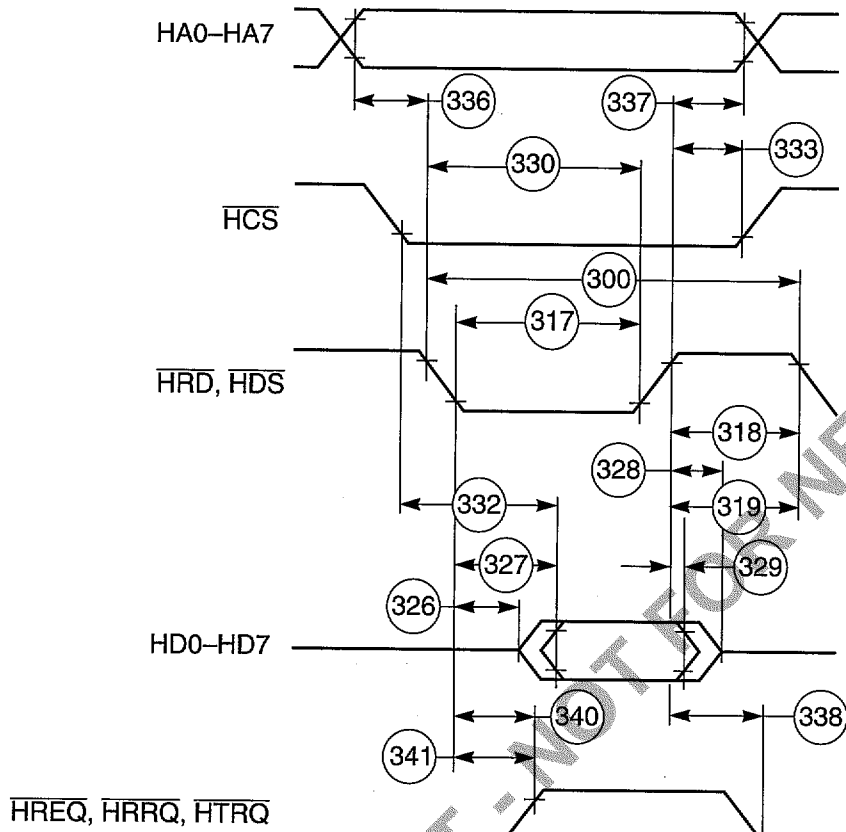
**Figure 2-29** Read Timing Diagram, Non-Multiplexed Bus
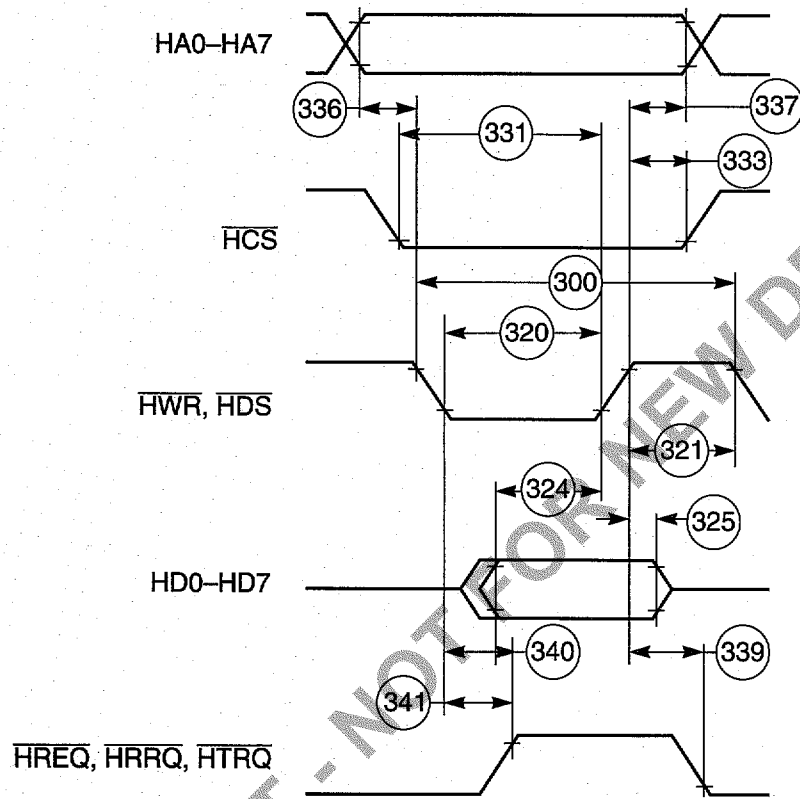
AA0485

**Figure 2-30** Write Timing Diagram, Non-Multiplexed Bus
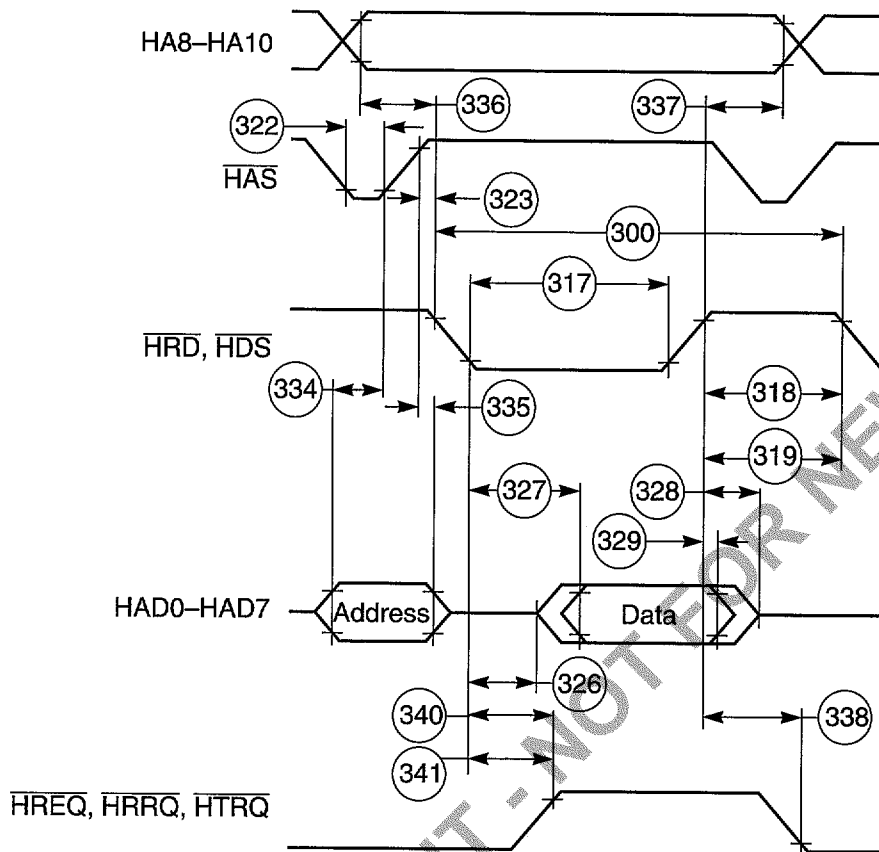
**Figure 2-31** Read Timing Diagram, Multiplexed Bus

AA0486
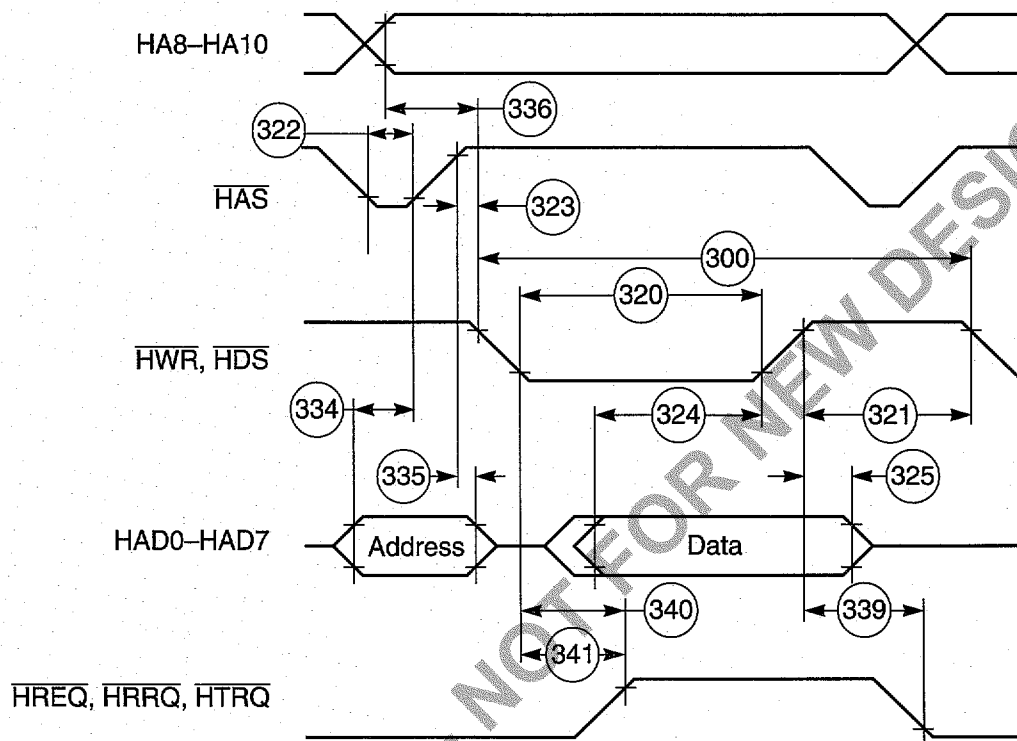
AA0487

**Figure 2-32** Write Timing Diagram, Multiplexed Bus

# SCI TIMING

Table 2-21   SCI Timing

| No. | Characteristics[1] | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|--------------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 400 | Synchronous clock cycle | $t_{SCC}$[2] | $8 \times T_C$ | 121.0 | — | 100.0 | — | ns |
| 401 | Clock low period | | $t_{SCC}/2 - 10.0$ | 50.5 | — | 40.0 | — | ns |
| 402 | Clock high period | | $t_{SCC}/2 - 10.0$ | 50.5 | — | 40.0 | — | ns |
| 403 | Output data setup to clock falling edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C - 17.0$ | 20.5 | — | 14.3 | — | ns |
| 404 | Output data hold after clock rising edge (internal clock) | | $t_{SCC}/4 - 0.5 \times T_C$ | 22.5 | — | 18.8 | — | ns |
| 405 | Input data setup time before clock rising edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C + 25.0$ | 63.0 | — | 56.3 | — | ns |
| 406 | Input data not valid before clock rising edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C - 5.5$ | — | 32.0 | — | 25.8 | ns |
| 407 | Clock falling edge to output data valid (external clock) | | | — | 32.0 | — | 32.0 | ns |
| 408 | Output data hold after clock rising edge (external clock) | | $T_C + 8.0$ | 23.0 | — | 20.5 | — | ns |
| 409 | Input data setup time before clock rising edge (external clock) | | | 0.0 | — | 0.0 | — | ns |
| 410 | Input data hold time after clock rising edge (external clock) | | | 9.0 | — | 9.0 | — | ns |
| 411 | Asynchronous clock cycle | $t_{ACC}$[3] | $64 \times T_C$ | 969.7 | — | 800.0 | — | ns |
| 412 | Clock low period | | $t_{ACC}/2 - 10.0$ | 474.8 | — | 390.0 | — | ns |

**Preliminary Data**

Table 2-21 SCI Timing (Continued)

| No. | Characteristics[1] | Symbol | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-------------------|--------|------------|--------|-----|--------|-----|------|
| | | | | Min | Max | Min | Max | |
| 413 | Clock high period | | $t_{ACC}/2 - 10.0$ | 474.8 | — | 390.0 | — | ns |
| 414 | Output data setup to clock rising edge (internal clock) | | $t_{ACC}/2 - 30.0$ | 458.8 | — | 370.0 | — | ns |
| 415 | Output data hold after clock rising edge (internal clock) | | $t_{ACC}/2 - 30.0$ | 458.8 | — | 370.0 | — | ns |

Note: 1. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads
2. $t_{SCC}$ = synchronous clock cycle time (For internal clock, $t_{SCC}$ is determined by the SCI clock control register and $T_C$.)
3. $t_{ACC}$ = asynchronous clock cycle time; value given for 1X clock mode (For internal clock, $t_{ACC}$ is determined by the SCI clock control register and $T_C$.)
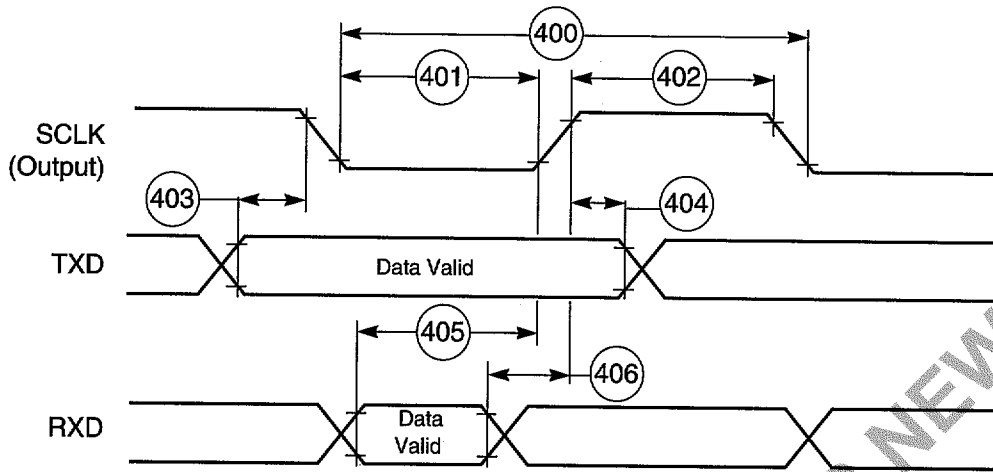
a) Internal Clock
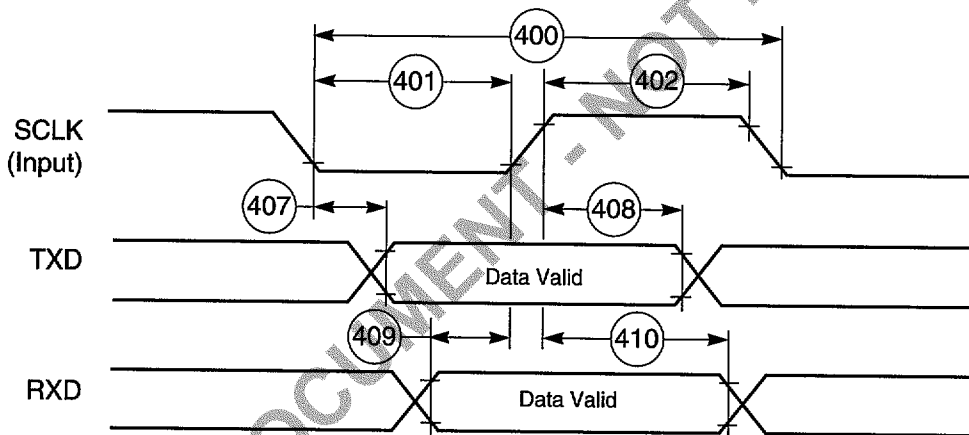


b) External Clock

AA0488

**Figure 2-33** SCI Synchronous Mode Timing



AA0489

**Figure 2-34** SCI Asynchronous Mode Timing

**Preliminary Data**

# ESSI0/ESSI1 TIMING

Table 2-22  ESSI Timings

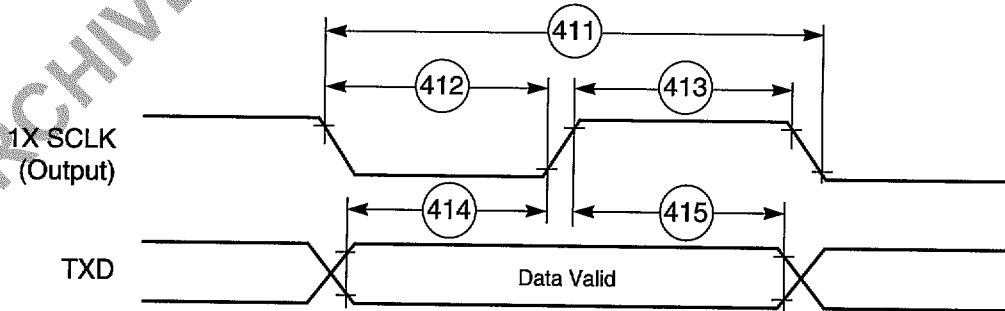| No. | Characteristics[4, 6, 7] | Symbol | Expression | 66 MHz | | 80 MHz | | Cond-ition[5] | Unit |
|-----|------------------------|--------|------------|--------|-----|--------|-----|---------|------|
| | | | | Min | Max | Min | Max | | |
| 430 | Clock cycle[1] | $t_{SSICC}$ | $4 \times T_C$ | 60.6 | — | 50.0 | — | i ck | ns |
| | | | $3 \times T_C$ | 45.5 | — | 37.5 | — | x ck | |
| 431 | Clock high period | | | | | | | | ns |
| | • For internal clock | | $2 \times T_C - 10.0$ | 20.3 | — | 15.0 | — | | |
| | • For external clock | | $1.5 \times T_C$ | 22.7 | — | 18.8 | — | | ns |
| 432 | Clock low period | | | | | | | | |
| | • For internal clock | | $2 \times T_C - 10.0$ | 20.3 | — | 15.0 | — | | ns |
| | • For external clock | | $1.5 \times T_C$ | 22.7 | — | 18.8 | — | | ns |
| 433 | RXC rising edge to FSR out (bl) high | | | — | 37.0 | — | 37.0 | x ck | ns |
| | | | | — | 22.0 | — | 22.0 | i ck a | |
| 434 | RXC rising edge to FSR out (bl) low | | | — | 37.0 | — | 37.0 | x ck | ns |
| | | | | — | 22.0 | — | 22.0 | i ck a | |
| 435 | RXC rising edge to FSR out (wr) high[2] | | | — | 39.0 | — | 39.0 | x ck | ns |
| | | | | — | 24.0 | — | 24.0 | i ck a | |
| 436 | RXC rising edge to FSR out (wr) low[2] | | | — | 39.0 | — | 39.0 | x ck | ns |
| | | | | — | 24.0 | — | 24.0 | i ck a | |
| 437 | RXC rising edge to FSR out (wl) high | | | — | 36.0 | — | 36.0 | x ck | ns |
| | | | | — | 21.0 | — | 21.0 | i ck a | |
| 438 | RXC rising edge to FSR out (wl) low | | | — | 37.0 | — | 37.0 | x ck | ns |
| | | | | — | 22.0 | — | 22.0 | i ck a | |
| 439 | Data in setup time before RXC (SCK in synchronous mode) falling edge | | | 0.0 | — | 0.0 | — | x ck | ns |
| | | | | 19.0 | — | 19.0 | — | i ck | |
| 440 | Data in hold time after RXC falling edge | | | 5.0 | — | 5.0 | — | x ck | ns |
| | | | | 3.0 | — | 3.0 | — | i ck | |
| 441 | FSR input (bl, wr) high before RXC falling edge [2] | | | 23.0 | — | 23.0 | — | x ck | ns |
| | | | | 1.0 | — | 1.0 | — | i ck a | |

**Preliminary Data**

**Table 2-22** ESSI Timings (Continued)

| No. | Characteristics[4,6,7] | Symbol | Expression | 66 MHz | | 80 MHz | | Cond-ition[5] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | | |
| 442 | FSR input (wl) high before RXC falling edge | | | 23.0 1.0 | — — | 23.0 1.0 | — — | x ck i ck a | ns |
| 443 | FSR input hold time after RXC falling edge | | | 3.0 0.0 | — — | 3.0 0.0 | — — | x ck i ck a | ns |
| 444 | Flags input setup before RXC falling edge | | | 0.0 19.0 | — — | 0.0 19.0 | — — | x ck i ck s | ns |
| 445 | Flags input hold time after RXC falling edge | | | 6.0 0.0 | — — | 6.0 0.0 | — — | x ck i ck s | ns |
| 446 | TXC rising edge to FST out (bl) high | | | — — | 29.0 15.0 | — — | 29.0 15.0 | x ck i ck | ns |
| 447 | TXC rising edge to FST out (bl) low | | | — — | 31.0 17.0 | — — | 31.0 17.0 | x ck i ck | ns |
| 448 | TXC rising edge to FST out (wr) high[2] | | | — — | 31.0 17.0 | — — | 31.0 17.0 | x ck i ck | ns |
| 449 | TXC rising edge to FST out (wr) low[2] | | | — — | 33.0 19.0 | — — | 33.0 19.0 | x ck i ck | ns |
| 450 | TXC rising edge to FST out (wl) high | | | — — | 30.0 16.0 | — — | 30.0 16.0 | x ck i ck | ns |
| 451 | TXC rising edge to FST out (wl) low | | | — — | 31.0 17.0 | — — | 31.0 17.0 | x ck i ck | ns |
| 452 | TXC rising edge to data out enable from high impedance | | | — — | 31.0 17.0 | — — | 31.0 17.0 | x ck i ck | ns |
| 453 | TXC rising edge to Transmitter #0 drive enable assertion | | | — — | 34.0 20.0 | — — | 34.0 20.0 | x ck i ck | ns |
| 454 | TXC rising edge to data out valid | | $35 + 0.5 \times T_C$ 21.0 | — — | 42.6 21.0 | — — | 41.3 21.0 | x ck i ck | ns |
| 455 | TXC rising edge to data out high impedance[3] | | | — — | 31.0 16.0 | — — | 31.0 16.0 | x ck i ck | ns |
| 456 | TXC rising edge to Transmitter #0 drive enable deassertion[3] | | | — — | 34.0 20.0 | — — | 34.0 20.0 | x ck i ck | ns |

**Preliminary Data**

**Table 2-22** ESSI Timings (Continued)

| No. | Characteristics[4, 6, 7] | Symbol | Expression | 66 MHz | | 80 MHz | | Cond-ition[5] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | | |
| 457 | FST input (bl, wr) setup time before TXC falling edge[2] | | | 2.0 21.0 | — — | 2.0 21.0 | — — | x ck i ck | ns |
| 458 | FST input (wl) to data out enable from high impedance | | | — | 27.0 | — | 27.0 | — | ns |
| 459 | FST input (wl) to Transmitter #0 drive enable assertion | | | — | 31.0 | — | 31.0 | — | ns |
| 460 | FST input (wl) setup time before TXC falling edge | | | 2.0 21.0 | — — | 2.0 21.0 | — — | x ck i ck | ns |
| 461 | FST input hold time after TXC falling edge | | | 4.0 0.0 | — — | 4.0 0.0 | — — | x ck i ck | ns |
| 462 | Flag output valid after TXC rising edge | | | — — | 32.0 18.0 | — — | 32.0 18.0 | x ck i ck | ns |

Note:
1. For the internal clock, the external clock cycle is defined by Icyc and the ESSI control register.
2. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as Bit Length Frame Sync signal), until the one before last bit clock of the first word in frame.
3. Periodically sampled and not 100% tested
4. $V_{CC} = 3.3$ V $\pm 0.3$ V; $T_J = -40°C$ to $+100$ °C, $C_L = 50$ pF + 2 TTL Loads
5. TXC (SCK Pin) = Transmit Clock
   RXC (SC0 or SCK Pin) = Receive Clock
   FST (SC2 Pin) = Transmit Frame Sync
   FSR (SC1 or SC2 Pin) Receive Frame Sync
6. i ck = Internal Clock
   x ck = External Clock
   i ck a = Internal Clock, Asynchronous mode
        (Asynchronous implies that TXC and RXC are two different clocks)
   i ck s = Internal Clock, Synchronous mode
        (Synchronous implies that TXC and RXC are the same clock)
7. bl = bit length
   wl = word length
   wr = word length relative

**Preliminary Data**
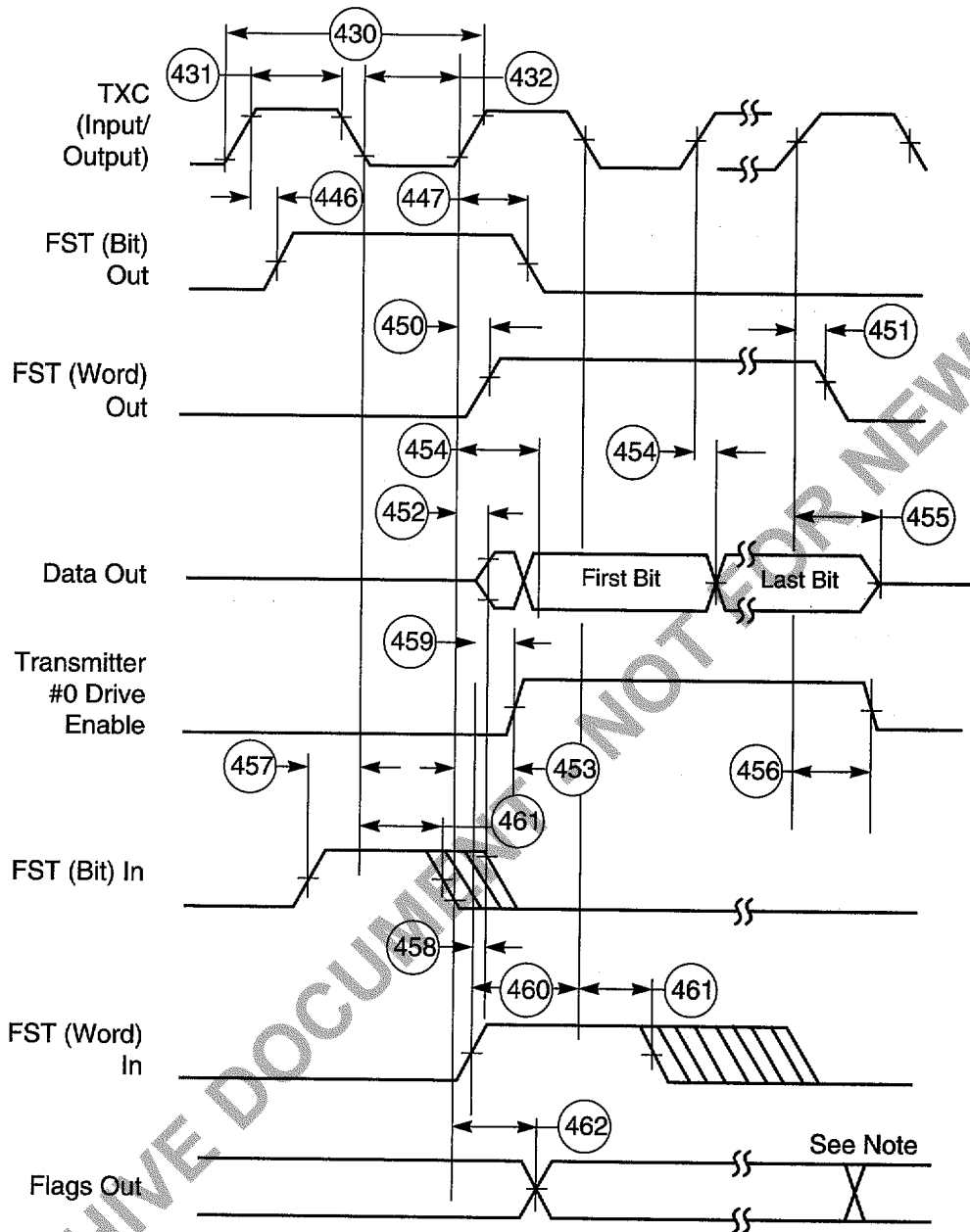
Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

AA0490

**Figure 2-35** ESSI Transmitter Timing
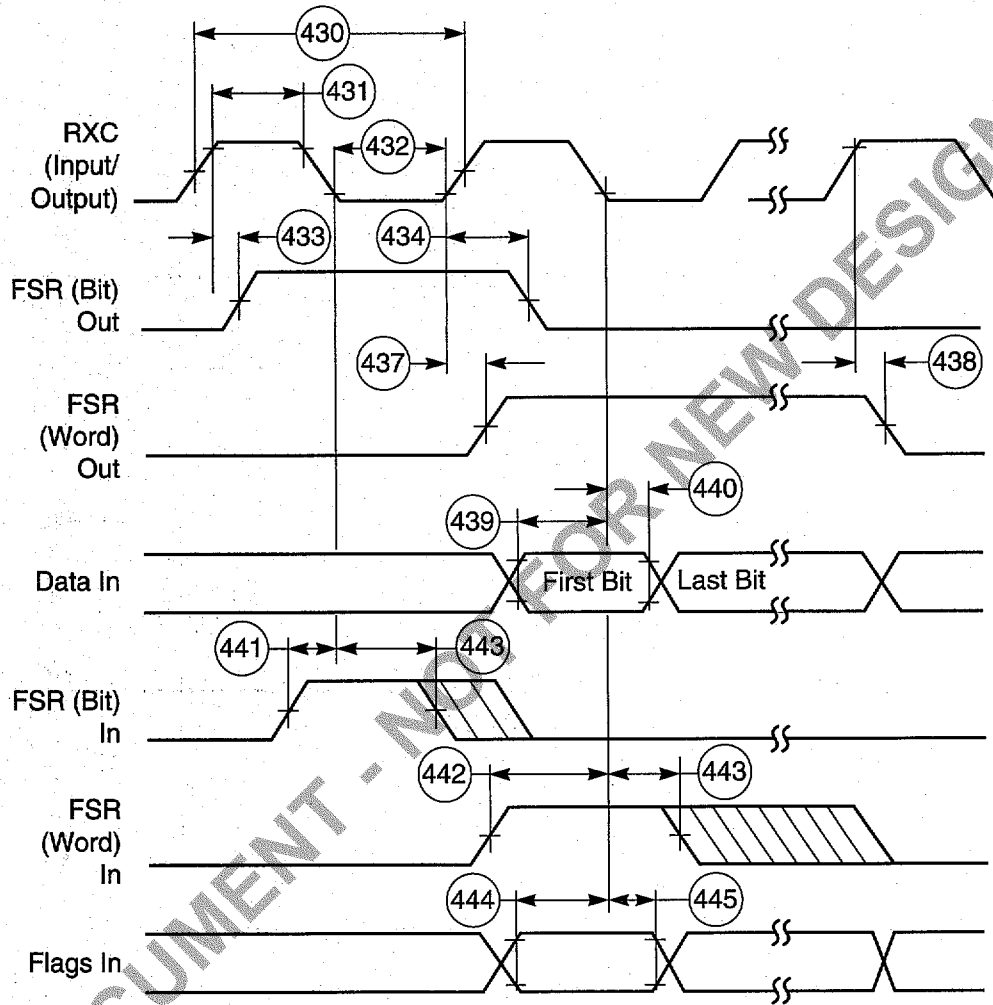
**Figure 2-36** ESSI Receiver Timing

AA0491

# TIMER TIMING

Table 2-23  Timer Timing

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 480 | TIO Low | $2 \times T_C + 2.0$ | 32.5 | — | 27.0 | — | ns |
| 481 | TIO High | $2 \times T_C + 2.0$ | 32.5 | — | 27.0 | — | ns |
| 482 | Timer setup time from TIO (Input) assertion to CLKOUT rising edge | | 9.0 | $T_C$ | 9.0 | $T_C$ | ns |
| 483 | Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution | $10.25 \times T_C + 1.0$ | 156.0 | — | 129.1 | — | ns |
| 484 | CLKOUT rising edge to TIO (Output) assertion<br>• Minimum | **66 MHz:**<br>$0.5 \times T_C + 3.4$ | 11.0 | — | — | — | ns |
| | | **80 MHz:**<br>$0.5 \times T_C + 3.5$ | — | — | 9.8 | — | ns |
| | • Maximum | **66 MHz:**<br>$0.5 \times T_C + 20.5$ | — | 28.1 | — | — | ns |
| | | **80 MHz:**<br>$0.5 \times T_C + 19.8$ | — | — | — | 26.1 | ns |
| 485 | CLKOUT rising edge to TIO (Output) deassertion<br>• Minimum | **66 MHz:**<br>$0.5 \times T_C + 3.4$ | 11.0 | 28.1 | — | — | ns |
| | | **80 MHz:**<br>$0.5 \times T_C + 3.5$ | — | — | 9.8 | 26.1 | ns |
| | • Maximum | **66 MHz:**<br>$0.5 \times T_C + 20.5$ | 11.0 | 28.1 | — | — | ns |
| | | **80 MHz:**<br>$0.5 \times T_C + 19.8$ | — | — | 9.8 | 26.1 | ns |

Note:    $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40°C$ to $+100 °C$, $C_L = 50 \text{ pF} + 2 \text{ TTL Loads}$

**Preliminary Data**

**Figure 2-37** TIO Timer Event Input Restrictions
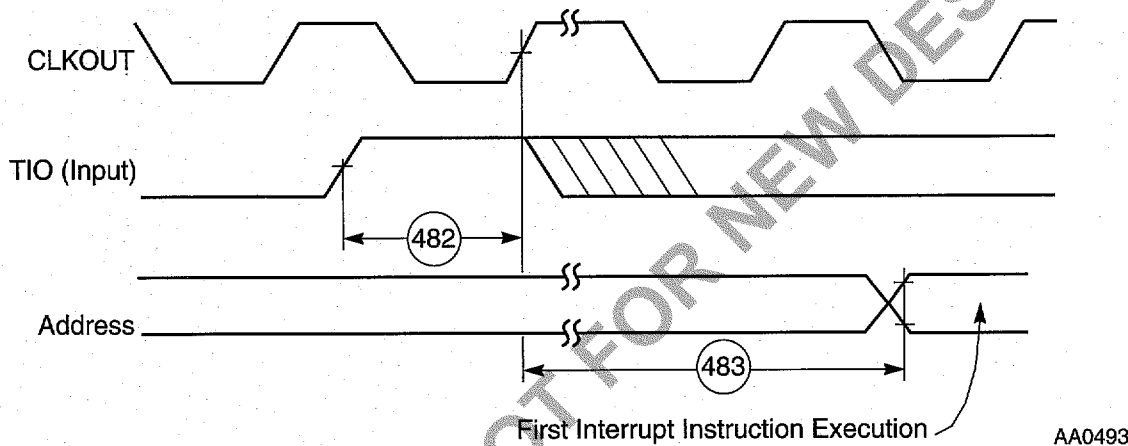


**Figure 2-38** Timer Interrupt Generation
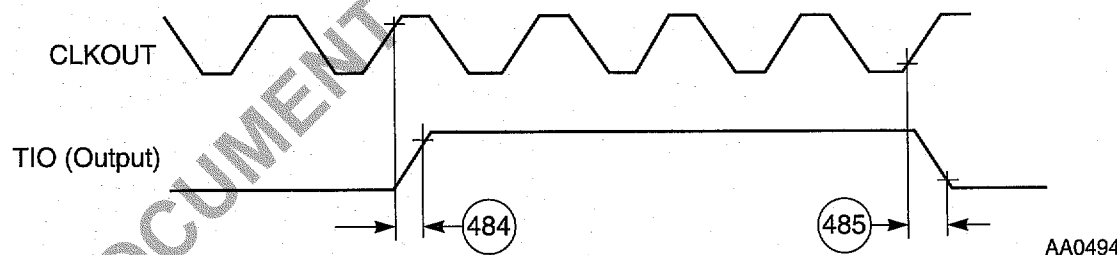


**Figure 2-39** External Pulse Generation

# GPIO TIMING

**Table 2-24** GPIO Timing

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|-----------------|------------|--------|-----|--------|-----|------|
| | | | Min | Max | Min | Max | |
| 490 | CLKOUT edge to GPIO out valid (GPIO out delay time) | | — | 31.0 | — | 31.0 | ns |
| 491 | CLKOUT edge to GPIO out not valid (GPIO out hold time) | | 3.0 | — | 3.0 | — | ns |
| 492 | GPIO In valid to CLKOUT edge (GPIO in set-up time) | | 12.0 | — | 12.0 | — | ns |
| 493 | CLKOUT edge to GPIO in not valid (GPIO in hold time) | | 0.0 | — | 0.0 | — | ns |
| 494 | Fetch to CLKOUT edge before GPIO change | $6.75 \times T_C$ | 102.3 | — | 84.4 | — | ns |

Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2\ TTL\ Loads$
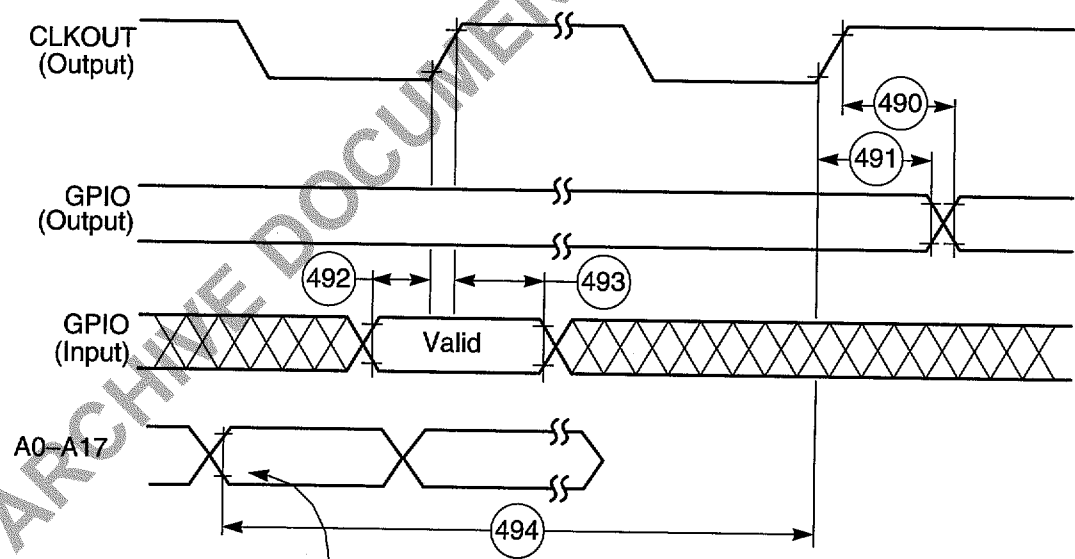


Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

AA0495

**Figure 2-40** GPIO Timing

**Preliminary Data**

## JTAG TIMING

Table 2-25  JTAG Timing

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 500 | TCK frequency of operation | | 0.0 | 22.0 | 0.0 | 22.0 | MHz |
| 501 | TCK cycle time in crystal mode | | 45.0 | — | 45.0 | — | ns |
| 502 | TCK clock pulse width measured at 1.5 V | | 20.0 | — | 20.0 | — | ns |
| 503 | TCK rise and fall times | | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| 504 | Boundary scan input data setup time | | 5.0 | — | 5.0 | — | ns |
| 505 | Boundary scan input data hold time | | 24.0 | — | 24.0 | — | ns |
| 506 | TCK low to output data valid | | 0.0 | 40.0 | 0.0 | 40.0 | ns |
| 507 | TCK low to output high impedance | | 0.0 | 40.0 | 0.0 | 40.0 | ns |
| 508 | TMS, TDI data setup time | | 5.0 | — | 5.0 | — | ns |
| 509 | TMS, TDI data hold time | | 25.0 | — | 25.0 | — | ns |
| 510 | TCK low to TDO data valid | | 0.0 | 44.0 | 0.0 | 44.0 | ns |
| 511 | TCK low to TDO high impedance | | 0.0 | 44.0 | 0.0 | 44.0 | ns |
| 512 | $\overline{TRST}$ assert time | | 100.0 | — | 100.0 | — | ns |
| 513 | $\overline{TRST}$ setup time to TCK low | | 40.0 | — | 40.0 | — | ns |

Note:  1.  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40°C$ to $+100 °C$, $C_L = 50 \text{ pF} + 2$ TTL Loads
2.  All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.
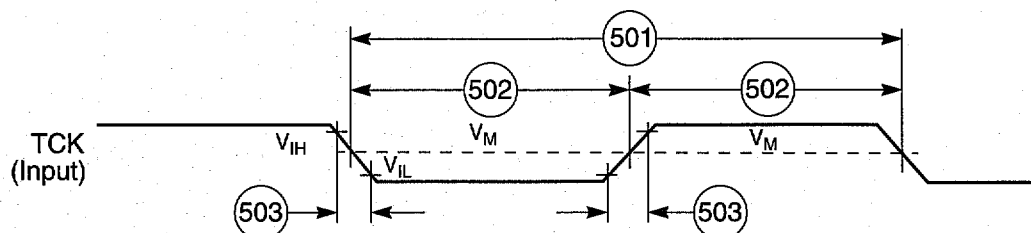


Figure 2-41 Test Clock Input Timing Diagram

**Preliminary Data**
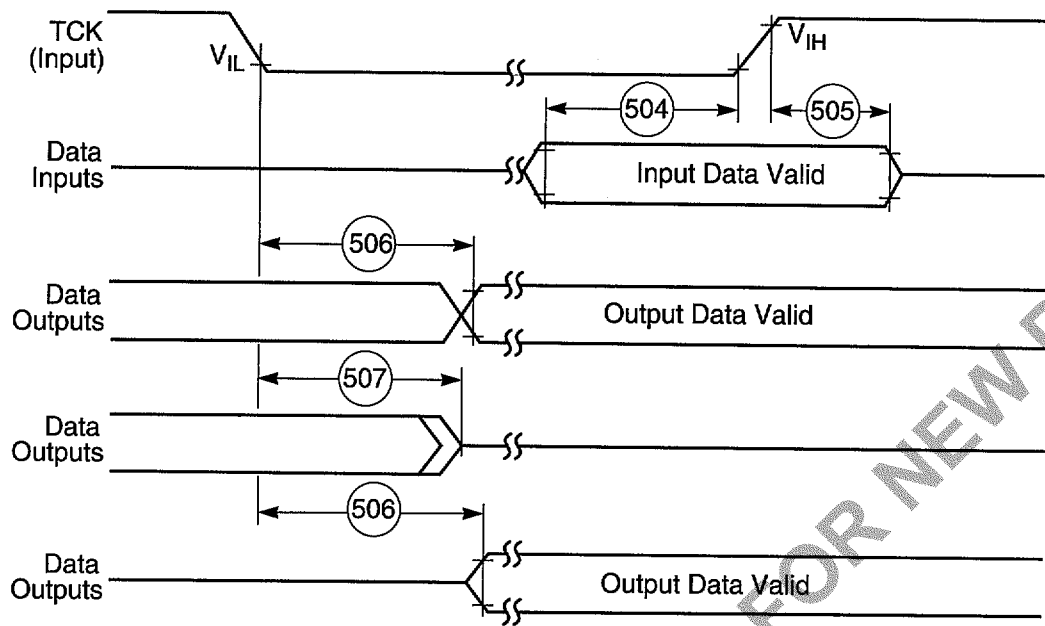
**Figure 2-42** Boundary Scan (JTAG) Timing Diagram
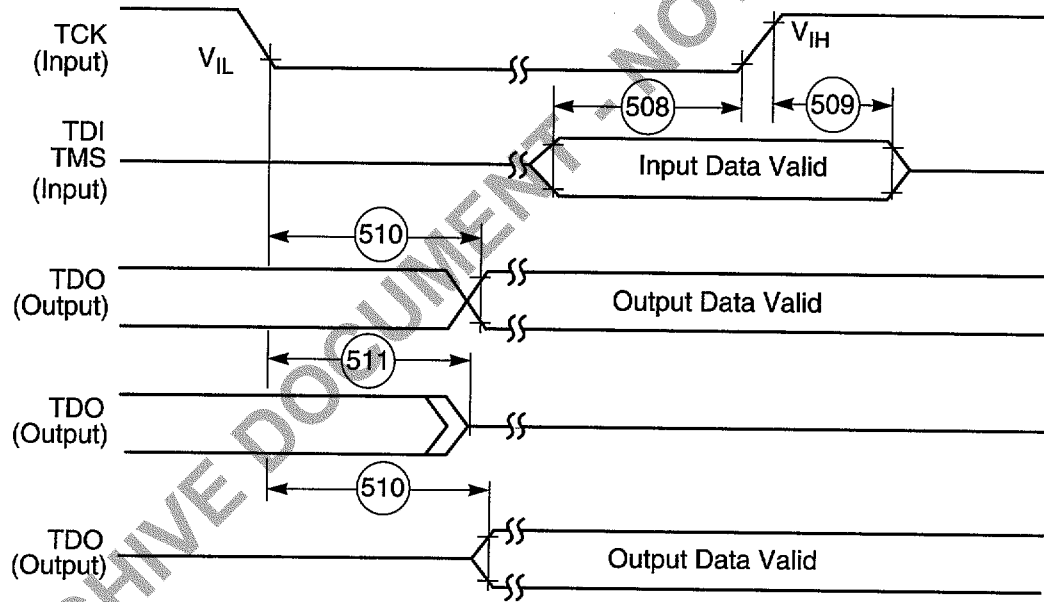


**Figure 2-43** Test Access Port Timing Diagram

**Preliminary Data**
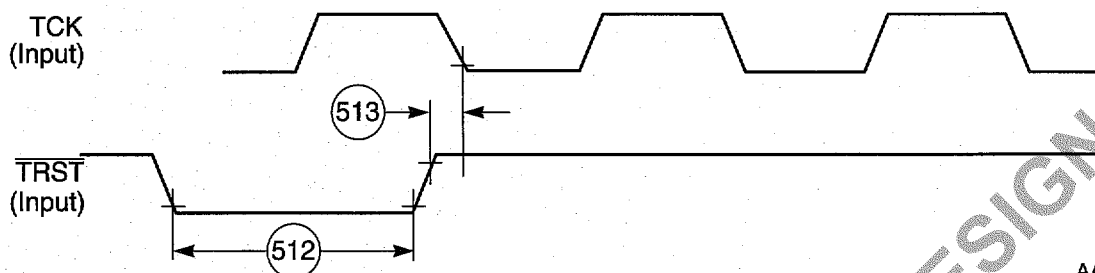
**Figure 2-44** $\overline{\text{TRST}}$ Timing Diagram

## OnCE MODULE TIMING

**Table 2-26** OnCE Module Timing

| No. | Characteristics | Expression | 66 MHz | | 80 MHz | | Unit |
|-----|----------------|------------|--------|--------|--------|--------|------|
| | | | Min | Max | Min | Max | |
| 500 | TCK frequency of operation | $1/(3 \times T_C)$, max 22.0 MHz | 0.0 | 22.0 | 0.0 | 22.0 | MHz |
| 514 | $\overline{\text{DE}}$ assertion time in order to enter debug mode | $1.5 \times T_C + 10.0$ | 32.0 | — | 28.8 | — | ns |
| 515 | Response time when DSP56304 is executing NOP instructions from internal memory | $5.5 \times T_C + 30.0$ | — | 114.0 | — | 98.8 | ns |
| 516 | Debug acknowledge assertion time | $3 \times T_C + 10.0$ | 55.5 | — | 47.5 | — | ns |

Note: $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40°C$ to $+100 °C$, $C_L = 50 \text{ pF} + 2$ TTL Loads
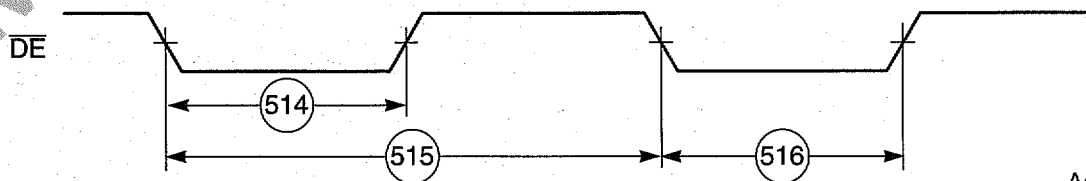


**Figure 2-45** OnCE—Debug Request

**Preliminary Data**

# SECTION 3

# PACKAGING

## PIN-OUT AND PACKAGE INFORMATION

This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for each package.

The DSP56304 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Plastic Ball Grid Array (PBGA)

## TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.
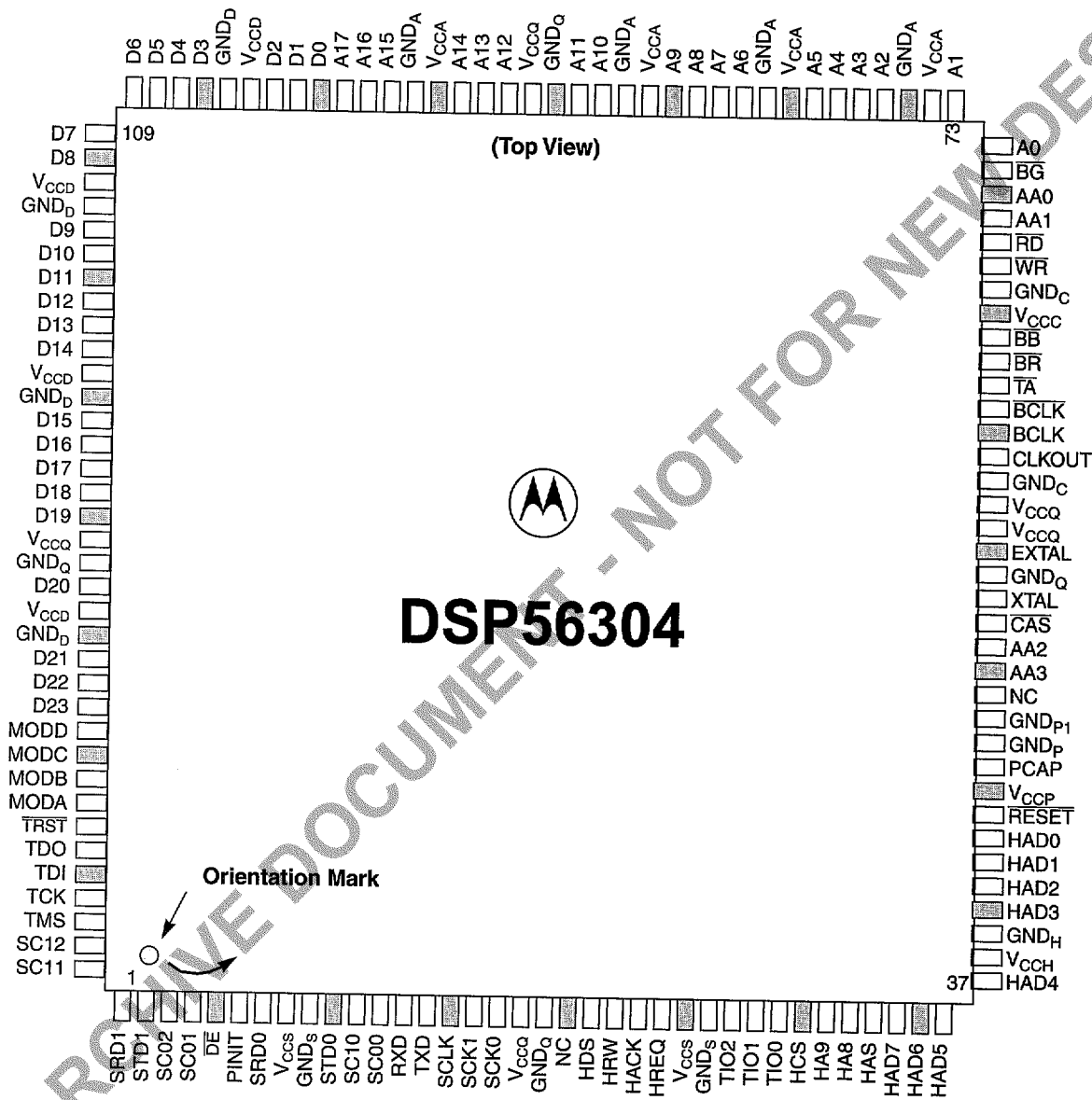


Note: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

AA0301

**Figure 3-1** DSP56304 Thin Quad Flat Pack (TQFP), Top View

**Preliminary Data**

Left side pins (top to bottom): A0, BG, AA0, AA1, RD, WR, GND_C, V_CCC, BB, BR, TA, BCLK, BCLK, CLKOUT, GND_C, V_CCC, V_CCQ, EXTAL, GND_Q, XTAL, CAS, AA2, AA3, NC, GND_P1, GND_P, PCAP, V_CCP, RESET, HAD0, HAD1, HAD2, HAD3, GND_H, V_CCH, HAD4

Top side pins (left to right): A1, V_CCA, GND_A, A2, A3, A4, A5, V_CCA, GND_A, A6, A7, A8, A9, V_CCA, GND_A, A10, A11, GND_Q, V_CCQ, A12, A13, A14, V_CCA, GND_A, A15, A16, A17, D0, D1, D2, V_CCD, GND_D, D3, D4, D5, D6

Right side pins (top to bottom): D7, D8, V_CCD, GND_D, D9, D10, D11, D12, D13, D14, V_CCD, GND_D, D15, D16, D17, D18, D19, V_CCQ, GND_Q, D20, V_CCD, GND_D, D21, D22, D23, MODD, MODC, MODB, MODA, TRST, TDO, TDI, TCK, TMS, SC12, SC11

Bottom side pins (left to right): HAD5, HAD6, HAD7, HAS, HA8, HA9, HCS, TIO0, TIO1, TIO2, GND_S, V_CCQ, HREQ, HACK, HRW, HDS, NC, GND_Q, V_CCQ, SCK0, SCK1, SCLK, TXD, RXD, SC00, SC10, STD0, GND_S, V_CCS, SRD0, PINIT, DE, SC01, SC02, STD1, SRD1

(Bottom View)

DSP56304

73    109

37    1

Orientation Mark (on top side)

Note: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

AA0302

**Figure 3-2** DSP56304 Thin Quad Flat Pack (TQFP), Bottom View

**Preliminary Data**

Table 3-1   DSP56304 TQFP Signal Identification by Pin Number

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|---|---|
| 1 | SRD1 or PD4 | 26 | $GND_S$ | 51 | AA2/$\overline{RAS2}$ |
| 2 | STD1 or PD5 | 27 | TIO2 | 52 | $\overline{CAS}$ |
| 3 | SC02 or PC2 | 28 | TIO1 | 53 | XTAL |
| 4 | SC01 or PC1 | 29 | TIO0 | 54 | $GND_Q$ |
| 5 | $\overline{DE}$ | 30 | $\overline{HCS}$/HCS, HA10, or PB13 | 55 | EXTAL |
| 6 | PINIT/$\overline{NMI}$ | 31 | HA2, HA9, or PB10 | 56 | $V_{CCQ}$ |
| 7 | SRD0 or PC4 | 32 | HA1, HA8, or PB9 | 57 | $V_{CCC}$ |
| 8 | $V_{CCS}$ | 33 | HA0, $\overline{HAS}$/HAS, or PB8 | 58 | $GND_C$ |
| 9 | $GND_S$ | 34 | H7, HAD7, or PB7 | 59 | CLKOUT |
| 10 | STD0 or PC5 | 35 | H6, HAD6, or PB6 | 60 | BCLK |
| 11 | SC10 or PD0 | 36 | H5, HAD5, or PB5 | 61 | $\overline{BCLK}$ |
| 12 | SC00 or PC0 | 37 | H4, HAD4, or PB4 | 62 | $\overline{TA}$ |
| 13 | RXD or PE0 | 38 | $V_{CCH}$ | 63 | $\overline{BR}$ |
| 14 | TXD or PE1 | 39 | $GND_H$ | 64 | $\overline{BB}$ |
| 15 | SCLK or PE2 | 40 | H3, HAD3, or PB3 | 65 | $V_{CCC}$ |
| 16 | SCK1 or PD3 | 41 | H2, HAD2, or PB2 | 66 | $GND_C$ |
| 17 | SCK0 or PC3 | 42 | H1, HAD1, or PB1 | 67 | $\overline{WR}$ |
| 18 | $V_{CCQ}$ | 43 | H0, HAD0, or PB0 | 68 | $\overline{RD}$ |
| 19 | $GND_Q$ | 44 | $\overline{RESET}$ | 69 | AA1/$\overline{RAS1}$ |
| 20 | Not Connected (NC), reserved | 45 | $V_{CCP}$ | 70 | AA0/$\overline{RAS0}$ |
| 21 | $\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12 | 46 | PCAP | 71 | $\overline{BG}$ |
| 22 | HRW, $\overline{HRD}$/HRD, or PB11 | 47 | $GND_P$ | 72 | A0 |
| 23 | $\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15 | 48 | $GND_{P1}$ | 73 | A1 |
| 24 | $\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, or PB14 | 49 | Not Connected (NC), reserved | 74 | $V_{CCA}$ |
| 25 | $V_{CCS}$ | 50 | AA3/$\overline{RAS3}$ | 75 | $GND_A$ |

**Preliminary Data**

**Table 3-1** DSP56304 TQFP Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|---|---|
| 76 | A2 | 99 | A17 | 122 | D16 |
| 77 | A3 | 100 | D0 | 123 | D17 |
| 78 | A4 | 101 | D1 | 124 | D18 |
| 79 | A5 | 102 | D2 | 125 | D19 |
| 80 | $V_{CCA}$ | 103 | $V_{CCD}$ | 126 | $V_{CCQ}$ |
| 81 | $GND_A$ | 104 | $GND_D$ | 127 | $GND_Q$ |
| 82 | A6 | 105 | D3 | 128 | D20 |
| 83 | A7 | 106 | D4 | 129 | $V_{CCD}$ |
| 84 | A8 | 107 | D5 | 130 | $GND_D$ |
| 85 | A9 | 108 | D6 | 131 | D21 |
| 86 | $V_{CCA}$ | 109 | D7 | 132 | D22 |
| 87 | $GND_A$ | 110 | D8 | 133 | D23 |
| 88 | A10 | 111 | $V_{CCD}$ | 134 | MODD/$\overline{IRQD}$ |
| 89 | A11 | 112 | $GND_D$ | 135 | MODC/$\overline{IRQC}$ |
| 90 | $GND_Q$ | 113 | D9 | 136 | MODB/$\overline{IRQB}$ |
| 91 | $V_{CCQ}$ | 114 | D10 | 137 | MODA/$\overline{IRQA}$ |
| 92 | A12 | 115 | D11 | 138 | $\overline{TRST}$ |
| 93 | A13 | 116 | D12 | 139 | TDO |
| 94 | A14 | 117 | D13 | 140 | TDI |
| 95 | $V_{CCA}$ | 118 | D14 | 141 | TCK |
| 96 | $GND_A$ | 119 | $V_{CCD}$ | 142 | TMS |
| 97 | A15 | 120 | $GND_D$ | 143 | SC12 or PD2 |
| 98 | A16 | 121 | D15 | 144 | SC11 or PD1 |

Note: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, Pin 34 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin.

**Preliminary Data**

**Table 3-2** DSP56304 TQFP Signal Identification by Name

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| A0 | 72 | $\overline{BG}$ | 71 | D7 | 109 |
| A1 | 73 | $\overline{BR}$ | 63 | D8 | 110 |
| A10 | 88 | $\overline{CAS}$ | 52 | D9 | 113 |
| A11 | 89 | CLKOUT | 59 | $\overline{DE}$ | 5 |
| A12 | 92 | D0 | 100 | EXTAL | 55 |
| A13 | 93 | D1 | 101 | $GND_A$ | 75 |
| A14 | 94 | D10 | 114 | $GND_A$ | 81 |
| A15 | 97 | D11 | 115 | $GND_A$ | 87 |
| A16 | 98 | D12 | 116 | $GND_A$ | 96 |
| A17 | 99 | D13 | 117 | $GND_C$ | 58 |
| A2 | 76 | D14 | 118 | $GND_C$ | 66 |
| A3 | 77 | D15 | 121 | $GND_D$ | 104 |
| A4 | 78 | D16 | 122 | $GND_D$ | 112 |
| A5 | 79 | D17 | 123 | $GND_D$ | 120 |
| A6 | 82 | D18 | 124 | $GND_D$ | 130 |
| A7 | 83 | D19 | 125 | $GND_H$ | 39 |
| A8 | 84 | D2 | 102 | $GND_P$ | 47 |
| A9 | 85 | D20 | 128 | $GND_{P1}$ | 48 |
| AA0 | 70 | D21 | 131 | $GND_Q$ | 19 |
| AA1 | 69 | D22 | 132 | $GND_Q$ | 54 |
| AA2 | 51 | D23 | 133 | $GND_Q$ | 90 |
| AA3 | 50 | D3 | 105 | $GND_Q$ | 127 |
| $\overline{BB}$ | 64 | D4 | 106 | $GND_S$ | 9 |
| BCLK | 60 | D5 | 107 | $GND_S$ | 26 |
| $\overline{BCLK}$ | 61 | D6 | 108 | H0 | 43 |

**Table 3-2** DSP56304 TQFP Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| H1 | 42 | $\overline{\text{HRD}}$/HRD | 22 | PB2 | 41 |
| H2 | 41 | $\overline{\text{HREQ}}$/HREQ | 24 | PB3 | 40 |
| H3 | 40 | $\overline{\text{HRRQ}}$/HRRQ | 23 | PB4 | 37 |
| H4 | 37 | HRW | 22 | PB5 | 36 |
| H5 | 36 | $\overline{\text{HTRQ}}$/HTRQ | 24 | PB6 | 35 |
| H6 | 35 | $\overline{\text{HWR}}$/HWR | 21 | PB7 | 34 |
| H7 | 34 | $\overline{\text{IRQA}}$ | 137 | PB8 | 33 |
| HA0 | 33 | $\overline{\text{IRQB}}$ | 136 | PB9 | 32 |
| HA1 | 32 | $\overline{\text{IRQC}}$ | 135 | PC0 | 12 |
| HA10 | 30 | $\overline{\text{IRQD}}$ | 134 | PC1 | 4 |
| HA2 | 31 | MODA | 137 | PC2 | 3 |
| HA8 | 32 | MODB | 136 | PC3 | 17 |
| HA9 | 31 | MODC | 135 | PC4 | 7 |
| $\overline{\text{HACK}}$/HACK | 23 | MODD | 134 | PC5 | 10 |
| HAD0 | 43 | NC | 20 | PCAP | 46 |
| HAD1 | 42 | $\overline{\text{NMI}}$ | 6 | PD0 | 11 |
| HAD2 | 41 | NC | 49 | PD1 | 144 |
| HAD3 | 40 | PB0 | 43 | PD2 | 143 |
| HAD4 | 37 | PB1 | 42 | PD3 | 16 |
| HAD5 | 36 | PB10 | 31 | PD4 | 1 |
| HAD6 | 35 | PB11 | 22 | PD5 | 2 |
| HAD7 | 34 | PB12 | 21 | PE0 | 13 |
| HAS | 33 | PB13 | 30 | PE1 | 14 |
| HCS/HCS | 30 | PB14 | 24 | PE2 | 15 |
| HDS/HDS | 21 | PB15 | 23 | PINIT | 6 |

**Preliminary Data**

Table 3-2 DSP56304 TQFP Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| $\overline{RAS0}$ | 70 | SRD1 | 1 | $V_{CCC}$ | 57 |
| $\overline{RAS1}$ | 69 | STD0 | 10 | $V_{CCC}$ | 65 |
| $\overline{RAS2}$ | 51 | STD1 | 2 | $V_{CCD}$ | 103 |
| $\overline{RAS3}$ | 50 | $\overline{TA}$ | 62 | $V_{CCD}$ | 111 |
| $\overline{RD}$ | 68 | TCK | 141 | $V_{CCD}$ | 119 |
| $\overline{RESET}$ | 44 | TDI | 140 | $V_{CCD}$ | 129 |
| RXD | 13 | TDO | 139 | $V_{CCH}$ | 38 |
| SC00 | 12 | TIO0 | 29 | $V_{CCP}$ | 45 |
| SC01 | 4 | TIO1 | 28 | $V_{CCQ}$ | 18 |
| SC02 | 3 | TIO2 | 27 | $V_{CCQ}$ | 56 |
| SC10 | 11 | TMS | 142 | $V_{CCQ}$ | 91 |
| SC11 | 144 | $\overline{TRST}$ | 138 | $V_{CCQ}$ | 126 |
| SC12 | 143 | TXD | 14 | $V_{CCS}$ | 8 |
| SCK0 | 17 | $V_{CCA}$ | 74 | $V_{CCS}$ | 25 |
| SCK1 | 16 | $V_{CCA}$ | 80 | $\overline{WR}$ | 67 |
| SCLK | 15 | $V_{CCA}$ | 86 | XTAL | 53 |
| SRD0 | 7 | $V_{CCA}$ | 95 | | |

**Preliminary Data**

## TQFP Package Mechanical Drawing



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5-1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCULDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLED DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.

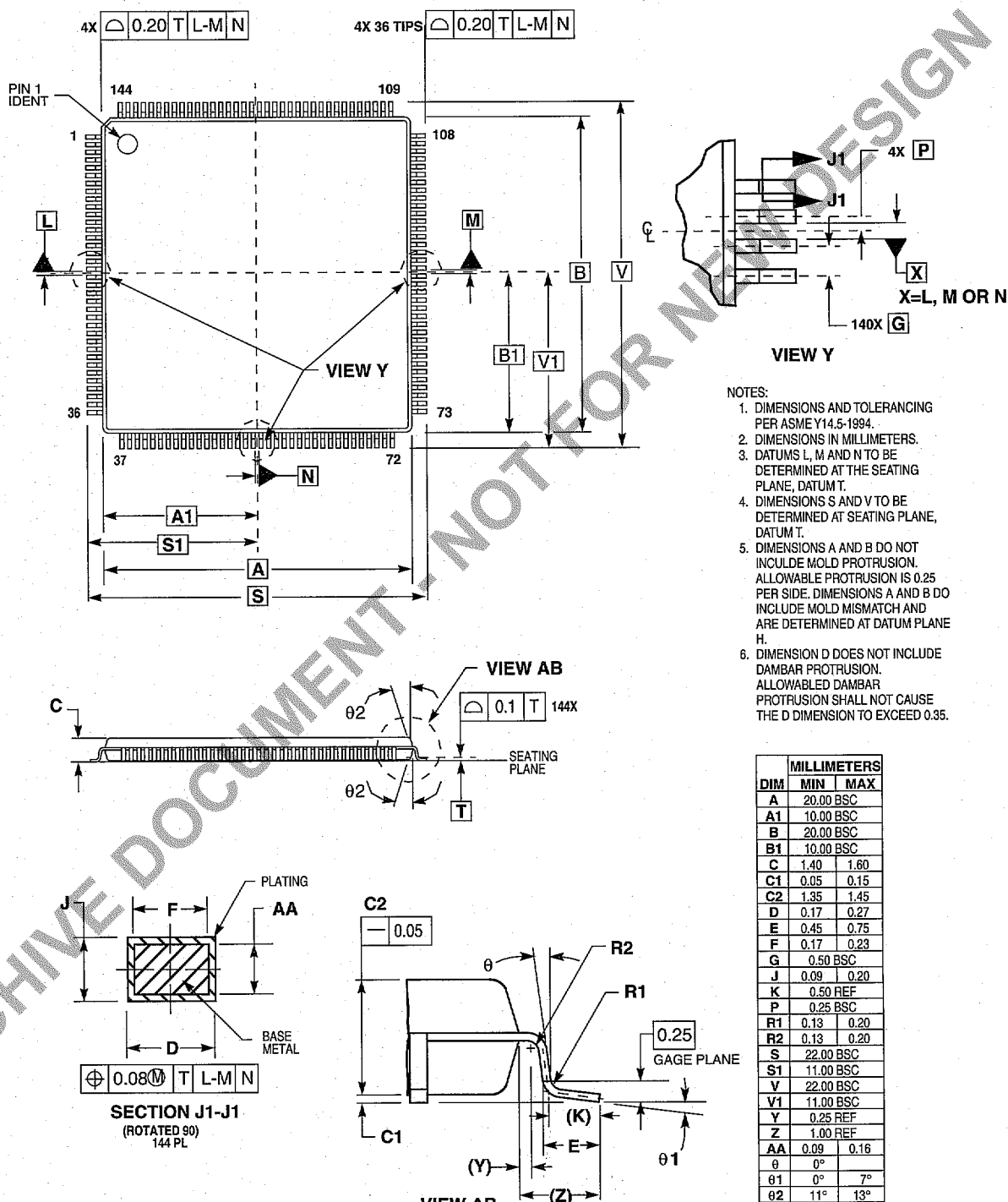| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 20.00 BSC | |
| A1 | 10.00 BSC | |
| B | 20.00 BSC | |
| B1 | 10.00 BSC | |
| C | 1.40 | 1.60 |
| C1 | 0.05 | 0.15 |
| C2 | 1.35 | 1.45 |
| D | 0.17 | 0.27 |
| E | 0.45 | 0.75 |
| F | 0.17 | 0.23 |
| G | 0.50 BSC | |
| J | 0.09 | 0.20 |
| K | 0.50 REF | |
| P | 0.25 BSC | |
| R1 | 0.13 | 0.20 |
| R2 | 0.13 | 0.20 |
| S | 22.00 BSC | |
| S1 | 11.00 BSC | |
| V | 22.00 BSC | |
| V1 | 11.00 BSC | |
| Y | 0.25 REF | |
| Z | 1.00 REF | |
| AA | 0.09 | 0.16 |
| θ | 0° | |
| θ1 | 0° | 7° |
| θ2 | 11° | 13° |

Case 918-03

**Figure 3-3** DSP56304 Mechanical Information, 144-pin TQFP Package

**Preliminary Data**

## PBGA Package Description

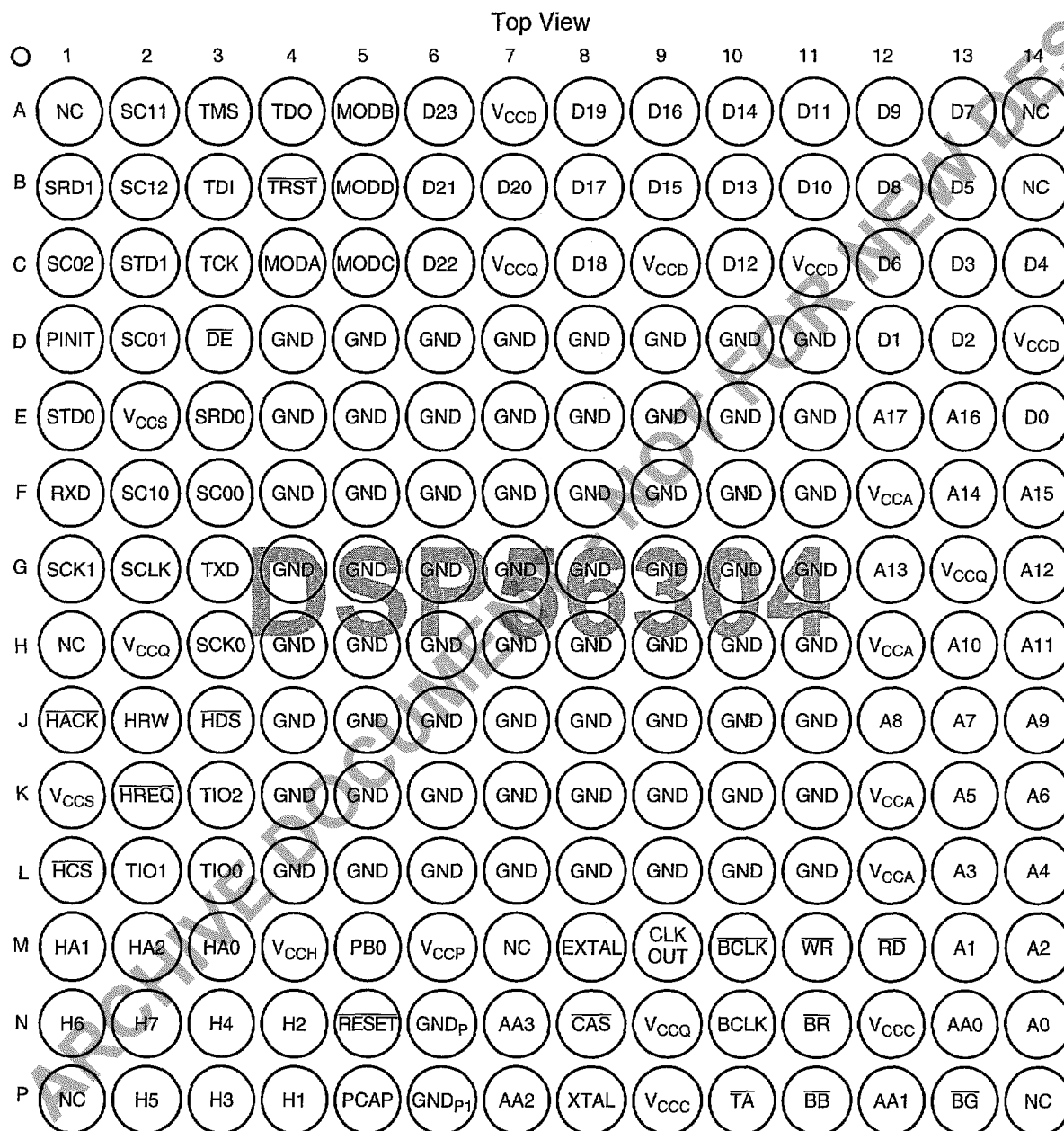Top and bottom views of the PBGA package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.

Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | SC11 | TMS | TDO | MODB | D23 | $V_{CCD}$ | D19 | D16 | D14 | D11 | D9 | D7 | NC |
| B | SRD1 | SC12 | TDI | $\overline{TRST}$ | MODD | D21 | D20 | D17 | D15 | D13 | D10 | D8 | D5 | NC |
| C | SC02 | STD1 | TCK | MODA | MODC | D22 | $V_{CCQ}$ | D18 | $V_{CCD}$ | D12 | $V_{CCD}$ | D6 | D3 | D4 |
| D | PINIT | SC01 | $\overline{DE}$ | GND | GND | GND | GND | GND | GND | GND | GND | D1 | D2 | $V_{CCD}$ |
| E | STD0 | $V_{CCS}$ | SRD0 | GND | GND | GND | GND | GND | GND | GND | GND | A17 | A16 | D0 |
| F | RXD | SC10 | SC00 | GND | GND | GND | GND | GND | GND | GND | GND | $V_{CCA}$ | A14 | A15 |
| G | SCK1 | SCLK | TXD | GND | GND | GND | GND | GND | GND | GND | GND | A13 | $V_{CCQ}$ | A12 |
| H | NC | $V_{CCQ}$ | SCK0 | GND | GND | GND | GND | GND | GND | GND | GND | $V_{CCA}$ | A10 | A11 |
| J | $\overline{HACK}$ | HRW | $\overline{HDS}$ | GND | GND | GND | GND | GND | GND | GND | GND | A8 | A7 | A9 |
| K | $V_{CCS}$ | $\overline{HREQ}$ | TIO2 | GND | GND | GND | GND | GND | GND | GND | GND | $V_{CCA}$ | A5 | A6 |
| L | $\overline{HCS}$ | TIO1 | TIO0 | GND | GND | GND | GND | GND | GND | GND | GND | $V_{CCA}$ | A3 | A4 |
| M | HA1 | HA2 | HA0 | $V_{CCH}$ | PB0 | $V_{CCP}$ | NC | EXTAL | CLK OUT | $\overline{BCLK}$ | $\overline{WR}$ | $\overline{RD}$ | A1 | A2 |
| N | H6 | H7 | H4 | H2 | $\overline{RESET}$ | $GND_P$ | AA3 | $\overline{CAS}$ | $V_{CCQ}$ | BCLK | $\overline{BR}$ | $V_{CCC}$ | AA0 | A0 |
| P | NC | H5 | H3 | H1 | PCAP | $GND_{P1}$ | AA2 | XTAL | $V_{CCC}$ | $\overline{TA}$ | $\overline{BB}$ | AA1 | $\overline{BG}$ | NC |

**Figure 3-4** DSP56304 Plastic Ball Grid Array (PBGA), Top View
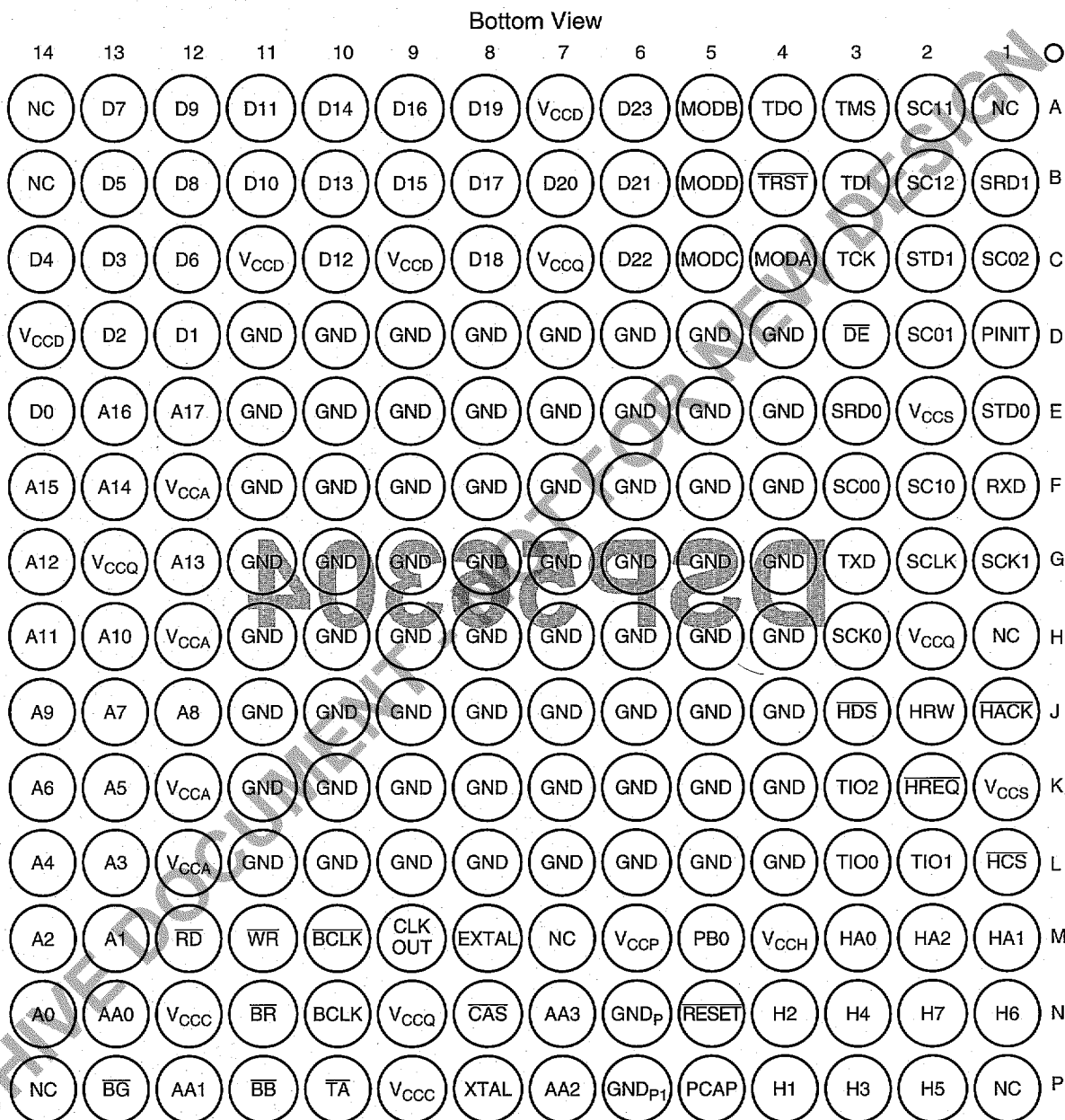
**Preliminary Data**

Bottom View



**Figure 3-5** DSP56304 Plastic Ball Grid Array (PBGA), Bottom View

**Table 3-3**  DSP56304 PBGA Signal Identification by Pin Number

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|---|---|
| A1 | Not Connected (NC), reserved | B12 | D8 | D9 | GND |
| A2 | SC11 or PD1 | B13 | D5 | D10 | GND |
| A3 | TMS | B14 | NC | D11 | GND |
| A4 | TDO | C1 | SC02 or PC2 | D12 | D1 |
| A5 | MODB/$\overline{\text{IRQB}}$ | C2 | STD1 or PD5 | D13 | D2 |
| A6 | D23 | C3 | TCK | D14 | $V_{CCD}$ |
| A7 | $V_{CCD}$ | C4 | MODA/$\overline{\text{IRQA}}$ | E1 | STD0 or PC5 |
| A8 | D19 | C5 | MODC/$\overline{\text{IRQC}}$ | E2 | $V_{CCS}$ |
| A9 | D16 | C6 | D22 | E3 | SRD0 or PC4 |
| A10 | D14 | C7 | $V_{CCQ}$ | E4 | GND |
| A11 | D11 | C8 | D18 | E5 | GND |
| A12 | D9 | C9 | $V_{CCD}$ | E6 | GND |
| A13 | D7 | C10 | D12 | E7 | GND |
| A14 | NC | C11 | $V_{CCD}$ | E8 | GND |
| B1 | SRD1 or PD4 | C12 | D6 | E9 | GND |
| B2 | SC12 or PD2 | C13 | D3 | E10 | GND |
| B3 | TDI | C14 | D4 | E11 | GND |
| B4 | $\overline{\text{TRST}}$ | D1 | PINIT/$\overline{\text{NMI}}$ | E12 | A17 |
| B5 | MODD/$\overline{\text{IRQD}}$ | D2 | SC01 or PC1 | E13 | A16 |
| B6 | D21 | D3 | $\overline{\text{DE}}$ | E14 | D0 |
| B7 | D20 | D4 | GND | F1 | RXD or PE0 |
| B8 | D17 | D5 | GND | F2 | SC10 or PD0 |
| B9 | D15 | D6 | GND | F3 | SC00 or PC0 |
| B10 | D13 | D7 | GND | F4 | GND |
| B11 | D10 | D8 | GND | F5 | GND |

**Preliminary Data**

**Table 3-3** DSP56304 PBGA Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------|---------|-------------|---------|-------------|
| F6 | GND | H3 | SCK0 or PC3 | J14 | A9 |
| F7 | GND | H4 | GND | K1 | $V_{CCS}$ |
| F8 | GND | H5 | GND | K2 | $\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, or PB14 |
| F9 | GND | H6 | GND | K3 | TIO2 |
| F10 | GND | H7 | GND | K4 | GND |
| F11 | GND | H8 | GND | K5 | GND |
| F12 | $V_{CCA}$ | H9 | GND | K6 | GND |
| F13 | A14 | H10 | GND | K7 | GND |
| F14 | A15 | H11 | GND | K8 | GND |
| G1 | SCK1 or PD3 | H12 | $V_{CCA}$ | K9 | GND |
| G2 | SCLK or PE2 | H13 | A10 | K10 | GND |
| G3 | TXD or PE1 | H14 | A11 | K11 | GND |
| G4 | GND | J1 | $\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15 | K12 | $V_{CCA}$ |
| G5 | GND | J2 | HRW, $\overline{HRD}$/HRD, or PB11 | K13 | A5 |
| G6 | GND | J3 | $\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12 | K14 | A6 |
| G7 | GND | J4 | GND | L1 | $\overline{HCS}$/HCS, HA10, or PB13 |
| G8 | GND | J5 | GND | L2 | TIO1 |
| G9 | GND | J6 | GND | L3 | TIO0 |
| G10 | GND | J7 | GND | L4 | GND |
| G11 | GND | J8 | GND | L5 | GND |
| G12 | A13 | J9 | GND | L6 | GND |
| G13 | $V_{CCQ}$ | J10 | GND | L7 | GND |
| G14 | A12 | J11 | GND | L8 | GND |
| H1 | NC | J12 | A8 | L9 | GND |
| H2 | $V_{CCQ}$ | J13 | A7 | L10 | GND |

**Preliminary Data**

**Table 3-3** DSP56304 PBGA Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|---|---|
| L11 | GND | M13 | A1 | P1 | NC |
| L12 | $V_{CCA}$ | M14 | A2 | P2 | H5, HAD5, or PB5 |
| L13 | A3 | N1 | H6, HAD6, or PB6 | P3 | H3, HAD3, or PB3 |
| L14 | A4 | N2 | H7, HAD7, or PB7 | P4 | H1, HAD1, or PB1 |
| M1 | HA1, HA8, or PB9 | N3 | H4, HAD4, or PB4 | P5 | PCAP |
| M2 | HA2, HA9, or PB10 | N4 | H2, HAD2, or PB2 | P6 | $GND_{P1}$ |
| M3 | HA0, $\overline{HAS}$/HAS, or PB8 | N5 | $\overline{RESET}$ | P7 | AA2/$\overline{RAS2}$ |
| M4 | $V_{CCH}$ | N6 | $GND_P$ | P8 | XTAL |
| M5 | H0, HAD0, or PB0 | N7 | AA3/$\overline{RAS3}$ | P9 | $V_{CCC}$ |
| M6 | $V_{CCP}$ | N8 | $\overline{CAS}$ | P10 | $\overline{TA}$ |
| M7 | NC | N9 | $V_{CCQ}$ | P11 | $\overline{BB}$ |
| M8 | EXTAL | N10 | BCLK | P12 | AA1/$\overline{RAS1}$ |
| M9 | CLKOUT | N11 | $\overline{BR}$ | P13 | $\overline{BG}$ |
| M10 | $\overline{BCLK}$ | N12 | $V_{CCC}$ | P14 | NC |
| M11 | $\overline{WR}$ | N13 | AA0/$\overline{RAS0}$ | | |
| M12 | $\overline{RD}$ | N14 | A0 | | |

Note: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for $GND_P$ and $GND_{P1}$ that support the PLL, other GND signals do not support individual subsystems in the chip.

**Table 3-4** DSP56304 PBGA Signal Identification by Name

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| A0 | N14 | $\overline{BG}$ | P13 | D7 | A13 |
| A1 | M13 | $\overline{BR}$ | N11 | D8 | B12 |
| A10 | H13 | $\overline{CAS}$ | N8 | D9 | A12 |
| A11 | H14 | CLKOUT | M9 | $\overline{DE}$ | D3 |
| A12 | G14 | D0 | E14 | EXTAL | M8 |
| A13 | G12 | D1 | D12 | GND | D4 |
| A14 | F13 | D10 | B11 | GND | D5 |
| A15 | F14 | D11 | A11 | GND | D6 |
| A16 | E13 | D12 | C10 | GND | D7 |
| A17 | E12 | D13 | B10 | GND | D8 |
| A2 | M14 | D14 | A10 | GND | D9 |
| A3 | L13 | D15 | B9 | GND | D10 |
| A4 | L14 | D16 | A9 | GND | D11 |
| A5 | K13 | D17 | B8 | GND | E4 |
| A6 | K14 | D18 | C8 | GND | E5 |
| A7 | J13 | D19 | A8 | GND | E6 |
| A8 | J12 | D2 | D13 | GND | E7 |
| A9 | J14 | D20 | B7 | GND | E8 |
| AA0 | N13 | D21 | B6 | GND | E9 |
| AA1 | P12 | D22 | C6 | GND | E10 |
| AA2 | P7 | D23 | A6 | GND | E11 |
| AA3 | N7 | D3 | C13 | GND | F4 |
| $\overline{BB}$ | P11 | D4 | C14 | GND | F5 |
| $\overline{BCLK}$ | M10 | D5 | B13 | GND | F6 |
| BCLK | N10 | D6 | C12 | GND | F7 |

**Preliminary Data**

**Table 3-4** DSP56304 PBGA Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| GND | F8 | GND | J9 | H4 | N3 |
| GND | F9 | GND | J10 | H5 | P2 |
| GND | F10 | GND | J11 | H6 | N1 |
| GND | F11 | GND | K4 | H7 | N2 |
| GND | G4 | GND | K5 | HA0 | M3 |
| GND | G5 | GND | K6 | HA1 | M1 |
| GND | G6 | GND | K7 | HA10 | L1 |
| GND | G7 | GND | K8 | HA2 | M2 |
| GND | G8 | GND | K9 | HA8 | M1 |
| GND | G9 | GND | K10 | HA9 | M2 |
| GND | G10 | GND | K11 | $\overline{\text{HACK}}$/HACK | J1 |
| GND | G11 | GND | L4 | HAD0 | M5 |
| GND | H4 | GND | L5 | HAD1 | P4 |
| GND | H5 | GND | L6 | HAD2 | N4 |
| GND | H6 | GND | L7 | HAD3 | P3 |
| GND | H7 | GND | L8 | HAD4 | N3 |
| GND | H8 | GND | L9 | HAD5 | P2 |
| GND | H9 | GND | L10 | HAD6 | N1 |
| GND | H10 | GND | L11 | HAD7 | N2 |
| GND | H11 | GND$_P$ | N6 | $\overline{\text{HAS}}$/HAS | M3 |
| GND | J4 | GND$_{P1}$ | P6 | $\overline{\text{HCS}}$/HCS | L1 |
| GND | J5 | H0 | M5 | $\overline{\text{HDS}}$/HDS | J3 |
| GND | J6 | H1 | P4 | $\overline{\text{HRD}}$/HRD | J2 |
| GND | J7 | H2 | N4 | $\overline{\text{HREQ}}$/HREQ | K2 |
| GND | J8 | H3 | P3 | $\overline{\text{HRRQ}}$/HRRQ | J1 |

**Preliminary Data**

**Table 3-4**  DSP56304 PBGA Signal Identification by Name  (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| HRW | J2 | PB14 | K2 | PE2 | G2 |
| $\overline{\text{HTRQ}}$/HTRQ | K2 | PB15 | J1 | PINIT | D1 |
| $\overline{\text{HWR}}$/HWR | J3 | PB2 | N4 | $\overline{\text{RAS0}}$ | N13 |
| $\overline{\text{IRQA}}$ | C4 | PB3 | P3 | $\overline{\text{RAS1}}$ | P12 |
| $\overline{\text{IRQB}}$ | A5 | PB4 | N3 | $\overline{\text{RAS2}}$ | P7 |
| $\overline{\text{IRQC}}$ | C5 | PB5 | P2 | $\overline{\text{RAS3}}$ | N7 |
| $\overline{\text{IRQD}}$ | B5 | PB6 | N1 | $\overline{\text{RD}}$ | M12 |
| MODA | C4 | PB7 | N2 | $\overline{\text{RESET}}$ | N5 |
| MODB | A5 | PB8 | M3 | RXD | F1 |
| MODC | C5 | PB9 | M1 | SC00 | F3 |
| MODD | B5 | PC0 | F3 | SC01 | D2 |
| NC | A1 | PC1 | D2 | SC02 | C1 |
| NC | A14 | PC2 | C1 | SC10 | F2 |
| NC | B14 | PC3 | H3 | SC11 | A2 |
| NC | H1 | PC4 | E3 | SC12 | B2 |
| NC | M7 | PC5 | E1 | SCK0 | H3 |
| NC | P1 | PCAP | P5 | SCK1 | G1 |
| NC | P14 | PD0 | F2 | SCLK | G2 |
| $\overline{\text{NMI}}$ | D1 | PD1 | A2 | SRD0 | E3 |
| PB0 | M5 | PD2 | B2 | SRD1 | B1 |
| PB1 | P4 | PD3 | G1 | STD0 | E1 |
| PB10 | M2 | PD4 | B1 | STD1 | C2 |
| PB11 | J2 | PD5 | C2 | $\overline{\text{TA}}$ | P10 |
| PB12 | J3 | PE0 | F1 | TCK | C3 |
| PB13 | L1 | PE1 | G3 | TDI | B3 |

**Preliminary Data**

**Table 3-4** DSP56304 PBGA Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---|---|---|---|---|---|
| TDO | A4 | $V_{CCA}$ | K12 | $V_{CCP}$ | M6 |
| TIO0 | L3 | $V_{CCA}$ | L12 | $V_{CCQ}$ | C7 |
| TIO1 | L2 | $V_{CCC}$ | N12 | $V_{CCQ}$ | G13 |
| TIO2 | K3 | $V_{CCC}$ | P9 | $V_{CCQ}$ | H2 |
| TMS | A3 | $V_{CCD}$ | A7 | $V_{CCQ}$ | N9 |
| $\overline{TRST}$ | B4 | $V_{CCD}$ | C9 | $V_{CCS}$ | E2 |
| TXD | G3 | $V_{CCD}$ | C11 | $V_{CCS}$ | K1 |
| $V_{CCA}$ | F12 | $V_{CCD}$ | D14 | $\overline{WR}$ | M11 |
| $V_{CCA}$ | H12 | $V_{CCH}$ | M4 | XTAL | P8 |

**Preliminary Data**

## PBGA Package Mechanical Drawing



| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.32 | 1.75 |
| A1 | 0.27 | 0.47 |
| A2 | 0.30 | 0.40 |
| A3 | 0.75 | 0.88 |
| b | 0.35 | 0.65 |
| D | 15.00 BSC | |
| D1 | 13.00 BSC | |
| D2 | 12.00 | 15.00 |
| E | 15.00 BSC | |
| E1 | 13.00 BSC | |
| E2 | 12.00 | 15.00 |
| e | 1.00 BSC | |
| R1 | — | 2.00 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

**TOP VIEW**

**BOTTOM VIEW**

**TOP VIEW**
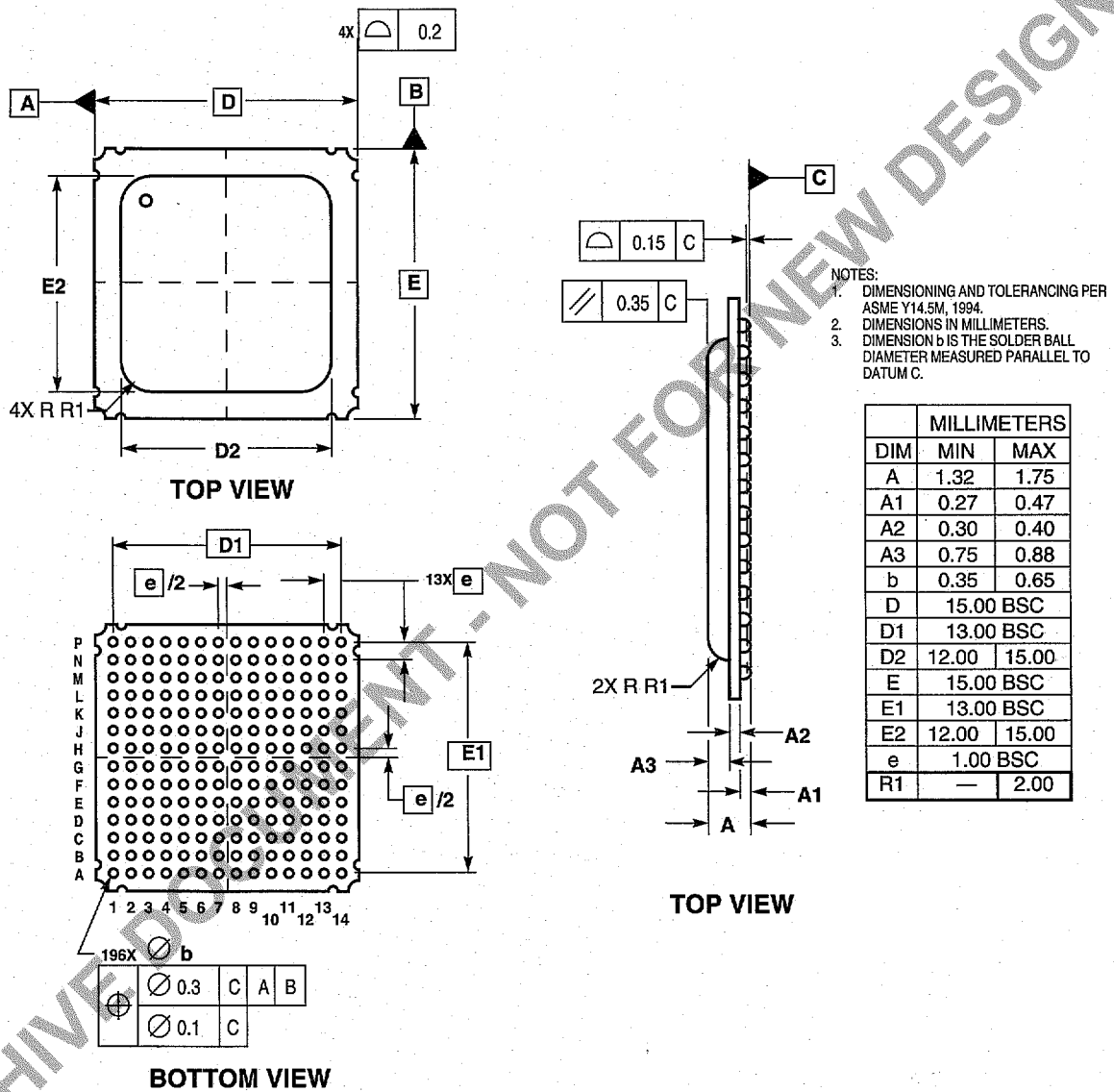
CASE 1128-01

**Figure 3-6** DSP56304 Mechanical Information, 196-pin PBGA Package

**Preliminary Data**

# ORDERING DRAWINGS

All devices manufactured by Motorola conform to current JEDEC standards. Complete mechanical information regarding DSP56304 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

> **(602) 244-6591**

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code

- The caller's Personal Identification Number (PIN)

**Note:** For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:

  - Instructions for using the system

  - A literature order form

  - Specific part technical information or data sheets

  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56304 144-pin TQFP package mechanical drawing is referenced as 918-03. The reference number for the 196-pin PBGA package is 1128-01.

# SECTION 4

# DESIGN CONSIDERATIONS

## THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the equation:

**Equation 1:** $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

$T_A$ = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$P_D$ = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

**Equation 2:** $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

**Preliminary Data**

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.

- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.

- If the temperature of the package case ($T_T$) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or $\Psi_{JT}$, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

# ELECTRICAL DESIGN CONSIDERATIONS

> **CAUTION**
>
> **This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$).**

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each $V_{CC}$ pin on the DSP, and from the board ground to each GND pin.

- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the $V_{CC}$ power source to GND.

- Ensure that capacitor leads and associated printed circuit traces that connect to the chip $V_{CC}$ and GND pins are less than 0.5 in per capacitor lead.

- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for $V_{CC}$ and GND.

- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{TA}$, and $\overline{BG}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the $V_{CC}$ and GND circuits.

- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors ($\overline{TRST}$, TMS, $\overline{DE}$).

**Preliminary Data**

- Take special care to minimize noise levels on the $V_{CCP}$, $GND_P$, and $GND_{P1}$ pins.

- The following pins must be asserted after power-up: $\overline{RESET}$ and $\overline{TRST}$ (See note 4 in **Table 2-7**).

- If multiple DSP56304 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.

# POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is Alternating Current (AC), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the formula:

**Equation 3:** $I = C \times V \times f$

where: 
C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

**Example 4-1** Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is:

**Equation 4:** $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^6 = 5.48 \text{ mA}$

The Maximum Internal Current ($I_{CCI}max$) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The Typical Internal Current ($I_{CCItyp}$) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption:

- Set the EBD bit when not accessing external memory.

- Minimize external memory accesses, and use internal memory accesses.

- Minimize the number of pins that are switching.

**Preliminary Data**

- Minimize the capacitive load on the pins.

- Connect the unused inputs to pull-up or pull-down resistors. Unused output pins may be left unconnected. Unused GPIO pins may either be connected to pull-up or pull-down resistors, or defined as outputs and left unconnected.

- Disable unused peripherals.

- Disable unused pin activity (e.g., CLKOUT, XTAL).

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value:

**Equation 5:**  $I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$

where:  $I_{typF2}$ = current at F2
$I_{typF1}$ = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

**Note:** F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

# PLL PERFORMANCE ISSUES

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

## Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2** on page 2-7, for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not

**Preliminary Data**

guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

## Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

## Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and approximately 2%. For large MF (MF > 500), the frequency jitter is 2–3%.

## Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

# SECTION 5

# ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

**Table 5-1** Ordering Information

| Part | Supply Voltage | Package Type | Pin Count | Frequency (MHz) | Order Number |
|------|----------------|--------------|-----------|-----------------|--------------|
| DSP56304 | 3 V | Thin Quad Flat Pack (TQFP) | 144 | 66 | DSP56304PV66 |
| DSP56304 | 3 V | Thin Quad Flat Pack (TQFP) | 144 | 80 | DSP56304PV80 |
| DSP56304 | 3 V | Plastic Ball Grid Array (PBGA) | 196 | 66 | DSP56304GC66 |
| DSP56304 | 3 V | Plastic Ball Grid Array (PBGA) | 196 | 80 | DSP56304GC80 |

**Preliminary Data**

# APPENDIX A

# POWER CONSUMPTION BENCHMARK

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*******************************************************************
;*******************************************************************
;*                                                                 *
;* CHECKS   Typical Power Consumption                              *
;*                                                                 *
;*******************************************************************

          page      200,55,0,0,0
          nolist

I_VEC EQU $000000   ; Interrupt vectors for program debug only
START EQU $8000     ; MAIN (external) program starting address
INT_PROG  EQU $100  ; INTERNAL program memory starting address
INT_XDAT  EQU $0    ; INTERNAL X-data memory starting address
INT_YDAT  EQU $0    ; INTERNAL Y-data memory starting address

          INCLUDE "ioequ.asm"
          INCLUDE "intequ.asm"

          list

          org       P:START

          movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Area 2 : 0 w.s (SSRAM)
; Default: 1 w.s (SRAM)
;
          movep     #$0d0000,x:M_PCTL         ; XTAL disable
                              ; PLL enable
                              ; CLKOUT disable

;
; Load the program
;
          move      #INT_PROG,r0
          move      #PROG_START,r1
          do        #(PROG_END-PROG_START),PLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,p:(r0)+
          nop
PLOAD_LOOP
;
```

**Preliminary Data**

```
; Load the X-data
;
          move      #INT_XDAT,r0
          move      #XDAT_START,r1
          do        #(XDAT_END-XDAT_START),XLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
          move      #INT_YDAT,r0
          move      #YDAT_START,r1
          do        #(YDAT_END-YDAT_START),YLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,y:(r0)+
YLOAD_LOOP
;

          jmp       INT_PROG

PROG_START
          move      #$0,r0
          move      #$0,r4
          move      #$3f,m0
          move      #$3f,m4
;
          clr       a
          clr       b
          move      #$0,x0
          move      #$0,x1
          move      #$0,y0
          move      #$0,y1
          bset      #4,omr                ; ebd
;
sbr       dor       #60,_end
          mac       x0,y0,a   x:(r0)+,x1        y:(r4)+,y1
          mac       x1,y1,a   x:(r0)+,x0        y:(r4)+,y0
          add       a,b
          mac       x0,y0,a   x:(r0)+,x1
          mac       x1,y1,a                     y:(r4)+,y0
          move      b1,x:$ff
_end
          bra       sbr
          nop
          nop
          nop
          nop
PROG_END
          nop
          nop
```

**Preliminary Data**

```
XDAT_START
;           org     x:0
            dc      $262EB9
            dc      $86F2FE
            dc      $E56A5F
            dc      $616CAC
            dc      $8FFD75
            dc      $9210A
            dc      $A06D7B
            dc      $CEA798
            dc      $8DFBF1
            dc      $A063D6
            dc      $6C6657
            dc      $C2A544
            dc      $A3662D
            dc      $A4E762
            dc      $84F0F3
            dc      $E6F1B0
            dc      $B3829
            dc      $8BF7AE
            dc      $63A94F
            dc      $EF78DC
            dc      $242DE5
            dc      $A3E0BA
            dc      $EBAB6B
            dc      $8726C8
            dc      $CA361
            dc      $2F6E86
            dc      $A57347
            dc      $4BE774
            dc      $8F349D
            dc      $A1ED12
            dc      $4BFCE3
            dc      $EA26E0
            dc      $CD7D99
            dc      $4BA85E
            dc      $27A43F
            dc      $A8B10C
            dc      $D3A55
            dc      $25EC6A
            dc      $2A255B
            dc      $A5F1F8
            dc      $2426D1
            dc      $AE6536
            dc      $CBBC37
            dc      $6235A4
            dc      $37F0D
            dc      $63BEC2
            dc      $A5E4D3
            dc      $8CE810
            dc      $3FF09
            dc      $60E50E
            dc      $CFFB2F
```

**Preliminary Data**

```
            dc          $40753C
            dc          $8262C5
            dc          $CA641A
            dc          $EB3B4B
            dc          $2DA928
            dc          $AB6641
            dc          $28A7E6
            dc          $4E2127
            dc          $482FD4
            dc          $7257D
            dc          $E53C72
            dc          $1A8C3
            dc          $E27540
XDAT_END

YDAT_START
;           org         y:0
            dc          $5B6DA
            dc          $C3F70B
            dc          $6A39E8
            dc          $81E801
            dc          $C666A6
            dc          $46F8E7
            dc          $AAEC94
            dc          $24233D
            dc          $802732
            dc          $2E3C83
            dc          $A43E00
            dc          $C2B639
            dc          $85A47E
            dc          $ABFDDF
            dc          $F3A2C
            dc          $2D7CF5
            dc          $E16A8A
            dc          $ECB8FB
            dc          $4BED18
            dc          $43F371
            dc          $83A556
            dc          $E1E9D7
            dc          $ACA2C4
            dc          $8135AD
            dc          $2CE0E2
            dc          $8F2C73
            dc          $432730
            dc          $A87FA9
            dc          $4A292E
            dc          $A63CCF
            dc          $6BA65C
            dc          $E06D65
            dc          $1AA3A
            dc          $A1B6EB
            dc          $48AC48
            dc          $EF7AE1
```

**Preliminary Data**

```
                    dc        $6E3006
                    dc        $62F6C7
                    dc        $6064F4
                    dc        $87E41D
                    dc        $CB2692
                    dc        $2C3863
                    dc        $C6BC60
                    dc        $43A519
                    dc        $6139DE
                    dc        $ADF7BF
                    dc        $4B3E8C
                    dc        $6079D5
                    dc        $E0F5EA
                    dc        $8230DB
                    dc        $A3B778
                    dc        $2BFE51
                    dc        $E0A6B6
                    dc        $68FFB7
                    dc        $28F324
                    dc        $8F2E8D
                    dc        $667842
                    dc        $83E053
                    dc        $A1FD90
                    dc        $6B2689
                    dc        $85B68E
                    dc        $622EAF
                    dc        $6162BC
                    dc        $E4A245
YDAT_END


;********************************************************************************
;
;       EQUATES for DSP56304 I/O registers and ports
;
;       Last update: June 11 1995
;
;********************************************************************************

                    page      132,55,0,0,0
                    opt       mex

ioequ       ident   1,0


;-------------------------------------------------------------------------------
;
;       EQUATES for I/O Port Programming
;
;-------------------------------------------------------------------------------


;           Register Addresses

M_HDR EQU $FFFFC9   ; Host port GPIO data Register
M_HDDR EQU $FFFFC8  ; Host port GPIO direction Register
```

**Preliminary Data**

```
M_PCRC EQU $FFFFBF ; Port C Control Register
M_PRRC EQU $FFFFBE          ; Port C Direction Register
M_PDRC EQU $FFFFBD          ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF          ; Port D Control register
M_PRRD EQU $FFFFAE          ; Port D Direction Data Register
M_PDRD EQU $FFFFAD          ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F          ; Port E Control register
M_PRRE EQU $FFFF9E          ; Port E Direction Register
M_PDRE EQU $FFFF9D          ; Port E Data Register
M_OGDB EQU $FFFFFC          ; OnCE GDB Register


;-----------------------------------------------------------------
;
;          EQUATES for Host Interface
;
;-----------------------------------------------------------------

;          Register Addresses

M_HCR EQU $FFFFC2           ; Host Control Register
M_HSR EQU $FFFFC3           ; Host Status Rgister
M_HPCR EQU $FFFFC4          ; Host Polarity Control Register
M_HBAR EQU $FFFFC5          ; Host Base Address Register
M_HRX EQU $FFFFC6           ; Host Receive Register
M_HTX EQU $FFFFC7           ; Host Transmit Register


;          HCR bits definition
M_HRIE EQU $0               ; Host Receive interrupts Enable
M_HTIE EQU $1               ; Host Transmit Interrupt Enable
M_HCIE EQU $2               ; Host Command Interrupt Enable
M_HF2 EQU $3                ; Host Flag 2
M_HF3 EQU $4                ; Host Flag 3


;          HSR bits definition
M_HRDF EQU $0               ; Host Receive Data Full
M_HTDE EQU $1               ; Host Receive Data Emptiy
M_HCP EQU $2                ; Host Command Pending
M_HF0 EQU $3                ; Host Flag 0
M_HF1 EQU $4                ; Host Flag 1


;          HPCR bits definition
M_HGEN EQU $0               ; Host Port GPIO Enable
M_HA8EN EQU $1              ; Host Address 8 Enable
M_HA9EN EQU $2              ; Host Address 9 Enable
M_HCSEN EQU $3             ; Host Chip Select Enable
M_HREN EQU $4              ; Host Request Enable
M_HAEN EQU $5              ; Host Acknowledge Enable
M_HEN EQU $6               ; Host Enable
M_HOD EQU $8               ; Host Request Open Drain mode
M_HDSP EQU $9              ; Host Data Strobe Polarity
M_HASP EQU $A              ; Host Address Strobe Polarity
```

**Preliminary Data**

```
        M_HMUX EQU $B                    ; Host Multiplexed bus select
        M_HD_HS EQU $C                   ; Host Double/Single Strobe select
        M_HCSP EQU $D                    ; Host Chip Select Polarity
        M_HRP EQU $E                     ; Host Request PolarityPolarity
        M_HAP EQU $F                     ; Host Acknowledge Polarity



        ;-----------------------------------------------------------------
        ;
        ;          EQUATES for Serial Communications Interface (SCI)
        ;
        ;-----------------------------------------------------------------


        ;          Register Addresses

        M_STXH EQU $FFFF97               ; SCI Transmit Data Register (high)
        M_STXM EQU $FFFF96               ; SCI Transmit Data Register (middle)
        M_STXL EQU $FFFF95               ; SCI Transmit Data Register (low)
        M_SRXH EQU $FFFF9A               ; SCI Receive Data Register (high)
        M_SRXM EQU $FFFF99               ; SCI Receive Data Register (middle)
        M_SRXL EQU $FFFF98               ; SCI Receive Data Register (low)
        M_STXA EQU $FFFF94               ; SCI Transmit Address Register
        M_SCR EQU $FFFF9C                ; SCI Control Register
        M_SSR EQU $FFFF93                ; SCI Status Register
        M_SCCR EQU $FFFF9B               ; SCI Clock Control Register

        ;          SCI Control Register Bit Flags

        M_WDS EQU $7                     ; Word Select Mask (WDS0-WDS3)
        M_WDS0 EQU 0                     ; Word Select 0
        M_WDS1 EQU 1                     ; Word Select 1
        M_WDS2 EQU 2                     ; Word Select 2
        M_SSFTD EQU 3                    ; SCI Shift Direction
        M_SBK EQU 4                      ; Send Break
        M_WAKE EQU 5                     ; Wakeup Mode Select
        M_RWU EQU 6                      ; Receiver Wakeup Enable
        M_WOMS EQU 7                     ; Wired-OR Mode Select
        M_SCRE EQU 8                     ; SCI Receiver Enable
        M_SCTE EQU 9                     ; SCI Transmitter Enable
        M_ILIE EQU 10                    ; Idle Line Interrupt Enable
        M_SCRIE EQU 11                   ; SCI Receive Interrupt Enable
        M_SCTIE EQU 12                   ; SCI Transmit Interrupt Enable
        M_TMIE EQU 13                    ; Timer Interrupt Enable
        M_TIR EQU 14                     ; Timer Interrupt Rate
        M_SCKP EQU 15                    ; SCI Clock Polarity
        M_REIE EQU 16                    ; SCI Error Interrupt Enable (REIE)

        ;          SCI Status Register Bit Flags

        M_TRNE EQU 0                     ; Transmitter Empty
        M_TDRE EQU 1                     ; Transmit Data Register Empty
        M_RDRF EQU 2                     ; Receive Data Register Full
        M_IDLE EQU 3                     ; Idle Line Flag
```

**Preliminary Data**

```
M_OR  EQU 4                        ; Overrun Error Flag
M_PE  EQU 5                        ; Parity Error
M_FE  EQU 6                        ; Framing Error Flag
M_R8  EQU 7                        ; Received Bit 8 (R8) Address


;          SCI Clock Control Registe
r


M_CD  EQU $FFF                     ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                       ; Clock Out Divider
M_SCP EQU 13                       ; Clock Prescaler
M_RCM EQU 14                       ; Receive Clock Mode Source Bit
M_TCM EQU 15                       ; Transmit Clock Source Bit


;--------------------------------------------------------------------
;
;          EQUATES for Synchronous Serial Interface (SSI)
;
;--------------------------------------------------------------------


;
;          Register Addresses Of SSI0
M_TX00   EQU $FFFFBC               ; SSI0 Transmit Data Register 0
M_TX01   EQU $FFFFBB               ; SSIO Transmit Data Register 1
M_TX02   EQU $FFFFBA               ; SSIO Transmit Data Register 2
M_TSR0   EQU $FFFFB9               ; SSI0 Time Slot Register
M_RX0    EQU $FFFFB8               ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7               ; SSI0 Status Register
M_CRB0   EQU $FFFFB6               ; SSI0 Control Register B
M_CRA0   EQU $FFFFB5               ; SSI0 Control Register A
M_TSMA0  EQU $FFFFB4               ; SSI0 Transmit Slot Mask Register A
M_TSMB0  EQU $FFFFB3               ; SSI0 Transmit Slot Mask Register B
M_RSMA0  EQU $FFFFB2               ; SSI0 Receive Slot Mask Register A
M_RSMB0  EQU $FFFFB1               ; SSI0 Receive Slot Mask Register B


;          Register Addresses Of SSI1
M_TX10   EQU $FFFFAC               ; SSI1 Transmit Data Register 0
M_TX11   EQU $FFFFAB               ; SSI1 Transmit Data Register 1
M_TX12   EQU $FFFFAA               ; SSI1 Transmit Data Register 2
M_TSR1   EQU $FFFFA9               ; SSI1 Time Slot Register
M_RX1    EQU $FFFFA8               ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7               ; SSI1 Status Register
M_CRB1   EQU $FFFFA6               ; SSI1 Control Register B
M_CRA1   EQU $FFFFA5               ; SSI1 Control Register A
M_TSMA1  EQU $FFFFA4               ; SSI1 Transmit Slot Mask Register A
M_TSMB1  EQU $FFFFA3               ; SSI1 Transmit Slot Mask Register B
M_RSMA1  EQU $FFFFA2               ; SSI1 Receive Slot Mask Register A
M_RSMB1  EQU $FFFFA1               ; SSI1 Receive Slot Mask Register B


;          SSI Control Register A Bit Flags


M_PM  EQU $FF                      ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                       ; Prescaler Range
```

**Preliminary Data**

```
        M_DC EQU $1F000              ; Frame Rate Divider Control Mask (DC0-DC7)
        M_ALC EQU 18                 ; Alignment Control (ALC)
        M_WL EQU $380000             ; Word Length Control Mask (WL0-WL7)
        M_SSC1 EQU 22                ; Select SC1 as TR #0 drive enable (SSC1)


        ;       SSI Control Register B Bit Flags

        M_OF EQU $3                  ; Serial Output Flag Mask
        M_OF0 EQU 0                  ; Serial Output Flag 0
        M_OF1 EQU 1                  ; Serial Output Flag 1
        M_SCD EQU $1C                ; Serial Control Direction Mask
        M_SCD0 EQU 2                 ; Serial Control 0 Direction
        M_SCD1 EQU 3                 ; Serial Control 1 Direction
        M_SCD2 EQU 4                 ; Serial Control 2 Direction
        M_SCKD EQU 5                 ; Clock Source Direction
        M_SHFD EQU 6                 ; Shift Direction
        M_FSL EQU $180               ; Frame Sync Length Mask (FSL0-FSL1)
        M_FSL0 EQU 7                 ; Frame Sync Length 0
        M_FSL1 EQU 8                 ; Frame Sync Length 1
        M_FSR EQU 9                  ; Frame Sync Relative Timing
        M_FSP EQU 10                 ; Frame Sync Polarity
        M_CKP EQU 11                 ; Clock Polarity
        M_SYN EQU 12                 ; Sync/Async Control
        M_MOD EQU 13                 ; SSI Mode Select
        M_SSTE EQU $1C000            ; SSI Transmit enable Mask
        M_SSTE2 EQU 14               ; SSI Transmit #2 Enable
        M_SSTE1 EQU 15               ; SSI Transmit #1 Enable
        M_SSTE0 EQU 16               ; SSI Transmit #0 Enable
        M_SSRE EQU 17                ; SSI Receive Enable
        M_SSTIE EQU 18               ; SSI Transmit Interrupt Enable
        M_SSRIE EQU 19               ; SSI Receive Interrupt Enable
        M_STLIE EQU 20               ; SSI Transmit Last Slot Interrupt Enable
        M_SRLIE EQU 21               ; SSI Receive Last Slot Interrupt Enable
        M_STEIE EQU 22               ; SSI Transmit Error Interrupt Enable
        M_SREIE EQU 23               ; SI Receive Error Interrupt Enable


        ;       SSI Status Register Bit Flags

        M_IF EQU $3                  ; Serial Input Flag Mask
        M_IF0 EQU 0                  ; Serial Input Flag 0
        M_IF1 EQU 1                  ; Serial Input Flag 1
        M_TFS EQU 2                  ; Transmit Frame Sync Flag
        M_RFS EQU 3                  ; Receive Frame Sync Flag
        M_TUE EQU 4                  ; Transmitter Underrun Error FLag
        M_ROE EQU 5                  ; Receiver Overrun Error Flag
        M_TDE EQU 6                  ; Transmit Data Register Empty
        M_RDF EQU 7                  ; Receive Data Register Full


        ;       SSI Transmit Slot Mask Register A

        M_SSTSA EQU $FFFF            ; SSI Transmit Slot Bits Mask A (TS0-TS15)


        ;       SSI Transmit Slot Mask Register B
```

**Preliminary Data**

```
M_SSTSB EQU $FFFF              ; SSI Transmit Slot Bits Mask B (TS16-TS31)

;         SSI Receive Slot Mask Register A

M_SSRSA EQU $FFFF              ; SSI Receive Slot Bits Mask A (RS0-RS15)

;         SSI Receive Slot Mask Register B

M_SSRSB EQU $FFFF              ; SSI Receive Slot Bits Mask B (RS16-RS31)




;-----------------------------------------------------------------
;
;         EQUATES for Exception Processing
;
;-----------------------------------------------------------------


;         Register Addresses

M_IPRC EQU $FFFFFF             ; Interrupt Priority Register Core
M_IPRP EQU $FFFFFE             ; Interrupt Priority Register Peripheral

;         Interrupt Priority Register Core (IPRC)

M_IAL EQU $7                   ; IRQA Mode Mask
M_IAL0 EQU 0                   ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1                   ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2                   ; IRQA Mode Trigger Mode
M_IBL EQU $38                  ; IRQB Mode Mask
M_IBL0 EQU 3                   ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4                   ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5                   ; IRQB Mode Trigger Mode
M_ICL EQU $1C0                 ; IRQC Mode Mask
M_ICL0 EQU 6                   ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7                   ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8                   ; IRQC Mode Trigger Mode
M_IDL EQU $E00                 ; IRQD Mode Mask
M_IDL0 EQU 9                   ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10                  ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11                  ; IRQD Mode Trigger Mode
M_D0L EQU $3000                ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12                  ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13                  ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000                ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14                  ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15                  ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000               ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16                  ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17                  ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000               ; DMA3 Interrupt Priority Level Mask
```

**Preliminary Data**

```
M_D3L0 EQU 18                    ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19                    ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000                ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20                    ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21                    ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000                ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22                    ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23                    ; DMA5 Interrupt Priority Level (high)


;            Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3                     ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0                     ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1                     ; Host Interrupt Priority Level (high)
M_S0L EQU $C                     ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2                     ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3                     ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30                    ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4                     ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5                     ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0                    ; SCI  Interrupt Priority Level Mask
M_SCL0 EQU 6                     ; SCI  Interrupt Priority Level (low)
M_SCL1 EQU 7                     ; SCI  Interrupt Priority Level (high)
M_T0L EQU $300                   ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8                     ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9                     ; TIMER Interrupt Priority Level (high)


;--------------------------------------------------------------------
;
;          EQUATES for TIMER
;
;--------------------------------------------------------------------


;          Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F              ; Timer 0 Control/Status Register
M_TLR0 EQU  $FFFF8E              ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D              ; TIMER0 Compare Register
M_TCR0 EQU  $FFFF8C              ; TIMER0 Count Register

;          Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B              ; TIMER1 Control/Status Register
M_TLR1 EQU  $FFFF8A              ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89             ; TIMER1 Compare Register
M_TCR1 EQU  $FFFF88              ; TIMER1 Count Register


;          Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87              ; TIMER2 Control/Status Register
```

**Preliminary Data**

```
M_TLR2 EQU  $FFFF86                          ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85 ; TIMER2 Compare Register
M_TCR2 EQU  $FFFF84                          ; TIMER2 Count Register
M_TPLR EQU  $FFFF83                          ; TIMER Prescaler Load Register
M_TPCR EQU  $FFFF82                          ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0              ; Timer Enable
M_TOIE EQU 1           ; Timer Overflow Interrupt Enable
M_TCIE EQU 2           ; Timer Compare Interrupt Enable
M_TC EQU $F0           ; Timer Control Mask (TC0-TC3)
M_INV EQU 8            ; Inverter Bit
M_TRM EQU 9            ; Timer Restart Mode
M_DIR EQU 11           ; Direction Bit
M_DI EQU 12            ; Data Input
M_DO EQU 13            ; Data Output
M_PCE EQU  15          ; Prescaled Clock Enable
M_TOF EQU 20           ; Timer Overflow Flag
M_TCF EQU 21           ; Timer Compare Flag


;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000  ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22


;         Timer Control Bits
M_TC0 EQU 4            ; Timer Control 0
M_TC1 EQU 5            ; Timer Control 1
M_TC2 EQU 6            ; Timer Control 2
M_TC3 EQU 7            ; Timer Control 3


;-------------------------------------------------------------------
;
;      EQUATES for Direct Memory Access (DMA)
;
;-------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                         ; DMA Status Register
M_DOR0 EQU $FFFFF3 ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2 ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1 ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0 ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE ; DMA0 Destination Address Register
```

**Preliminary Data**

```
M_DCO0 EQU $FFFFED ; DMA0 Counter
M_DCR0 EQU $FFFFEC ; DMA0 Control Register

;          Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9 ; DMA1 Counter
M_DCR1 EQU $FFFFE8 ; DMA1 Control Register

;          Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7 ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6 ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5 ; DMA2 Counter
M_DCR2 EQU $FFFFE4 ; DMA2 Control Register

;          Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3 ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2 ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1 ; DMA3 Counter
M_DCR3 EQU $FFFFE0 ; DMA3 Control Register

;          Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD ; DMA4 Counter
M_DCR4 EQU $FFFFDC ; DMA4 Control Register

;          Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9 ; DMA5 Counter
M_DCR5 EQU $FFFFD8 ; DMA5 Control Register

;          DMA Control Register

M_DSS EQU $3        ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0        ; DMA Source Memory space 0
M_DSS1 EQU 1        ; DMA Source Memory space 1
M_DDS EQU $C        ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2        ; DMA Destination Memory Space 0
M_DDS1 EQU 3        ; DMA Destination Memory Space 1
M_DAM EQU $3f0      ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4       ; DMA Address Mode 0
M_DAM1  EQU 5       ; DMA Address Mode 1
M_DAM2  EQU 6       ; DMA Address Mode 2
M_DAM3  EQU 7       ; DMA Address Mode 3
M_DAM4  EQU 8       ; DMA Address Mode 4
```

**Preliminary Data**

```
M_DAM5   EQU 9            ; DMA Address Mode 5
M_D3D EQU 10             ; DMA Three Dimensional Mode
M_DRS EQU $F800          ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16            ; DMA Continuous Mode
M_DPR EQU $60000         ; DMA Channel Priority
M_DPR0 EQU 17            ; DMA Channel Priority Level (low)
M_DPR1 EQU 18            ; DMA Channel Priority Level (high)
M_DTM EQU $380000        ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19            ; DMA Transfer Mode 0
M_DTM1 EQU 20            ; DMA Transfer Mode 1
M_DTM2 EQU 21            ; DMA Transfer Mode 2
M_DIE EQU 22             ; DMA Interrupt Enable bit
M_DE EQU 23              ; DMA Channel Enable bit

;          DMA Status Register

M_DTD EQU $3F            ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0             ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1             ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2             ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3             ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4             ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5             ; DMA Channel Transfer Done Status 5
M_DACT EQU  8            ; DMA Active State
M_DCH EQU  $E00          ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9            ; DMA Active Channel 0
M_DCH1 EQU  10           ; DMA Active Channel 1
M_DCH2 EQU  11           ; DMA Active Channel 2


;-----------------------------------------------------------------------
;
;          EQUATES for Phase Locked Loop (PLL)
;
;-----------------------------------------------------------------------

;          Register Addresses Of PLL

M_PCTL EQU $FFFFFD            ; PLL Control Register

;          PLL Control Register

M_MF EQU $FFF            : Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000           ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15            ; XTAL Range select bit
M_XTLD EQU 16            ; XTAL Disable Bit
M_PSTP EQU 17            ; STOP Processing State Bit
M_PEN EQU 18             ; PLL Enable Bit
M_PCOD EQU 19            ; PLL Clock Output Disable Bit
M_PD EQU $F00000         ; PreDivider Factor Bits Mask (PD0-PD3)
```

**Preliminary Data**

```
;------------------------------------------------------------------
;
;          EQUATES for BIU
;
;------------------------------------------------------------------

;          Register Addresses Of BIU


M_BCR EQU $FFFFFB  ; Bus Control Register
M_DCR EQU $FFFFFA  ; DRAM Control Register
M_AAR0 EQU $FFFFF9 ; Address Attribute Register 0
M_AAR1 EQU $FFFFF8 ; Address Attribute Register 1
M_AAR2 EQU $FFFFF7 ; Address Attribute Register 2
M_AAR3 EQU $FFFFF6 ; Address Attribute Register 3
M_IDR EQU  $FFFFF5 ; ID Register


;          Bus Control Register

M_BA0W EQU $1F      ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0     ; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00    ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000    ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000  ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21        ; Bus State
M_BLH EQU 22        ; Bus Lock Hold
M_BRH EQU 23        ; Bus Request Hold


;          DRAM Control Register

M_BCW EQU $3        ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C        ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300      ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11       ; Page Logic Enable
M_BME EQU 12        ; Mastership Enable
M_BRE EQU 13        ; Refresh Enable
M_BSTR EQU 14       ; Software Triggered Refresh
M_BRF EQU $7F8000   ; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23        ; Refresh prescaler


;          Address Attribute Registers

M_BAT EQU $3        ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2        ; Address Attribute Pin Polarity
M_BPEN EQU 3        ; Program Space Enable
M_BXEN EQU 4        ; X Data Space Enable
M_BYEN EQU 5        ; Y Data Space Enable
M_BAM EQU 6         ; Address Muxing
M_BPAC EQU 7        ; Packing Enable
M_BNC EQU $F00      ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000   ; Address to Compare Bits Mask (BAC0-BAC11)
```

**Preliminary Data**

```
;          control and status bits in SR

M_CP EQU $c00000      ; mask for CORE-DMA priority bits in SR
M_CA EQU 0            ; Carry
M_V  EQU 1            ; Overflow
M_Z  EQU 2            ; Zero
M_N  EQU 3            ; Negative
M_U  EQU 4            ; Unnormalized
M_E  EQU 5            ; Extension
M_L  EQU 6            ; Limit
M_S  EQU 7            ; Scaling Bit
M_I0 EQU 8            ; Interupt Mask Bit 0
M_I1 EQU 9            ; Interupt Mask Bit 1
M_S0 EQU 10           ; Scaling Mode Bit 0
M_S1 EQU 11           ; Scaling Mode Bit 1
M_SC EQU 13           ; Sixteen_Bit Compatibility
M_DM EQU 14           ; Double Precision Multiply
M_LF EQU 15           ; DO-Loop Flag
M_FV EQU 16           ; DO-Forever Flag
M_SA EQU 17           ; Sixteen-Bit Arithmetic
M_CE EQU 19           ; Instruction Cache Enable
M_SM EQU 20           ; Arithmetic Saturation
M_RM EQU 21           ; Rounding Mode
M_CP0 EQU 22          ; bit 0 of priority bits in SR
M_CP1 EQU 23          ; bit 1 of priority bits in SR

;          control and status bits in OMR
M_CDP EQU $300        ; mask for CORE-DMA priority bits in OMR
M_MA    equ0          ; Operating Mode A
M_MB    equ1          ; Operating Mode B
M_MC    equ2          ; Operating Mode C
M_MD    equ3          ; Operating Mode D
M_EBD EQU 4           ; External Bus Disable bit in OMR
M_SD EQU 6            ; Stop Delay
M_MS EQU 7            ; Memory Switch bit in OMR
M_CDP0 EQU 8          ; bit 0 of priority bits in OMR
M_CDP1 EQU 9          ; bit 1 of priority bits in OMR
M_BEN    EQU 10       ; Burst Enable
M_TAS    EQU 11       ; TA Synchronize Select
M_BRT    EQU 12       ; Bus Release Timing
M_ATE EQU 15          ; Address Tracing Enable bit in OMR.
M_XYS EQU 16          ; Stack Extension space select bit in OMR.
M_EUN EQU 17          ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18          ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19          ; Extended WRaP flag in OMR.
M_SEN EQU 20          ; Stack Extension Enable bit in OMR.
```

**Preliminary Data**

```
;**************************************************************************
;
;       EQUATES for DSP56304 interrupts
;
;       Last update: June 11 1995
;
;**************************************************************************

          page      132,55,0,0,0
          opt       mex

intequ  ident   1,0

          if        @DEF(I_VEC)
          ;leave user definition as is.
          else
I_VEC EQU $0
          endif

;--------------------------------------------------------------------------
; Non-Maskable interrupts
;--------------------------------------------------------------------------
I_RESET EQU I_VEC+$00        ; Hardware RESET
I_STACK EQU I_VEC+$02        ; Stack Error
I_ILL EQU I_VEC+$04          ; Illegal Instruction
I_DBG EQU I_VEC+$06          ; Debug Request
I_TRAP EQU I_VEC+$08         ; Trap
I_NMI EQU I_VEC+$0A          ; Non Maskable Interrupt

;--------------------------------------------------------------------------
; Interrupt Request Pins
;--------------------------------------------------------------------------
I_IRQA EQU I_VEC+$10         ; IRQA
I_IRQB EQU I_VEC+$12         ; IRQB
I_IRQC EQU I_VEC+$14         ; IRQC
I_IRQD EQU I_VEC+$16         ; IRQD

;--------------------------------------------------------------------------
; DMA Interrupts
;--------------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18         ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A         ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C         ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E         ; DMA Channel 3
I_DMA4 EQU I_VEC+$20         ; DMA Channel 4
I_DMA5 EQU I_VEC+$22         ; DMA Channel 5

;--------------------------------------------------------------------------
; Timer Interrupts
;--------------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24        ; TIMER 0 compare
```

**Preliminary Data**

```
I_TIM0OF EQU I_VEC+$26        ; TIMER 0 overflow
I_TIM1C  EQU I_VEC+$28        ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A        ; TIMER 1 overflow
I_TIM2C  EQU I_VEC+$2C        ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E        ; TIMER 2 overflow


;----------------------------------------------------------------
; ESSI Interrupts
;----------------------------------------------------------------
I_SI0RD  EQU I_VEC+$30        ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32        ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34        ; ESSI0 Receive last slot
I_SI0TD  EQU I_VEC+$36        ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38        ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A        ; ESSI0 Transmit last slot
I_SI1RD  EQU I_VEC+$40        ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42        ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44        ; ESSI1 Receive last slot
I_SI1TD  EQU I_VEC+$46        ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48        ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A        ; ESSI1 Transmit last slot


;----------------------------------------------------------------
; SCI Interrupts
;----------------------------------------------------------------
I_SCIRD  EQU I_VEC+$50        ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52        ; SCI Receive Data With Exception Status
I_SCITD  EQU I_VEC+$54        ; SCI Transmit Data
I_SCIIL  EQU I_VEC+$56        ; SCI Idle Line
I_SCITM  EQU I_VEC+$58        ; SCI Timer


;----------------------------------------------------------------
; HOST Interrupts
;----------------------------------------------------------------
I_HRDF EQU I_VEC+$60          ; Host Receive Data Full
I_HTDE EQU I_VEC+$62          ; Host Transmit Data Empty
I_HC   EQU I_VEC+$64          ; Default Host Command


;----------------------------------------------------------------
; INTERRUPT ENDING ADDRESS
;----------------------------------------------------------------
I_INTEND EQU I_VEC+$FF        ; last address of interrupt vector space
```

**Preliminary Data**

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