IS62LV256

32K x 8 LOW VOLTAGE STATIC RAM

JULY 1997

FEATURES

- Access time: 45, 70, 100 ns
- Low active power: 70 mW
- Low standby power
  — 45 µW CMOS standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply

DESCRIPTION

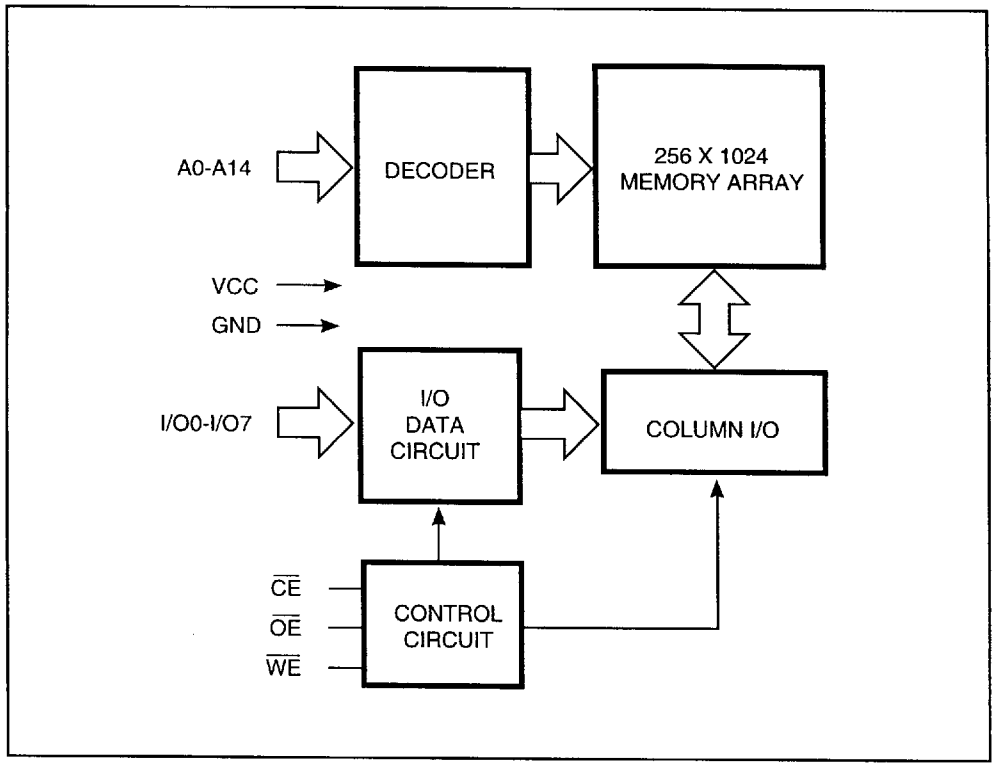
The *ISSI* IS62LV256 is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS double-metal technology.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 10 µW (typical) with CMOS input levels.

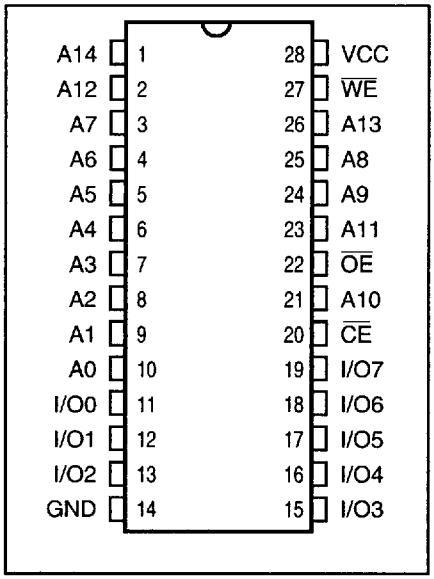
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62LV256 is pin compatible with other 32K x 8 SRAMs in 300-mil plastic DIP and SOJ, 330-mil plastic SOP, and TSOP (Type I) packages.

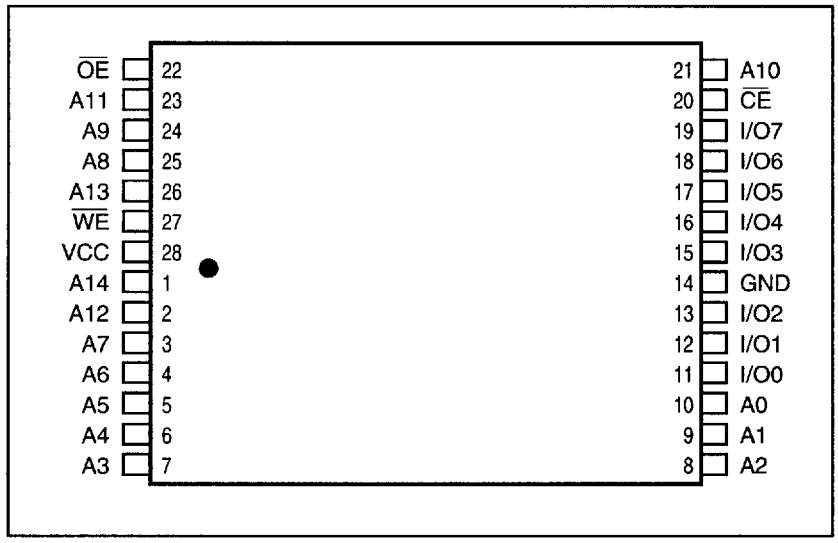
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin DIP, SOJ and SOP



PIN CONFIGURATION
28-Pin TSOP (Type I)



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com.	–2	2	µA
			Ind.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com.	–2	2	µA
			Ind.	–5	5	

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	-100 ns Min.	-100 ns Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = 0	Com.	—	20	—	20	—	20	mA
			Ind.	—	30	—	30	—	30	
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	35	—	30	—	30	mA
			Ind.	—	45	—	40	—	40	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f = 0	Com.	—	2	—	2	—	2	mA
			Ind.	—	5	—	5	—	5	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	90	—	90	—	90	µA
			Ind.	—	200	—	200	—	200	

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc =3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	-100 ns Min.	-100 ns Max.	Unit
t_{RC}	Read Cycle Time	45	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	45	—	70	—	100	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	45	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	—	50	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	20	0	25	0	25	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	20	0	25	0	25	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	30	—	50	—	50	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

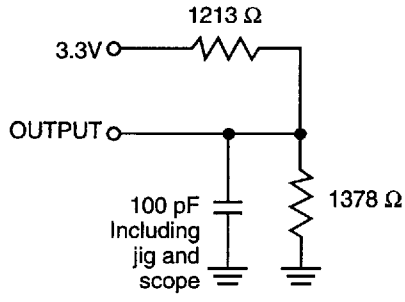


Figure 1a.

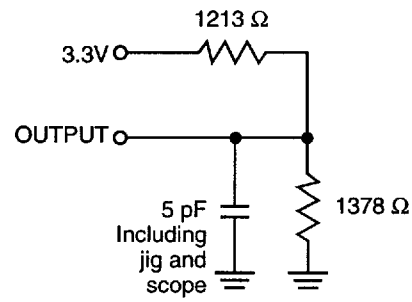
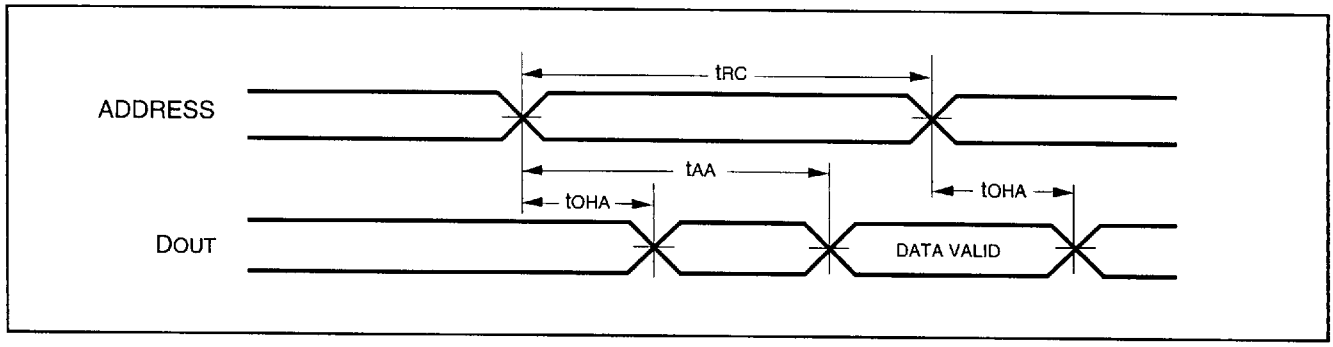


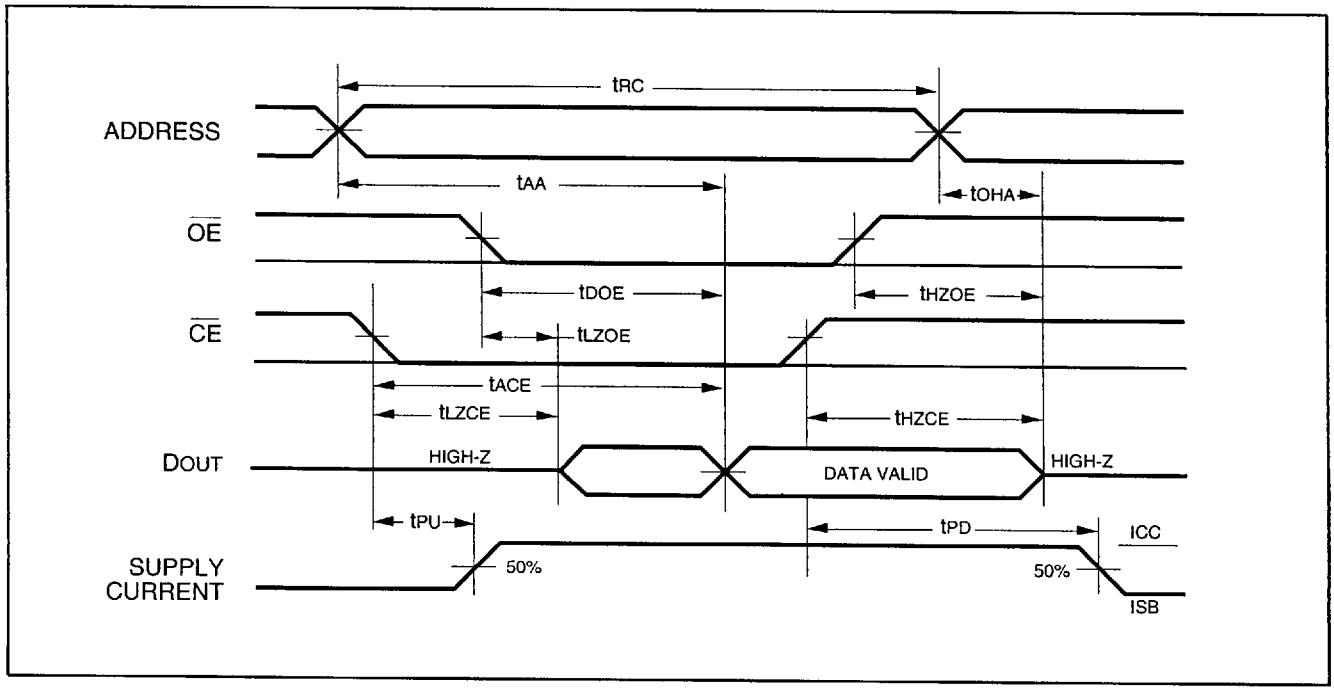
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

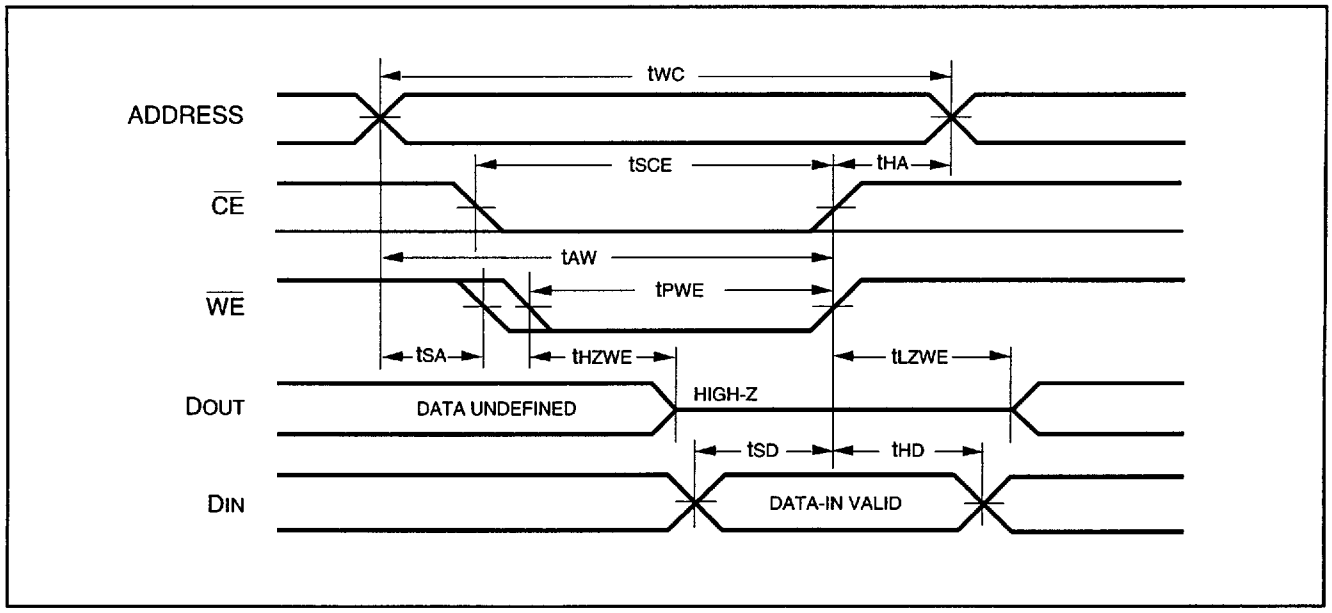
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2,3] (Over Operating Range)

Symbol	Parameter	-45 ns Min.	-45 ns Max.	-70 ns Min.	-70 ns Max.	-100 ns Min.	-100 ns Max.	Unit
t_{WC}	Write Cycle Time	45	—	70	—	100	—	ns
t_{SCE}	$\overline{CE}$ to Write End	35	—	60	—	80	—	ns
t_{AW}	Address Setup Time to Write End	25	—	60	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	25	—	55	—	60	—	ns
t_{SD}	Data Setup to Write End	20	—	30	—	35	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns

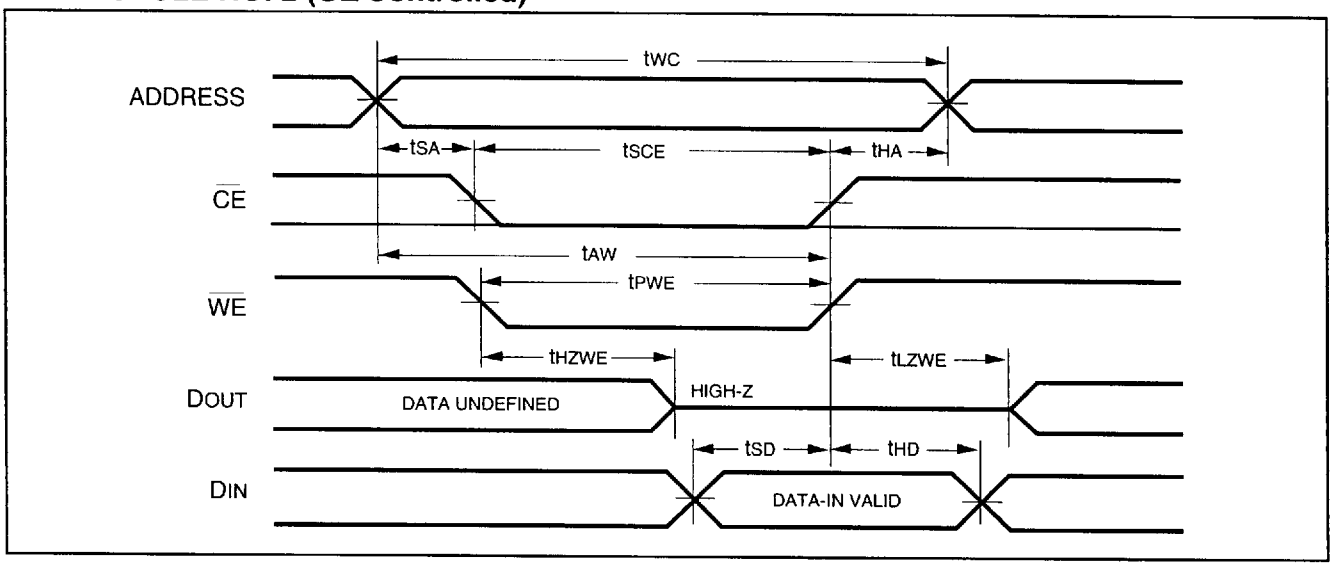
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]



Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

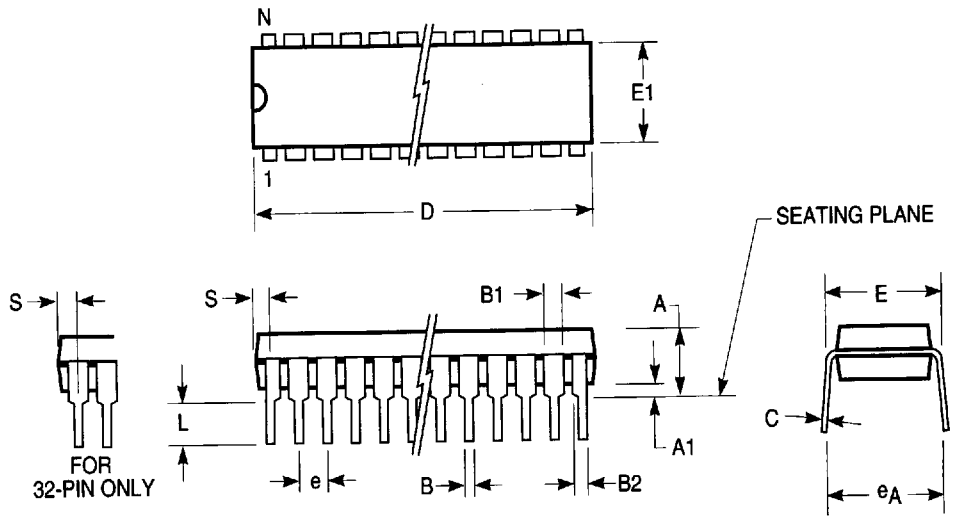
Speed (ns)	Order Part No.	Package
45	IS62LV256-45N	300-mil Plastic DIP
45	IS62LV256-45J	300-mil Plastic SOJ
45	IS62LV256-45T	TSOP (Type I)
45	IS62LV256-45U	330-mil SOP
70	IS62LV256-70N	300-mil Plastic DIP
70	IS62LV256-70J	300-mil Plastic SOJ
70	IS62LV256-70T	TSOP (Type I)
70	IS62LV256-70U	330-mil SOP
100	IS62LV256-100N	300-mil Plastic DIP
100	IS62LV256-100J	300-mil Plastic SOJ
100	IS62LV256-100T	TSOP (Type I)
100	IS62LV256-100U	330-mil SOP

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV256-45JI	300-mil Plastic SOJ
45	IS62LV256-45TI	TSOP (Type I)
45	IS62LV256-45UI	330-mil SOP
70	IS62LV256-70JI	300-mil Plastic SOJ
70	IS62LV256-70TI	TSOP (Type I)
70	IS62LV256-70UI	330-mil SOP
100	IS62LV256-100JI	300-mil Plastic SOJ
100	IS62LV256-100TI	TSOP (Type I)
100	IS62LV256-100UI	330-mil SOP

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Tel: 1-800-379-4774
Fax: (408) 588-0806
e-mail: sales@issiusa.com
http://www.issiusa.com

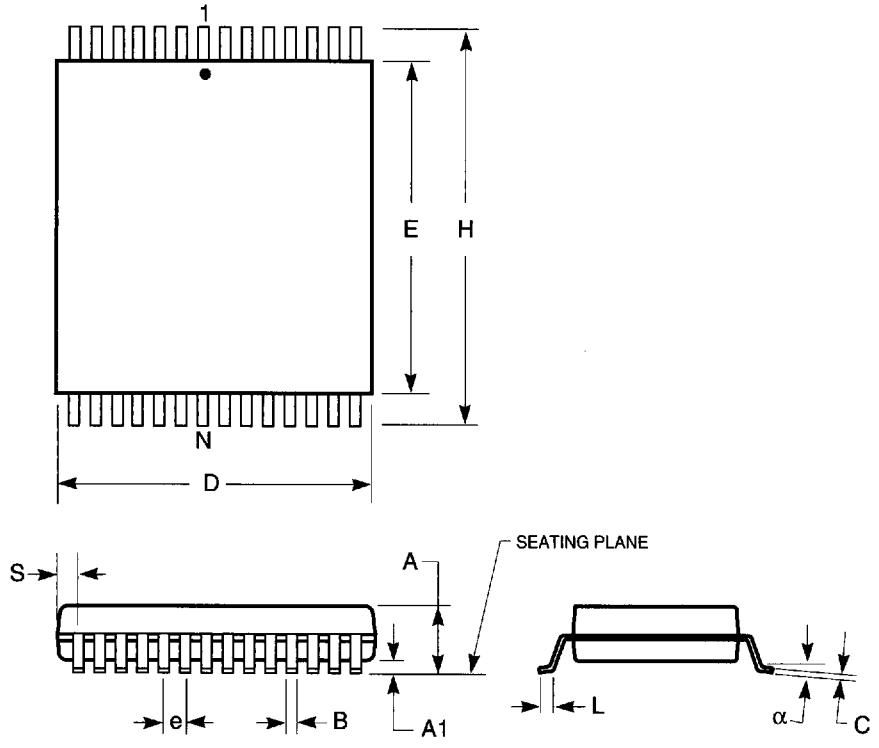
300-mil Plastic DIP
Package Code: N, P



300-mil Plastic DIP (N, P)								
	Inches							
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
N	8		16		28		32	
A	0.145	0.180	0.125	0.130	0.145	0.180	0.140	0.180
A1	0.015	—	0.010	—	0.010	0.035	0.015	0.035
B	0.014	0.022	0.018 BSC		0.016	0.022	0.015	0.021
B1	0.045	0.060	0.060 BSC		0.050	0.070	0.040	0.070
B2	0.032	0.046	—	—	0.032	0.046	—	—
C	0.008	0.013	0.005	0.015	0.008	0.015	0.005	0.015
D	0.359	0.375	0.745	0.755	1.380	1.400	1.595	1.605
E	0.300	0.325	0.293	0.320	0.295	0.315	0.305	0.325
E1	0.244	0.260	0.245	0.255	0.275	0.295	0.285	0.292
e_A	0.320	0.380	0.320	0.380	0.310	0.400	0.330	0.370
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
L	0.125	—	0.120	0.140	0.120	0.150	0.120	0.150
S	0.025	0.030	0.015	0.035	0.020	0.042	0.065	0.085

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

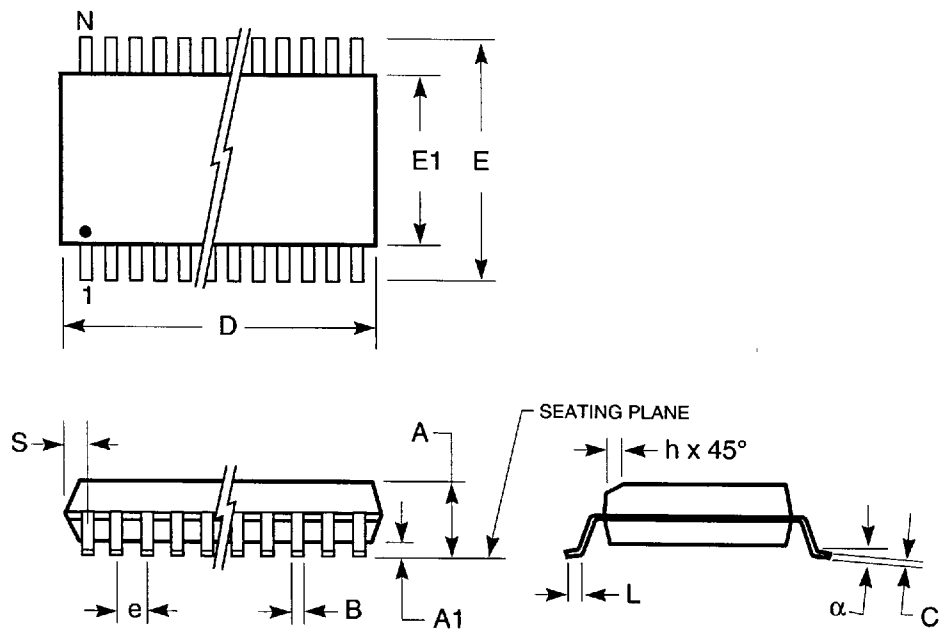
Plastic TSOP - 28-pins
Package Code: T



Plastic TSOP (T)		
	Inches	
Symbol	Min	Max
Ref. Std.		
N	28	
A	0.037	0.047
A1	0.002	0.008
B	0.006	0.011
C	0.004	0.008
D	0.311	0.319
E	0.460	0.468
H	0.520	0.536
e	0.020 BSC	
L	0.011	0.027
α	0°	5°

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

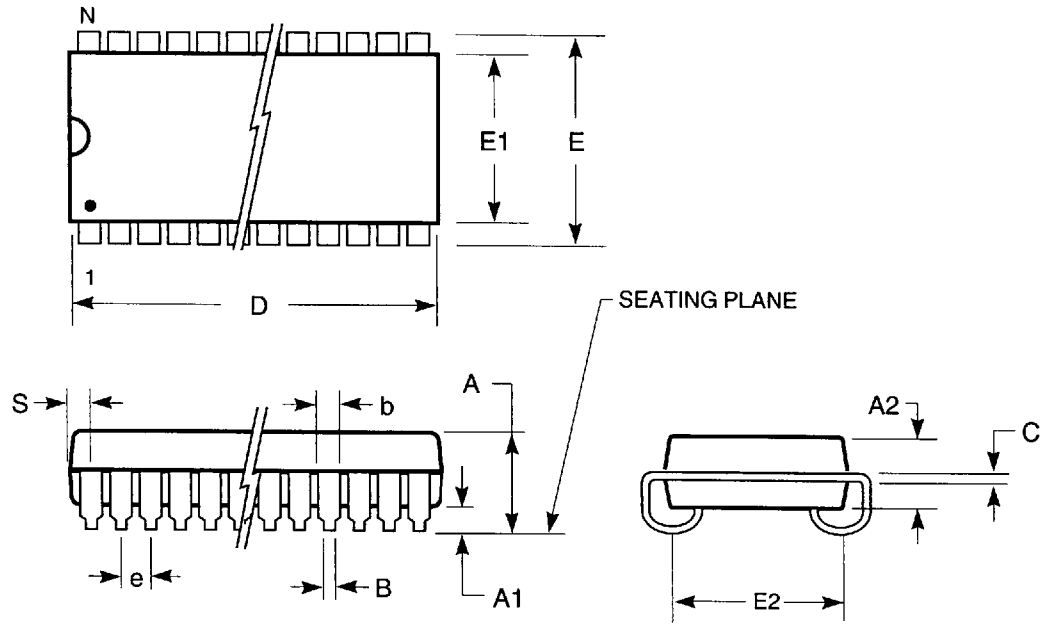
330-mil Plastic SOP
Package Code: U



330-mil Plastic SOP (U)		
	Inches	
Symbol	Min	Max
Ref. Std.		
No. Leads	28	
A	—	0.112
A1	0.004	—
B	0.014	0.020
C	0.010	—
D	0.708	0.718
E	0.453	0.477
E1	0.326	0.336
e	0.050 BSC	
h	0.012	0.020
L	0.028	0.045
α	0°	8°
S	0.023	0.047

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

300-mil Plastic SOJ
Package Code: J



300-mil Plastic SOJ (J-bend) (J)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	28		32	
A	—	0.140	—	0.140
A1	0.020	—	0.020	—
A2	0.095	0.105	0.095	0.105
B	0.016	0.022	0.016	0.022
b	0.026	0.032	0.026	0.032
C	0.008	0.014	0.008	0.014
D	0.710	0.730	0.815	0.835
E	0.327	0.347	0.325	0.345
E1	0.295	0.305	0.295	0.305
E2	0.245	0.285	0.247	0.287
e	0.050 BSC		0.050 BSC	
S	—	0.045	0.023	0.035

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.