

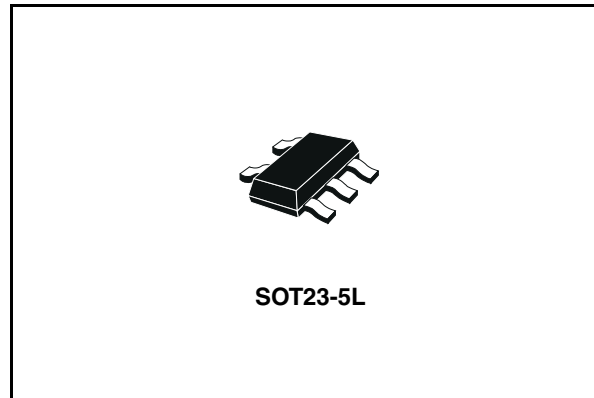
Low noise low drop voltage regulator with shutdown function

Features

- Output current up to 200 mA
- Low dropout voltage (500 mV max at $I_{OUT} = 200$ mA)
- Very low quiescent current: 0.1 μ A in OFF mode and max 250 μ A in ON mode at $I_{OUT} = 0$ mA
- Low output noise: typ. 30 μ V at $I_{OUT} = 60$ mA and 10 Hz $< f < 80$ kHz
- Wide range of output voltages
- Internal current and thermal limit
- V_{OUT} tolerance $\pm 2\%$ (at 25 °C)
- Operative input voltage from:
 $V_{OUT} + 0.5$ to 14 V (for $V_{OUT} > 2$ V)
 or from 2.5 V to 14 V (for $V_{OUT} < 2$ V)

Description

The LK112Sxx is a low dropout linear regulator with a built in electronic switch. The internal switch can be controlled by TTL or CMOS logic levels. The device is ON state when the control pin is pulled to a logic high level. An external capacitor can be used connected to the noise bypass pin to lower the output noise level to 30



μ Vrms. An internal PNP pass transistor is used to achieve a low dropout voltage.

The LK112Sxx has a very low quiescent current in ON MODE while in OFF MODE the I_q is reduced down to 100 nA max. The internal thermal shutdown circuitry limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shutdown in the presence of a short circuit or overcurrent condition at the output.

Table 1. Device summary

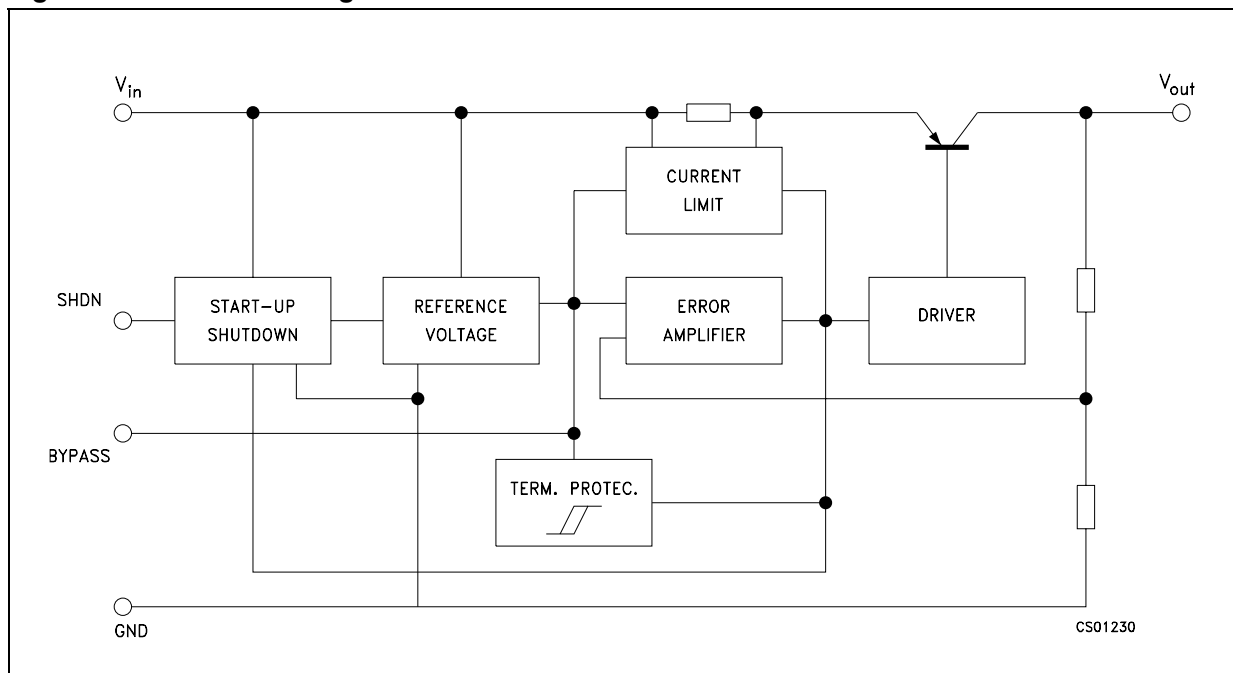
Part numbers			
LK112SXX13	LK112SXX24	LK112SXX36	LK112SXX45
LK112SXX14	LK112SXX26	LK112SXX37	LK112SXX46
LK112SXX18	LK112SXX28	LK112SXX38	LK112SXX47
LK112SXX19	LK112SXX29	LK112SXX39	LK112SXX48
LK112SXX20	LK112SXX31	LK112SXX41	LK112SXX49
LK112SXX21	LK112SXX33	LK112SXX42	LK112SXX50
LK112SXX22	LK112SXX34	LK112SXX43	
LK112SXX23	LK112SXX35	LK112SXX44	

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1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connection (top view)

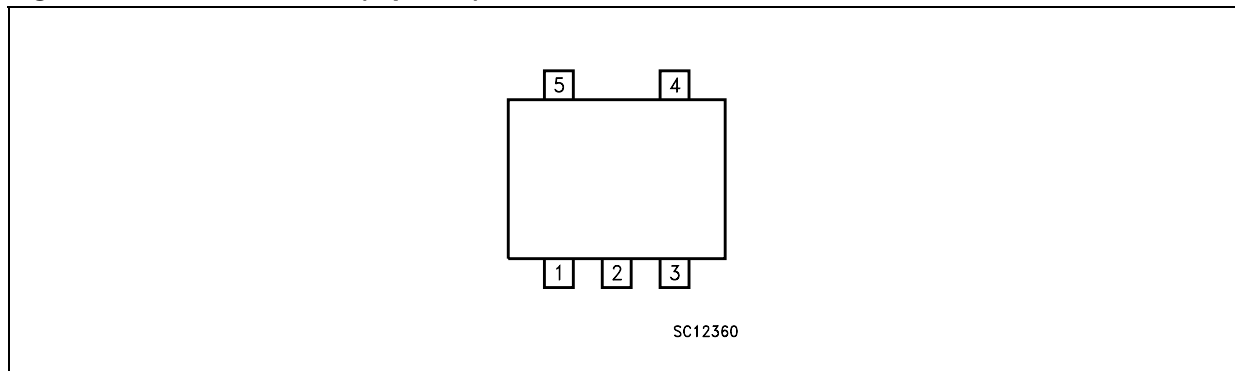


Table 2. Pin description

Pin n°	Symbol	Note
1	SHDN	Shutdown Input: Disables the regulator when is connected to GND or to positive voltage less than 0.6 V
2	GND	Ground Pin: Internally connected to the die attach flag to decrease the total thermal resistance and increase the package ability to dissipate power.
3	Bypass	Bypass Pin: Bypass with 0.1 μ F to improve the V_{REF} thermal noise performances.
4	OUT	Output port
5	IN	Input port

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	16	V
V_{SHDN}	DC input voltage	16	V
I_O	Output current	Internally limited	
T_{STG}	Storage temperature range	-55 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Table 4. Thermal data

Symbol	Parameter	SOT23-5L	Unit
R_{thJC}	Thermal resistance junction-case	81	°C/W
R_{thJA}	Thermal resistance junction-ambient	255	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics for LK112S ($T_J = 25\text{ }^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{ V}$ ⁽¹⁾, $I_{OUT} = 0\text{ mA}$, $V_{SHDN} = 1.8\text{ V}$, $C_I = 1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_d	Quiescent current	ON MODE (except I_{SHDN})		175	250	μA
		OFF MODE, $V_I = 8\text{ V}$, $V_{SHDN} = 0\text{ V}$		0	0.1	μA
V_O	Output voltage	$I_O = 30\text{ mA}$	(see table)			
ΔV_O	Line regulation	$V_I = V_O + 1\text{ V}$ to $V_O + 6\text{ V}$, $V_O \leq 5.6\text{ V}$		0.7	20	mV
		$V_I = V_O + 1\text{ V}$ to $V_O + 6\text{ V}$, $V_O > 5.6\text{ V}$		0.8	40	mV
ΔV_O	Load regulation	$I_O = 1$ to 60 mA		15	30	mV
		$I_O = 1$ to 200 mA		30	90	mV
V_d	Dropout voltage	$I_O = 60\text{ mA}$ ⁽²⁾		0.17	0.24	V
		$I_O = 200\text{ mA}$ ⁽²⁾		0.35	0.5	V
I_{SC}	Short circuit current		200			mA
SVR	Supply voltage rejection	$V_I = V_O + 1.5\text{ V}$, $C_{BYP} = 0.1\text{ }\mu\text{F}$ $C_O = 10\text{ }\mu\text{F}$, $f = 400\text{ Hz}$, $I_O = 30\text{ mA}$		55		dB
eN	Output noise voltage	$B = 10\text{ Hz}$ to 80 kHz , $C_{BYP} = 0.1\text{ }\mu\text{F}$ $C_O = 10\text{ }\mu\text{F}$, $V_I = V_O + 1.5\text{ V}$, $I_O = 60\text{ mA}$		30		μV_{rms}
I_{SHDN}	Shutdown input current	$V_{SHDN} = 1.8\text{ V}$, Output ON		12	35	μA
V_{SHDN}	Shutdown input logic	Output ON	1.8			V
		Output OFF			0.6	
$\Delta V_O/T_J$	Output voltage temperature coefficient	$I_O = 10\text{ mA}$		0.09		mV/ $^\circ\text{C}$

1. For version with output voltage less than 2V $V_{IN} = 2.4\text{ V}$
2. Only for version with output voltage more than 2.1V

5 Typical characteristics

(Unless otherwise specified, $T_J = 25\text{ }^\circ\text{C}$, $C_I = 1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$, $C_{BYP} = 100\text{ nF}$)

Figure 3. Output voltage vs temperature

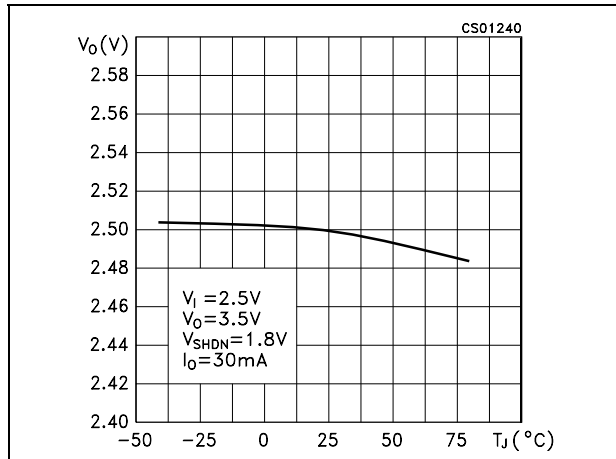


Figure 4. Output voltage vs temperature

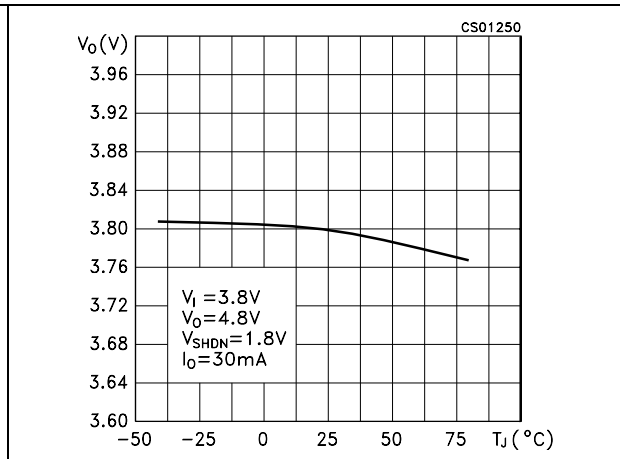


Figure 5. Line regulation vs temperature

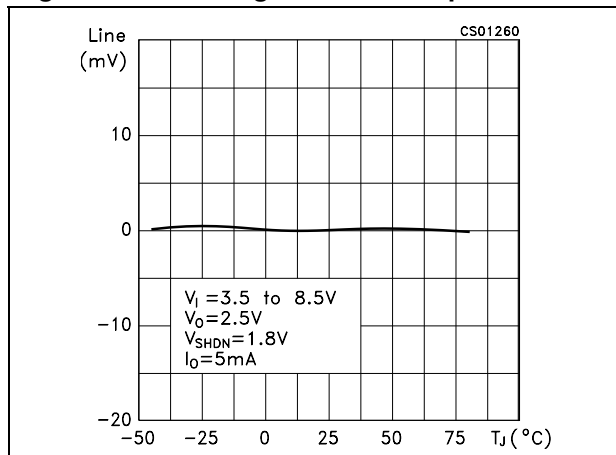


Figure 6. Load regulation vs temperature

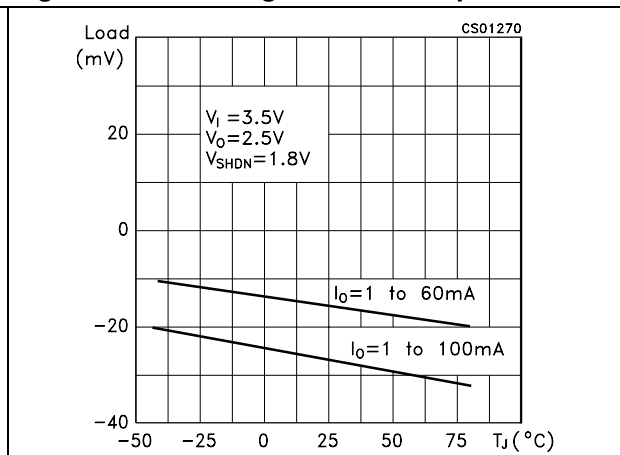


Figure 7. Dropout voltage vs temperature

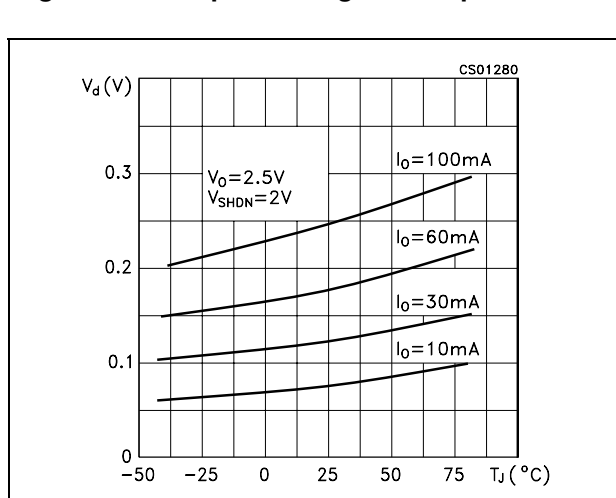


Figure 8. Short circuit current vs dropout voltage

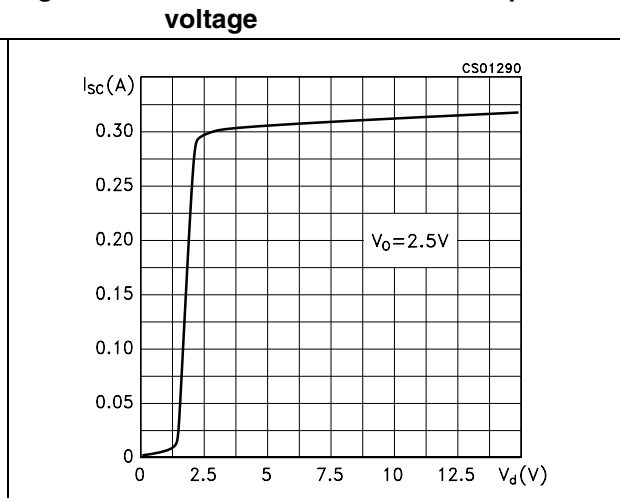


Figure 9. Output voltage vs input voltage

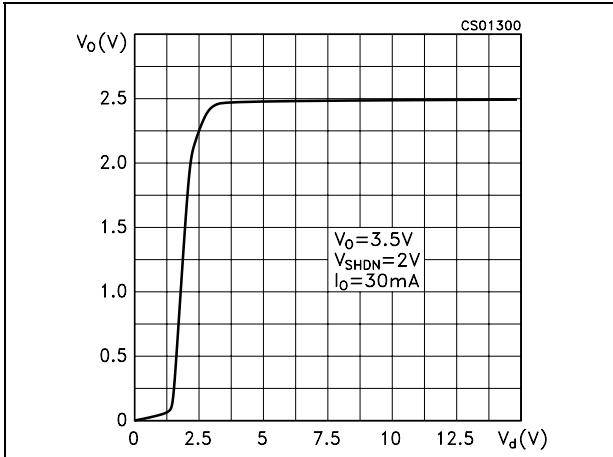


Figure 10. Shutdown voltage vs temperature

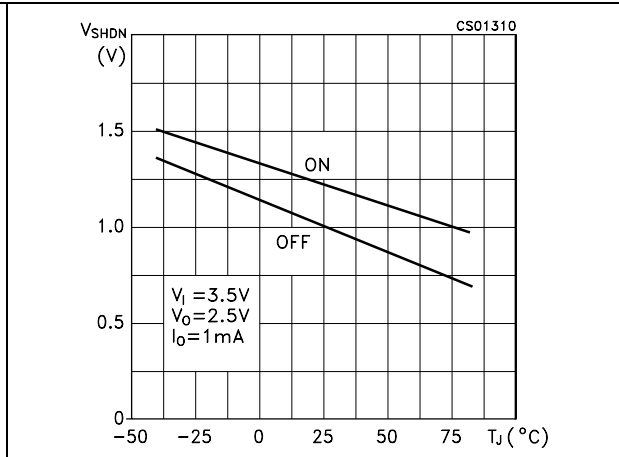


Figure 11. Shutdown current vs shutdown voltage

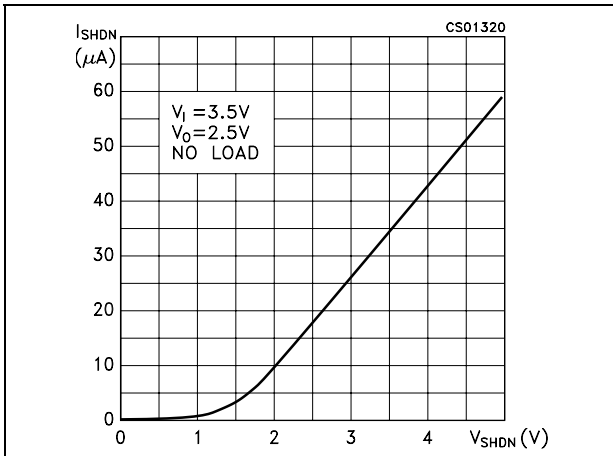


Figure 12. Supply voltage rejection vs temperature

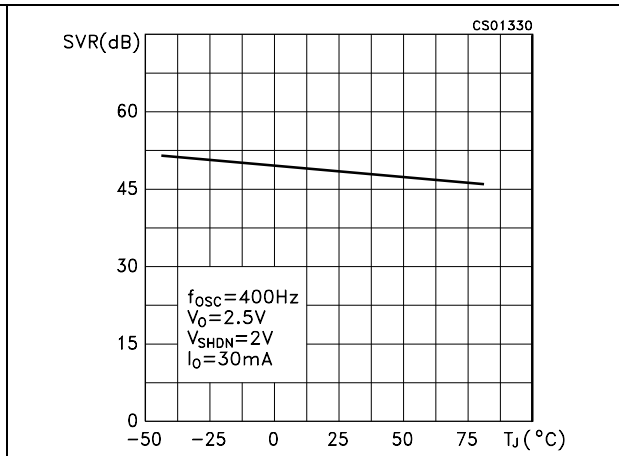


Figure 13. Supply voltage rejection vs output current

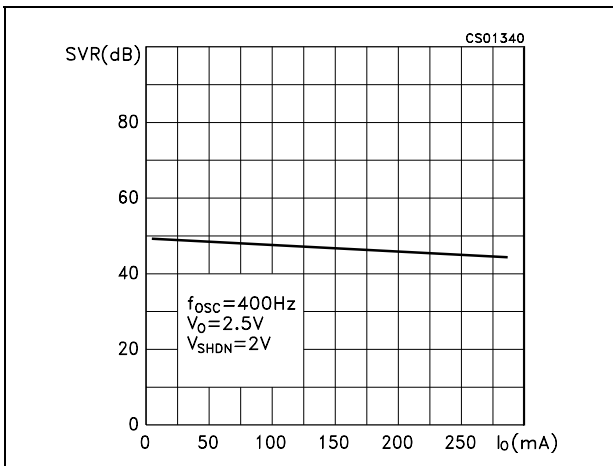


Figure 14. Supply voltage rejection vs frequency

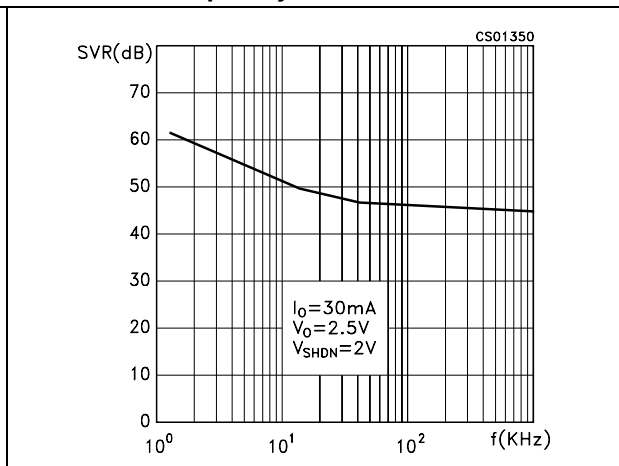


Figure 15. Supply voltage rejection vs temperature

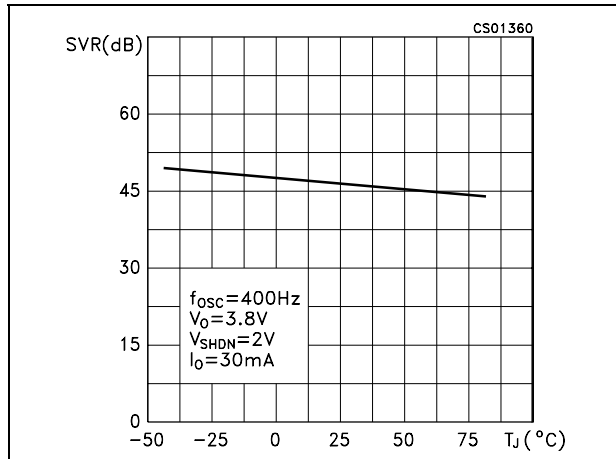


Figure 16. Quiescent current vs temperature

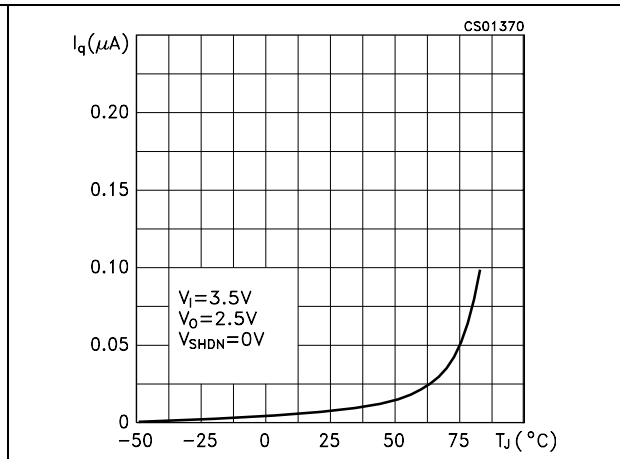


Figure 17. Quiescent current vs input voltage

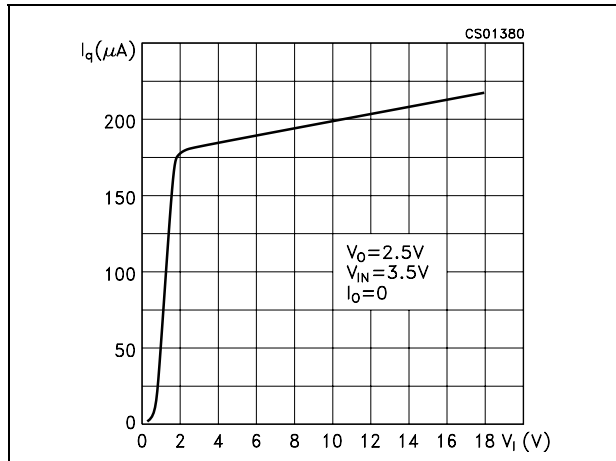


Figure 18. Quiescent current vs shutdown voltage

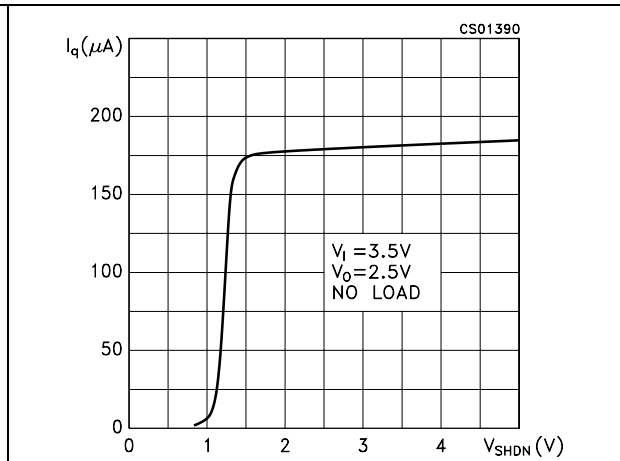


Figure 19. Quiescent current vs temperature

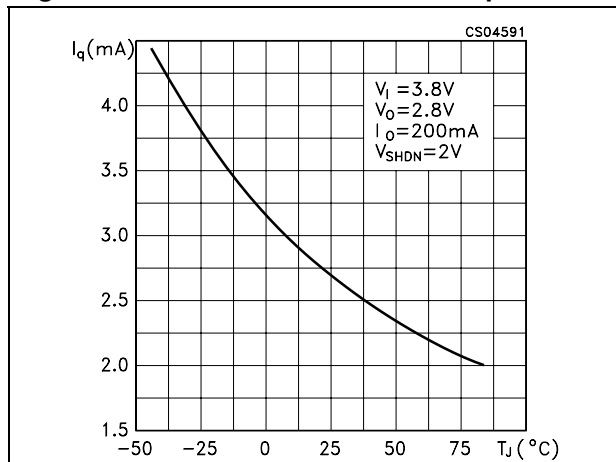


Figure 20. Reverse current vs reverse voltage

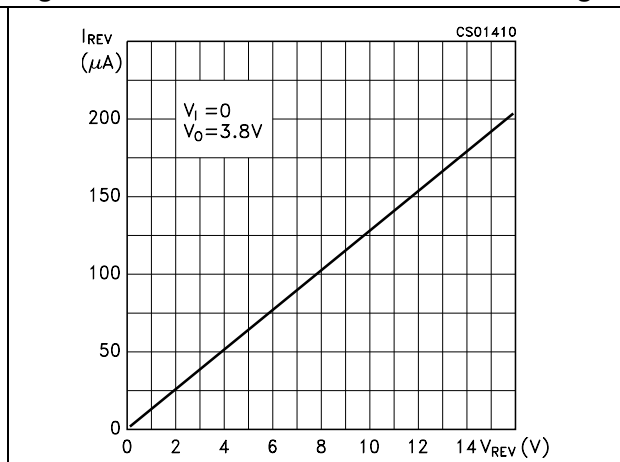


Figure 21. Stability

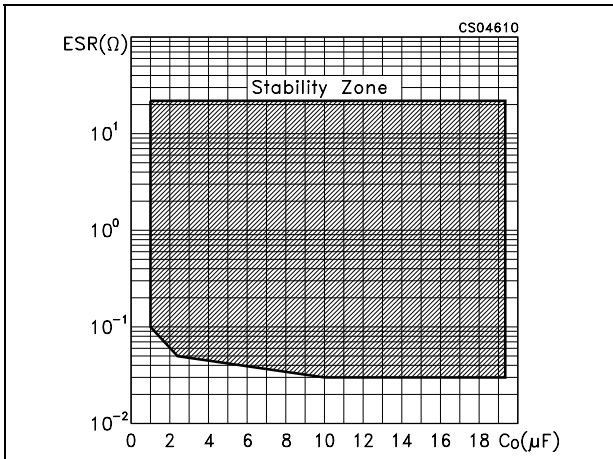


Figure 22. Spectrum noise

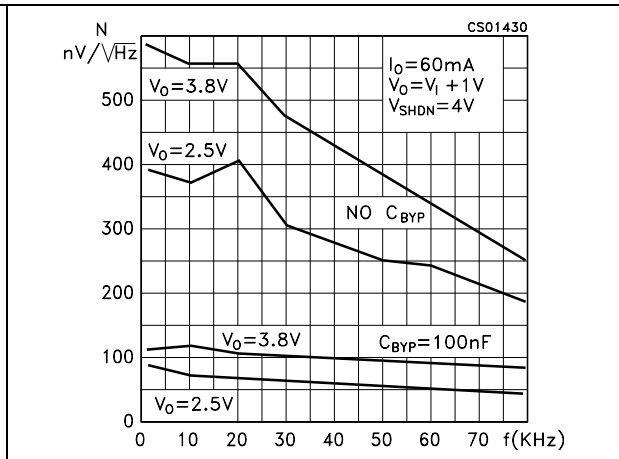


Figure 23. Start-up transient

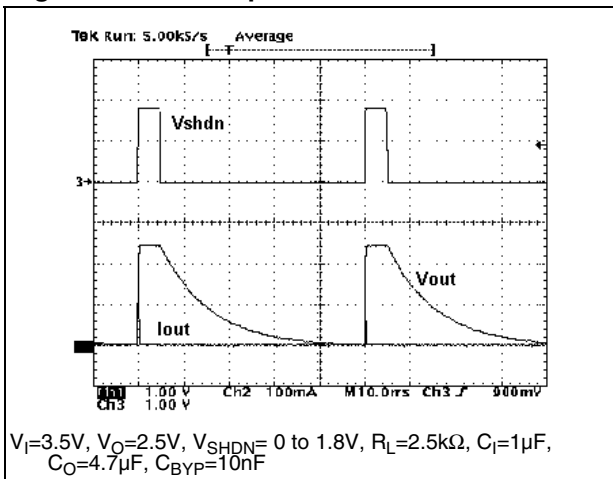


Figure 24. Start-up transient

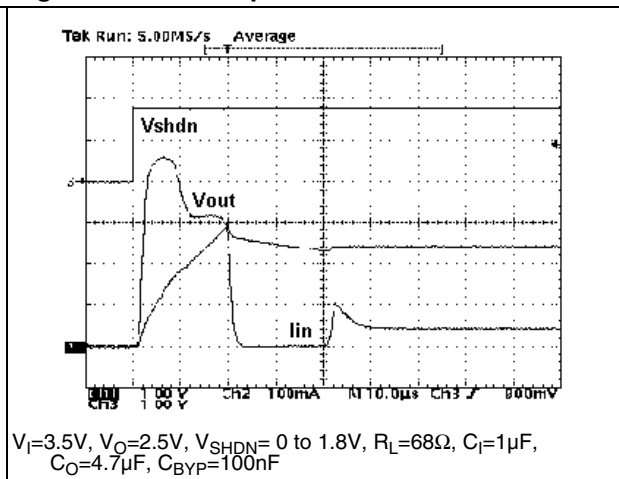


Figure 25. Line transient

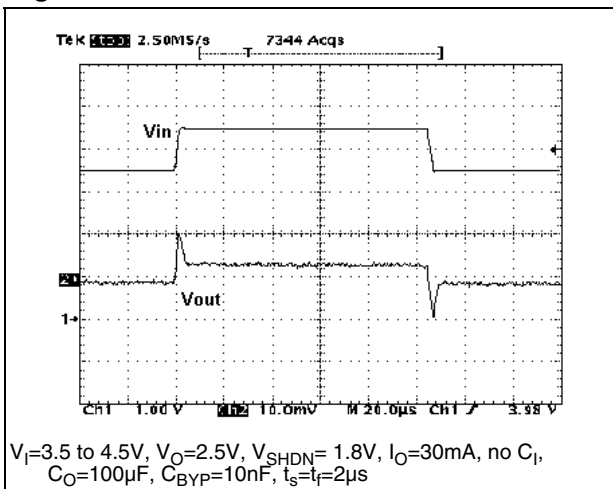


Figure 26. Line transient

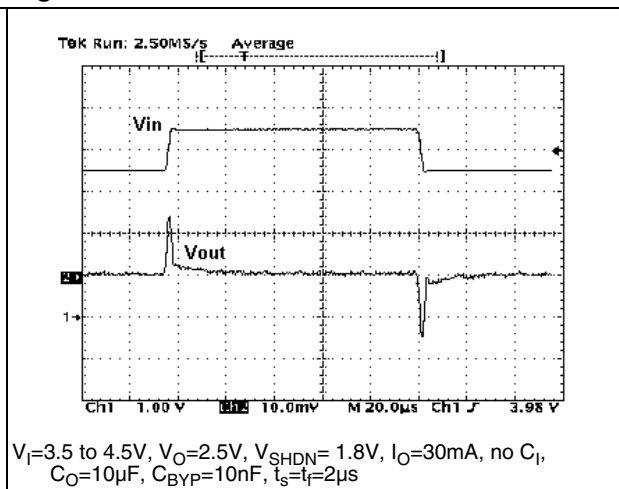


Figure 27. Line transient

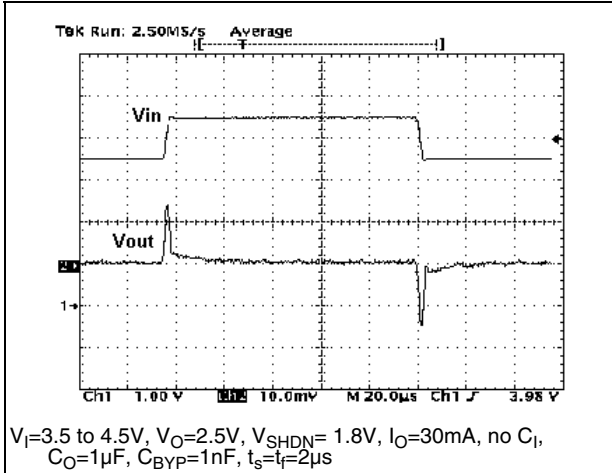


Figure 28. Load transient

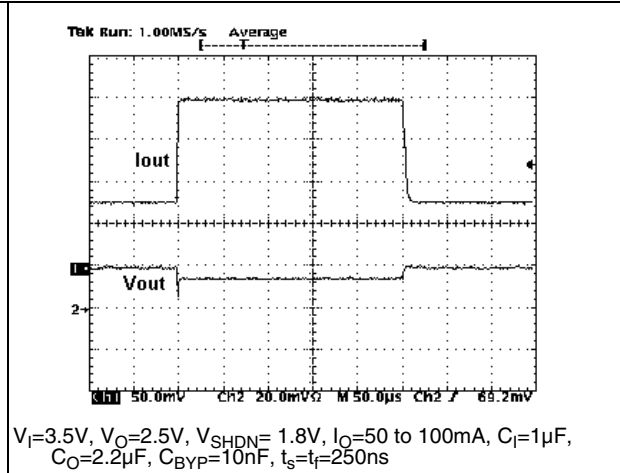


Figure 29. Load transient

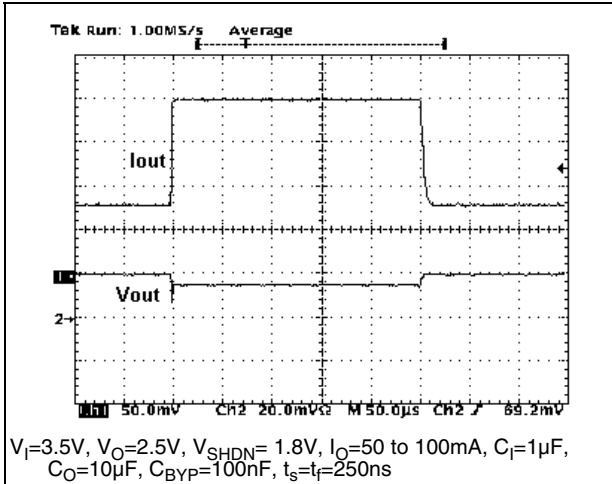
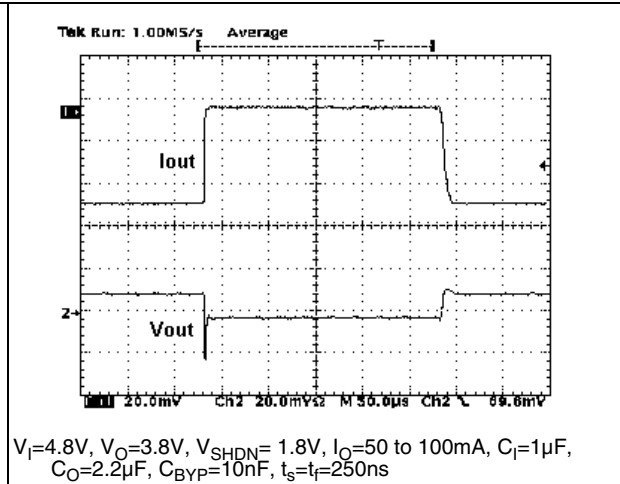


Figure 30. Load transient

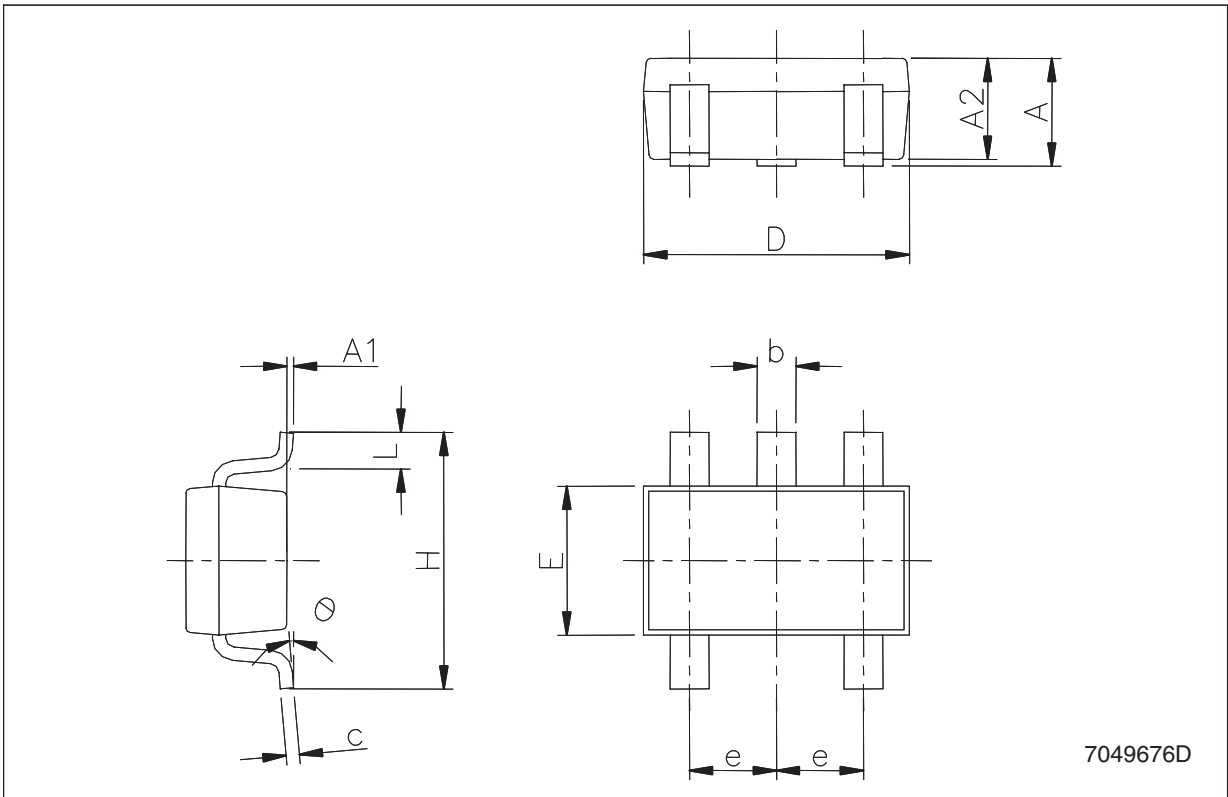


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

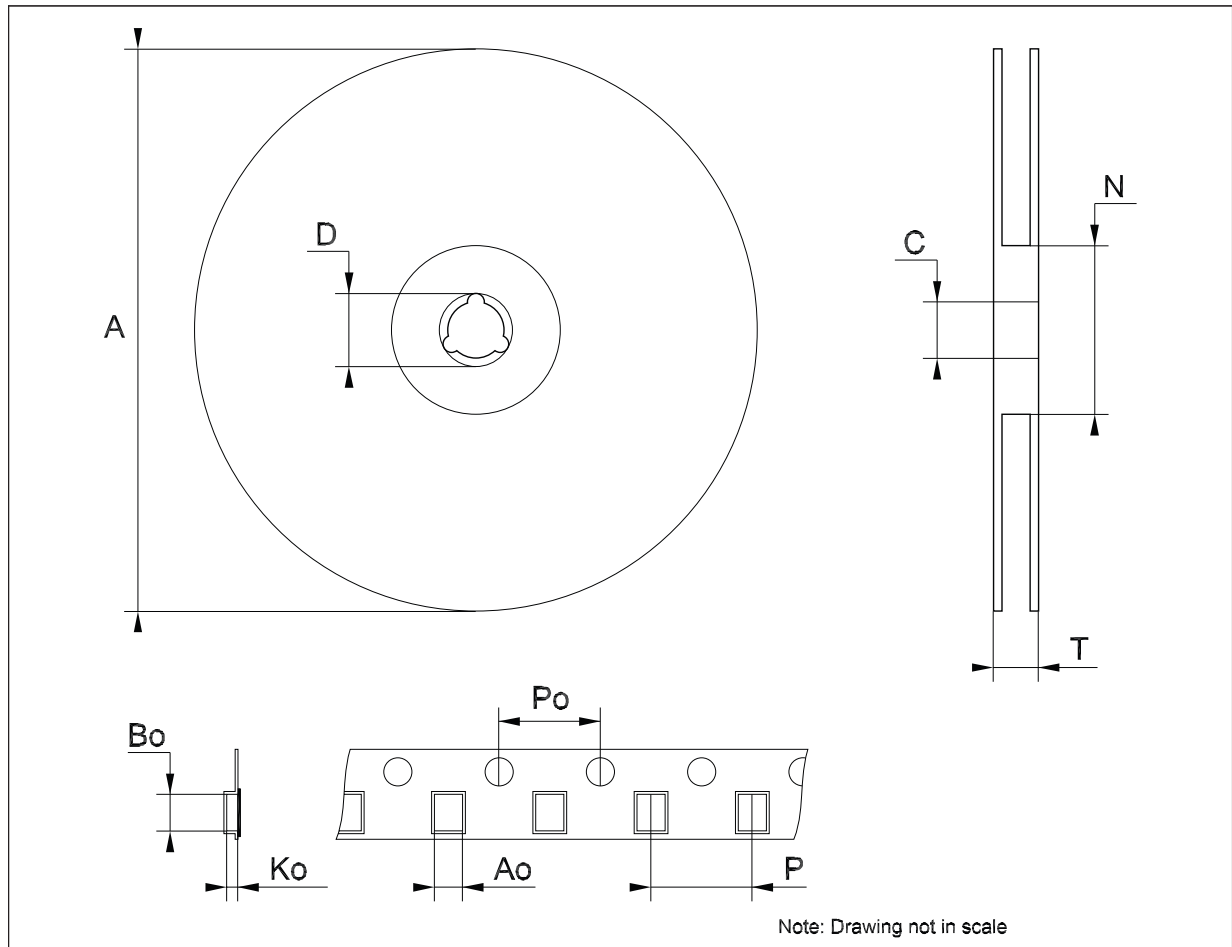
SOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



Tape & reel SOT23-xL mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



7 Order codes

Table 6. Order codes

Part number	Output voltage	V _{OUT} Min.	V _{OUT} Max.	Test voltage
LK112SM13TR ⁽¹⁾	1.3V	1.24V	1.36V	2.4V
LK112SM14TR ⁽¹⁾	1.4V	1.34V	1.46V	2.4V
LK112SM18TR	1.8V	1.74V	1.86V	2.4V
LK112SM19TR ⁽¹⁾	1.9V	1.84V	1.96V	2.4V
LK112SM20TR ⁽¹⁾	2.0V	1.94V	2.06V	3.0V
LK112SM21TR ⁽¹⁾	2.1V	2.04V	2.16V	3.1V
LK112SM22TR ⁽¹⁾	2.2V	2.14V	2.26V	3.2V
LK112SM23TR ⁽¹⁾	2.3V	2.24V	2.36V	3.3V
LK112SM24TR ⁽¹⁾	2.4V	2.34V	2.46V	3.4V
LK112SM26TR ⁽¹⁾	2.6V	2.54V	2.66V	3.6V
LK112SM28TR	2.8V	2.74V	2.86V	3.8V
LK112SM29TR ⁽¹⁾	2.9V	2.84V	2.96V	3.9V
LK112SM31TR ⁽¹⁾	3.1V	3.04V	3.16V	4.1V
LK112SM33TR	3.3V	3.24V	3.36V	4.3V
LK112SM34TR ⁽¹⁾	3.4V	3.335V	3.465V	4.4V
LK112SM35TR ⁽¹⁾	3.5V	3.435V	3.565V	4.5V
LK112SM36TR ⁽¹⁾	3.6V	3.535V	3.655V	4.6V
LK112SM37TR ⁽¹⁾	3.7V	3.630V	3.770V	4.7V
LK112SM38TR ⁽¹⁾	3.8V	3.725V	3.875V	4.8V
LK112SM39TR ⁽¹⁾	3.9V	3.825V	3.975V	4.9V
LK112SM41TR ⁽¹⁾	4.1V	4.020V	4.180V	5.1V
LK112SM42TR ⁽¹⁾	4.2V	4.120V	4.280V	5.2V
LK112SM43TR ⁽¹⁾	4.3V	4.215V	4.385V	5.3V
LK112SM44TR ⁽¹⁾	4.4V	4.315V	4.485V	5.4V
LK112SM45TR ⁽¹⁾	4.5V	4.410V	4.590V	5.5V
LK112SM46TR ⁽¹⁾	4.6V	4.510V	4.690V	5.6V
LK112SM47TR ⁽¹⁾	4.7V	4.605V	4.795V	5.7V
LK112SM48TR ⁽¹⁾	4.8V	4.705V	4.895V	5.8V
LK112SM49TR ⁽¹⁾	4.9V	4.800V	5.000V	5.9V
LK112SM50TR	5.0V	4.900V	5.100V	6.0V

1. Available on request.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
31-Aug-2004	3	Mistake on fig. 19.
31-Jan-2005	4	Change maturity code.
12-Jun-2006	5	Order codes updated.
17-Oct-2006	6	The T _{OP} value on table 2 updated.
20-Jul-2007	7	Add Table 1 in cover page.
21-Sep-2007	8	Features updated.
11-Dec-2007	9	Modified: Table 6 .
12-Feb-2008	10	Modified: Table 6 on page 15 .
10-Jul-2008	11	Modified: Table 1 on page 1 and Table 6 on page 15 .

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