KM93CS56/KM93CS66 CMOS EEPROM

2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Write protection with memory pointer**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **Memory organization:**
  - **— 256 x 16 bits for KM93CS66**
  - **— 128 x 16 bits for KM93CS56**
- **System Clock Frequency: 1 MHz (max.)**
- **Self timed write cycle**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

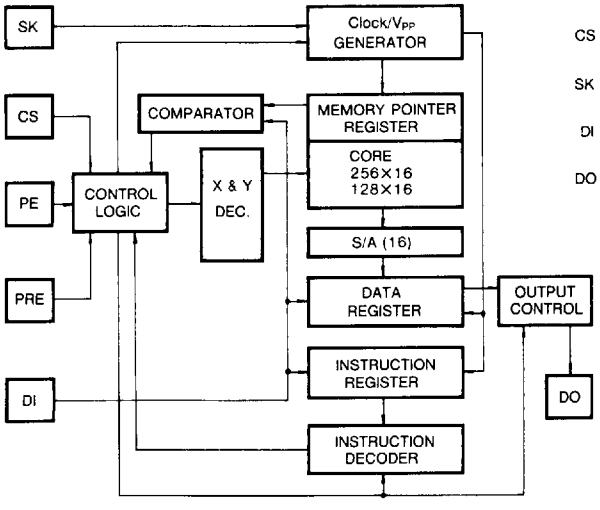
GENERAL DESCRIPTION

The KM93CS56/66 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

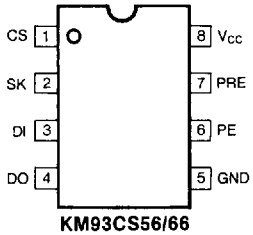
The KM93CS56/66 can be organized as 128/256 registers of 16 bits each, which can be read/written serially and provides data security feature with the memory pointer against the data modification. Besides, this memory pointer address can be locked permanetly.

The KM93CS56/66 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

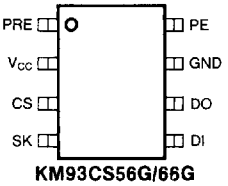
FUNCTIONAL BLOCK DIAGRAM



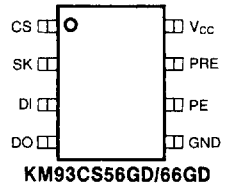
PIN CONFIGURATION



KM93CS56/66



KM93CS56G/66G (S56/66)



KM93CS56GD/66GD (S56D/66D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	250	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	100	μA
Input Low Voltage Levels		V_{IL}		-0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	Vcc+0.3	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
PRE Setup Time	t_{PRES}	Relative to SK	50	—	ns
PE Setup Time	t_{PES}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
PE Hold Time	t_{PEH}	Relative to CS	100	—	ns
PRE Hold Time	t_{PREH}	Relative to CS	100	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in Tri-state	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

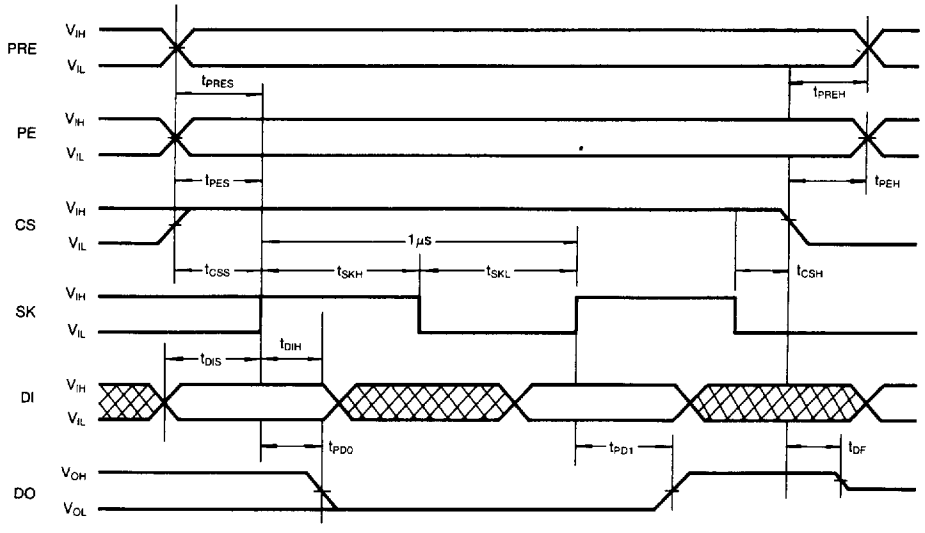
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	PRE	PE	Comment
READ	1	10	A7 - A0	D_{OUT}	0	X	Read register starting at specified address
WRITE	1	01	A7 - A0	D_{15}-D_0	0	1	Write data at memory
EWEN	1	00	11XXXXXX	—	0	1	Erase/Write enable
EWDS	1	00	00XXXXXX	—	0	X	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	0	1	Write all registers
MPRRD	1	10	XXXXXXXX	D_{OUT}	1	X	Read MPR*[1]
MPREN	1	00	11XXXXXX	—	1	1	Enable MPR write related instructions
MPRCLR	1	11	11111111	—	1	1	Clear the MPR
MPRWRT	1	01	A7 - A0	—	1	1	Write address in MPR*
MPRDS	1	00	00000000	—	1	1	One time only instruction to lock the MPR address permanently

Note: 1. MPR: Memory Pointer Register
2. A7 is a "don't care" address for KM93CS56

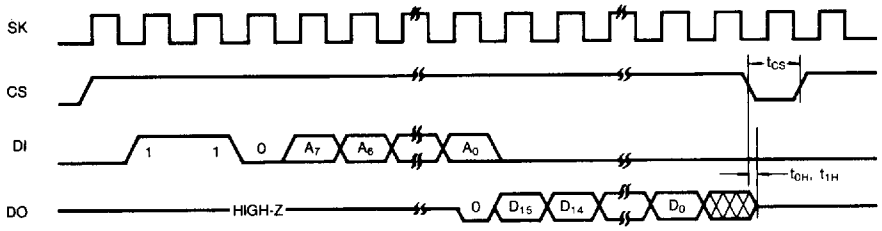
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



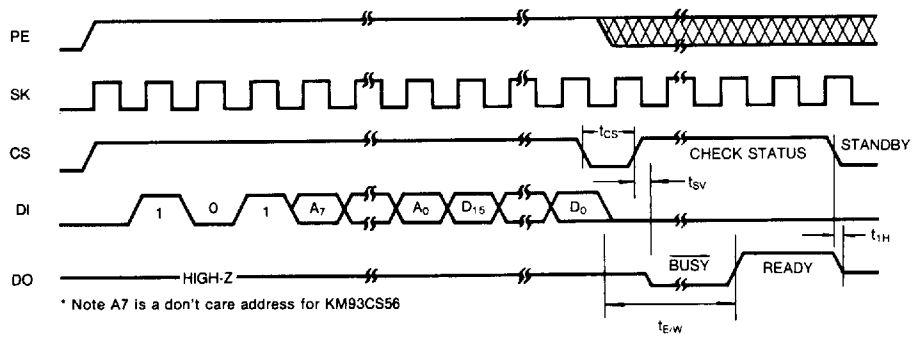
SAMSUNG ELECTRONICS

READ (PRE=V_{IL}, PE="Don't Care")



* Note A7 is a don't care address for KM93CS56

WRITE (PRE=V_{IL})



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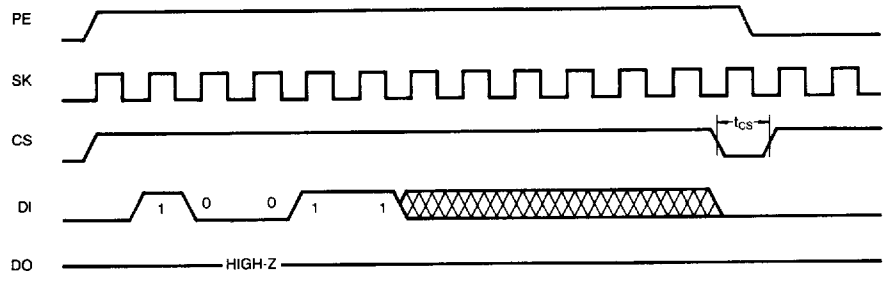
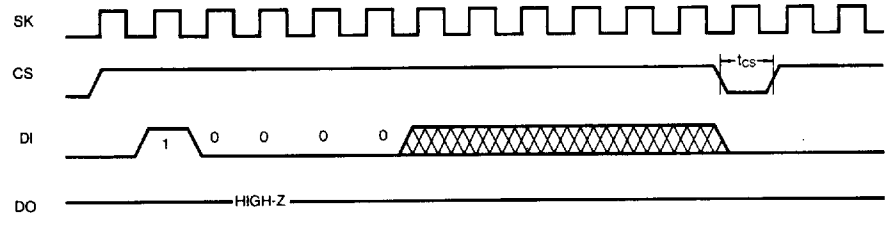
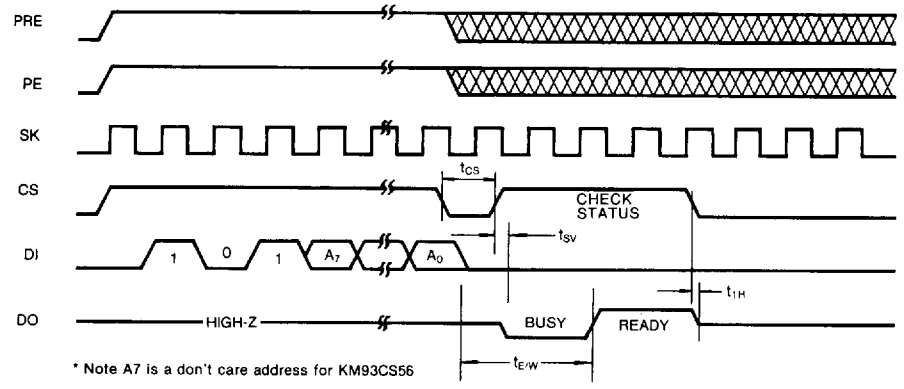
EWEN (PRE=V_{IL})



EWDS (PRE=V_{IL}, PE="Don't Care")



MPRWRT



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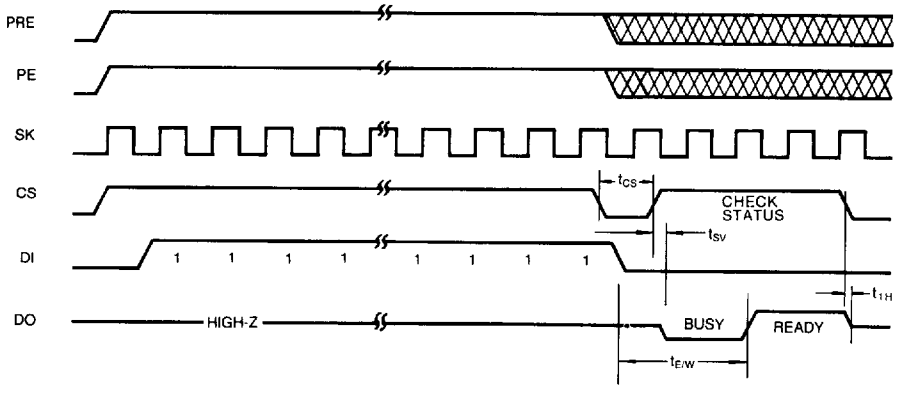
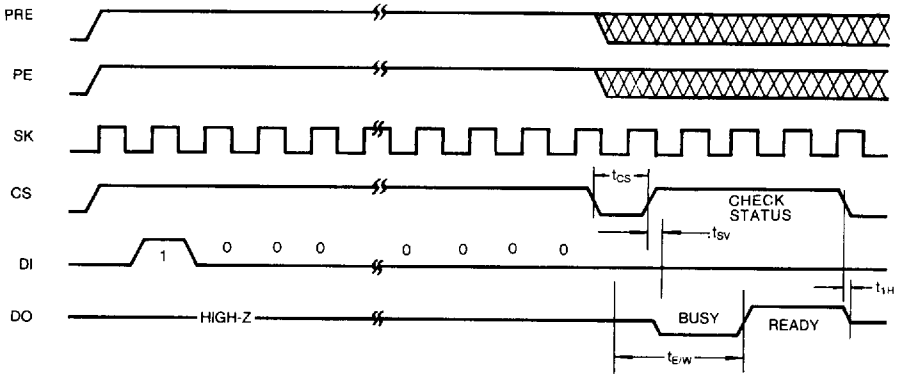
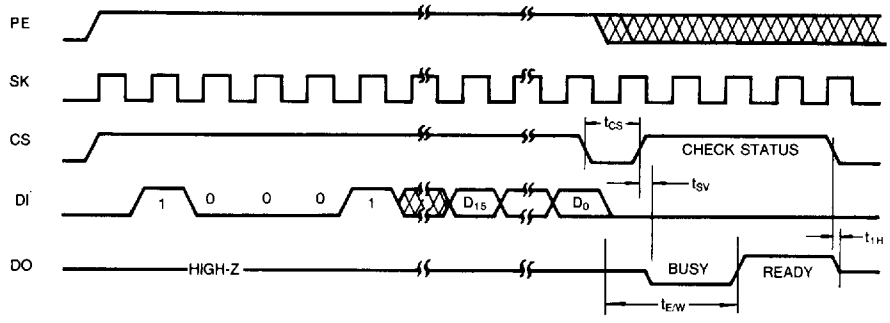
MPRCLR



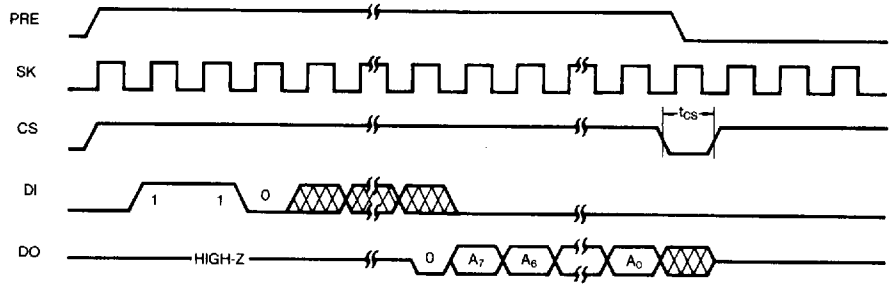
MPRDS



WRAL (PRE=V_{IL})



MPRRD (PE="Don't Care")



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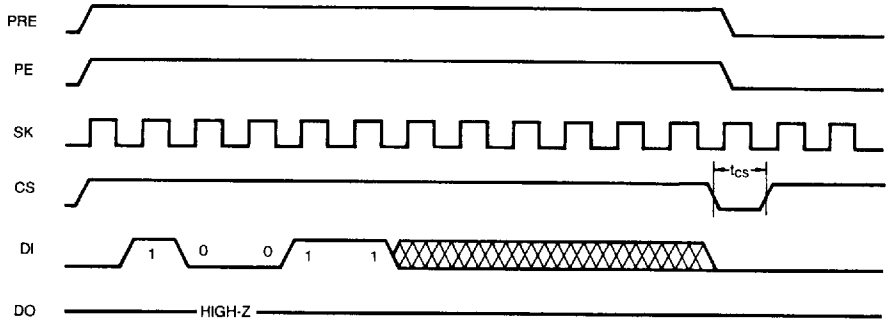
MPREN



INTRODUCTION

The KM93CS56/66 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93CS56/66 is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention. The KM93CS56/66 offers a data security feature with memory pointer to prevent the protected memory register. Once defined the memory pointer, the memory register is divided into a read/write area and read only area. The addresses equal to or greater than the memory pointer are protected from the Write operation unless clearing the memory pointer register.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string. After 16 bits are clocked out, the device read out the next address automatically. To terminate the read operation CS pin must be toggled high to low.

EWEN/EWDS

The KM93CS56/66 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle. During loading the WRITE instruction, the PE pin must be high, however after loading the WRITE instruction, the PE pin becomes "don't care".

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are writen simultaneously with given data. The WRAL instruction is valid only when the memory pointer register has been cleared by executing a MPRCLR instruction and while loading the WRAL instruction, the PE pin must be held high, however after loading the WRAL instruction, the PE pin becomes "don't care"

MPRRD

The memory pointer register read (MPRRD) instruction outputs serial 8-bit address stored in the memory pointer register on the DO pin. Like the read operation, a dummy bit (logical "0") precedes the 8 bit address string. While loading the MPRRD instruction, PRE pin must be held high.

MPREN

The memory pointer register enable (MPREN) instruction is used to enable the MPRCLR. MPRWRT and MPRDS modes. The device must be in EWEN mode, before MPREN mode is executed. Both the PRE and PE pin must be held high while loading the MPREN instruction, however after loading the instruction, PE and PRE pins become "don't care". Note that MPREN instruction must be immediately preceded before executing a MPRCLR, MPRWRT, or MPRDS instruction.

MPRCLR

The memory pointer clear (MPRCLR) instruction reset the address stored in the memory pointer register. After executing the MPRCLR, the entire memory register can be programmed by using WRITE and WRAL instruction. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care".

MPRWRT

The memory pointer register write (MPRWRT) instruction program the memory pointer address into the memory pointer register. Once defined the memory pointer address, the memory registers, which has greater than or equal to the memory pointer address, are protected from the data modification. The memory pointer register must be reset before moving the memory pointer address, by executing the MPRCLR instruction. Both the PRE and PE pin must be held high while loading the MPWRT instruction. Once enabled this instruction, both the PE and PRE pins become "don't care"

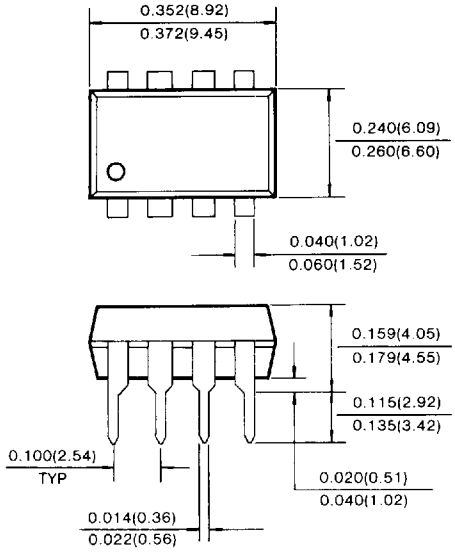
MPRDS

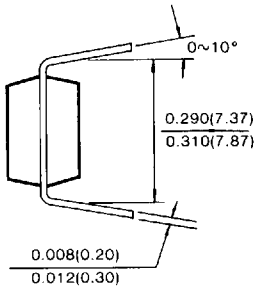
The memory pointer function disable (MPRDS) instruction is one time only instruction. The MPRWRT, MPRCLR, and MPREN instruction is disabled by executing this instruction. Therefore the address of the memory pointer register is permanently unalterable so that the memory registers whose address is greater than or equal to the memory pointer address, are not afford to modify the data permanetly. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care."

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)





8 PIN PLASTIC SMALL OUT LINE PACKAGE