MR27V3202F

2M–Word × 16–Bit or 4M–Word × 8–Bit P2ROM

FEATURES

· 2,097,152-word × 16-bit / 4,194,304-word × 8-bit electrically switchable configuration
· +3.0 V to 3.6 V power supply
· Access time 80 ns MAX
· Operating current 20 mA MAX (5MHz)
· Standby current 10 µA MAX
· Input/Output TTL compatible
· Three-state output

PACKAGES

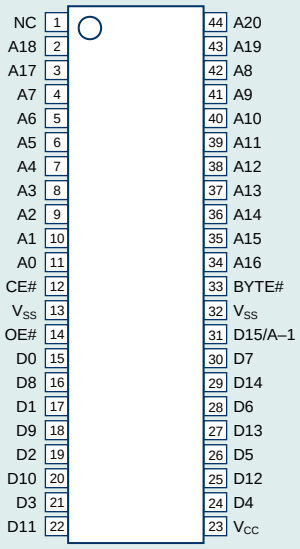
· MR27V3202F-xxxMA
  44-pin plastic SOP (SOP44-P-600-1.27-K)
· MR27V3202F-xxxTP
  44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)
· MR27V3202F-xxxTN
  48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

P2ROM ADVANCED TECHNOLOGY

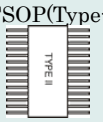
P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor's technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

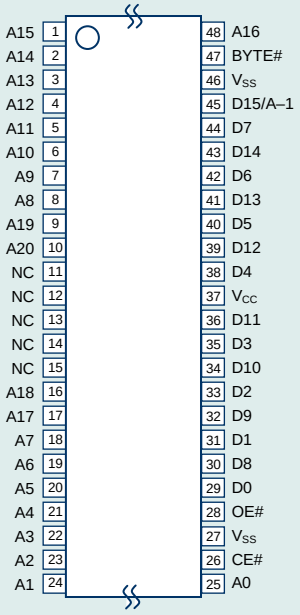
- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge,** unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.
- **Pin Compatible with Mask ROM** and some FLASH products.

PIN CONFIGURATION (TOP VIEW)



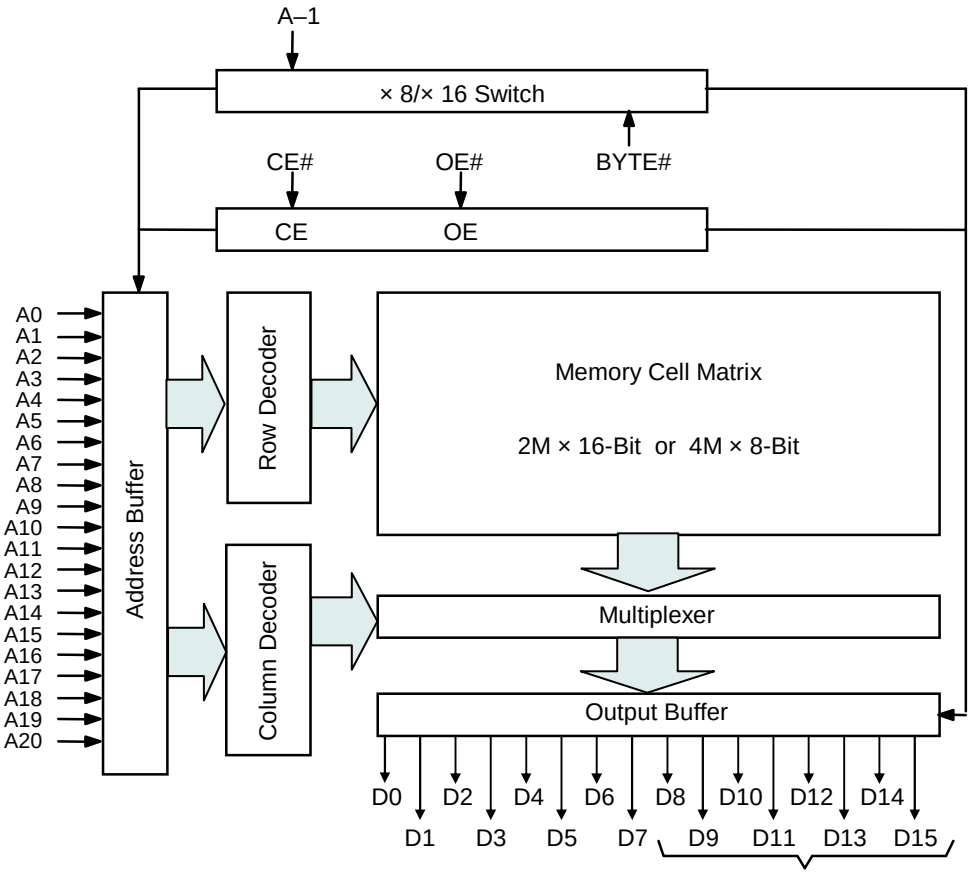
44SOP,
44TSOP(Type-II)





48TSOP(Type-I)

BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A–1	Data output / Address input
A0 to A20	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V_{CC}	Power supply voltage
V_{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V_{CC}	D0 to D7	D8 to D14	D15/A–1
Read (16-Bit)	L	L	H	3.3 V	D_{OUT}		
Read (8-Bit)	L	L	L		D_{OUT}	Hi–Z	L/H
Output disable	L	H	H		Hi–Z		
			L				*
Standby	H	*	H		Hi–Z		
			L				*

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Ta	—	0 to 70	°C
Storage temperature	Tstg		–55 to 125	°C
Input voltage	V_I	relative to V_{SS}	–0.5 to V_{CC}+0.5	V
Output voltage	V_O		–0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		–0.5 to 5	V
Power dissipation per package	P_D	Ta = 25°C	1.0	W
Output short circuit current	I_{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	V_{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V_{IH}		2.2	—	V_{CC}+0.5*	V
Input "L" level	V_{IL}		–0.5**	—	0.6	V

Voltage is relative to V_{SS}.
* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	8	pF
BYTE#	C_{IN2}		—	—	120	
Output	C_{OUT}	V_O = 0 V	—	—	10	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	—	—	10	µA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	—	—	10	µA
V_{CC} power supply current (Standby)	I_{CCSC}	CE# = V_{CC}	—	—	10	µA
	I_{CCST}	CE# = V_{IH}	—	—	1	mA
V_{CC} power supply current (Read)	I_{CCA}	CE# = V_{IL}, OE# = V_{IH} f=5MHz	—	—	20	mA
Input “H” level	V_{IH}	—	2.2	—	V_{CC}+0.5*	V
Input “L” level	V_{IL}	—	–0.5**	—	0.6	V
Output “H” level	V_{OH}	I_{OH} = –2 mA	2.4	—	—	V
Output “L” level	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V

Voltage is relative to V_{SS}.
* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

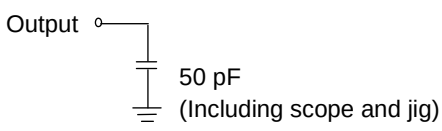
(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t_C	—	80	—	ns
Address access time	t_{ACC}	CE# = OE# = V_{IL}	—	80	ns
CE# access time	t_{CE}	OE# = V_{IL}	—	80	ns
OE# access time	t_{OE}	CE# = V_{IL}	—	30	ns
Output disable time	t_{CHZ}	OE# = V_{IL}	0	20	ns
	t_{OHZ}	CE# = V_{IL}	0	20	ns
Output hold time	t_{OH}	CE# = OE# = V_{IL}	0	—	ns

Measurement conditions

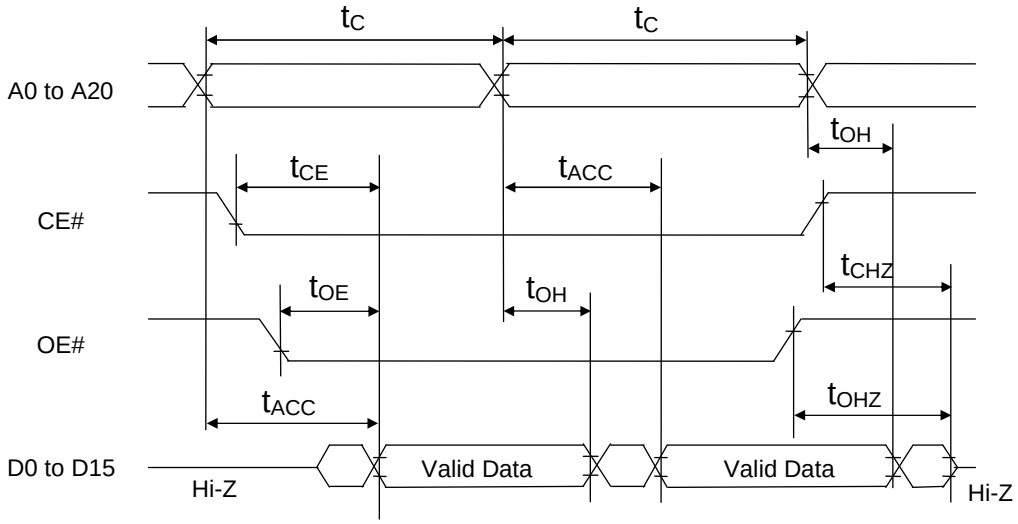
Input signal level ----------0 V/3 V
Input timing reference level----------1/2Vcc
Output load ----------50 pF
Output timing reference level ---------- 1/2Vcc

Output load

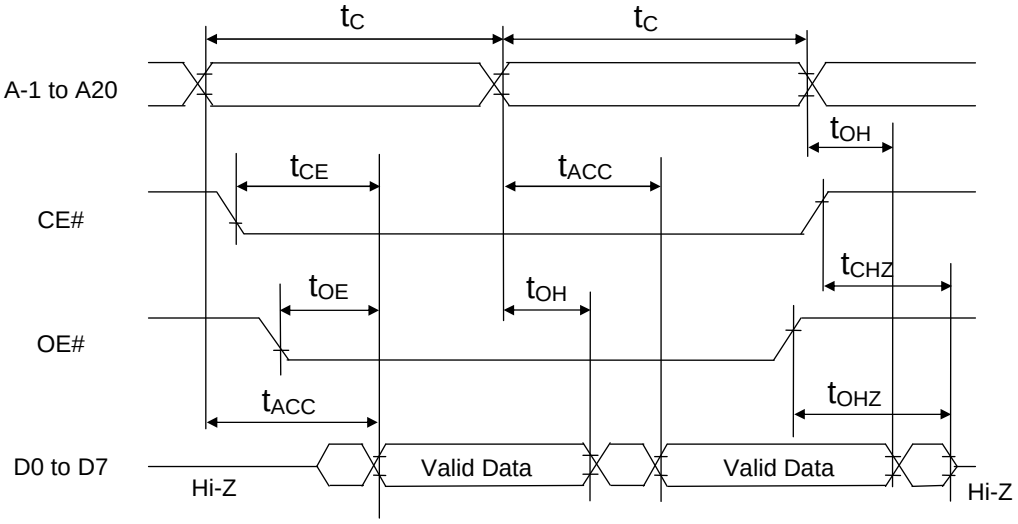


TIMING CHART (READ CYCLE)

16-BIT READ MODE (BYTE# = V_{IH})



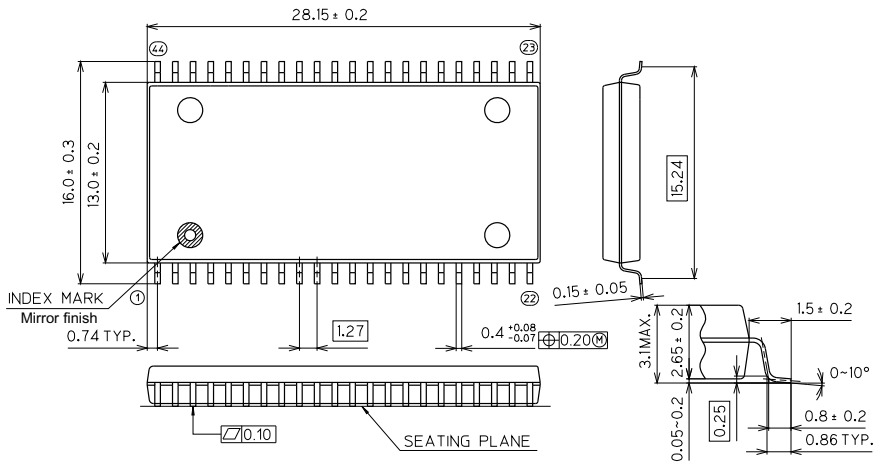
8-BIT READ MODE (BYTE# = V_{IL})



PACKAGE DIMENSIONS

(Unit: mm)

SOP44-P-600-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	2.10 TYP.
Rev. No./Last Revised	4/Dec. 5, 1996

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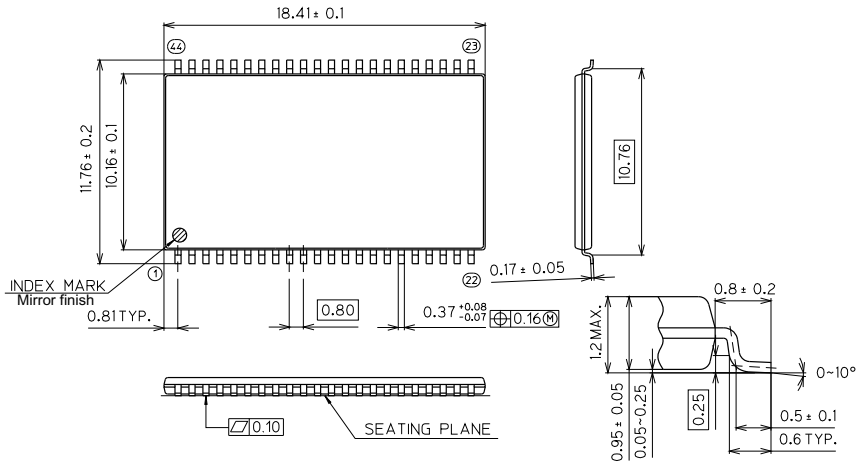
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

TSOP(2)44-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.54 TYP.
Rev. No./Last Revised	3/Dec. 10, 1996

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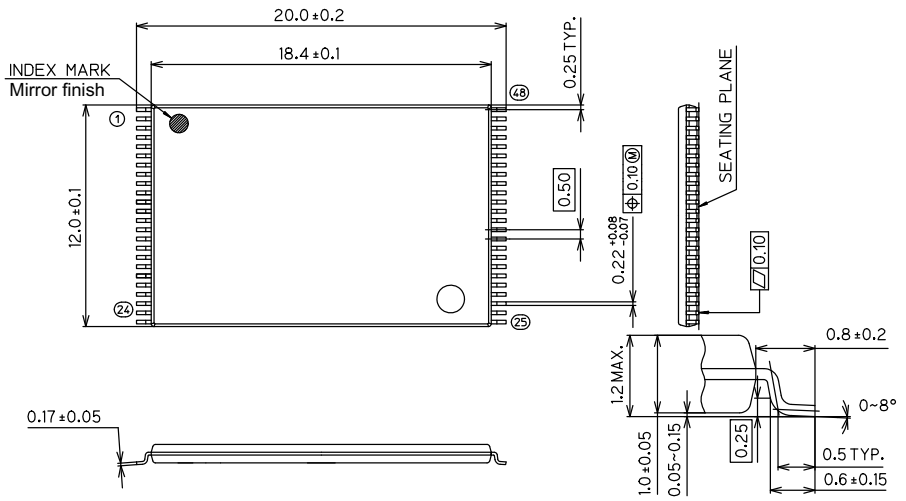
(Unit: mm)

TSOP(1)48-P-1220-0.50-1K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Dec. 2, 1999

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27V3202F-02-01	Oct., 2000	–	–	Final edition 1
FEDR27V3202F-02-02	Mar., 2002	5	4	Changed t_C, t_{ACC}, t_{CE} to 80ns
				Added I_{CCA2} at t_C = 200ns Change the symbol, I_{CCA} to I_{CCA1}
				Changed I_{CCA1} to 30mA
				Changed t_{OE} to 30ns
				Changed I_{CCSC} to 10uA
		1-4, 7	1-3	Changed the form
FEDR27V3202F-02-03	Jun. 6, 2003	1	1	Change 48TSOP(1) package code to –1K
		1, 4	1, 4	Unify I_{CCA} condition into f=5MHz
FEDR27V3202F-02-04	Jul. 8, 2003	4	4	Change t_{CHZ}, t_{OHZ} to 20ns
FEDR27V3202F-02-05	Jul. 9, 2004	3	3	Add P_D condition and I_{OS} = 10mA

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