

**54ACT11240, 74ACT11240  
OCTAL BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

SCAS210 - D3410, MAY 1987 - REVISED APRIL 1993

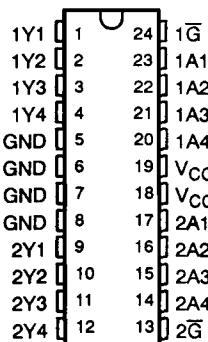
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

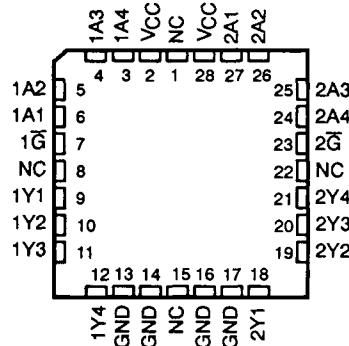
These octal buffers or line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical  $\bar{G}$  (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT11240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**54ACT11240 . . . JT PACKAGE  
74ACT11240 . . . DB, DW OR NT PACKAGE  
(TOP VIEW)**



**54ACT11240 . . . FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE  
(each buffer)**

INPUTS		OUTPUT
$\bar{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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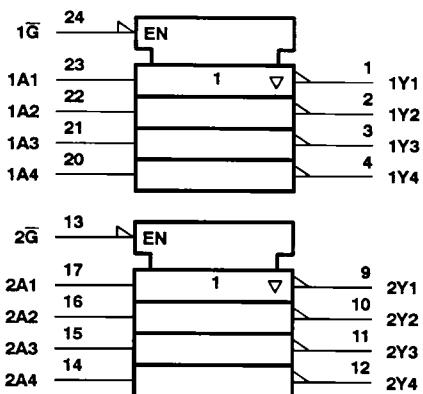


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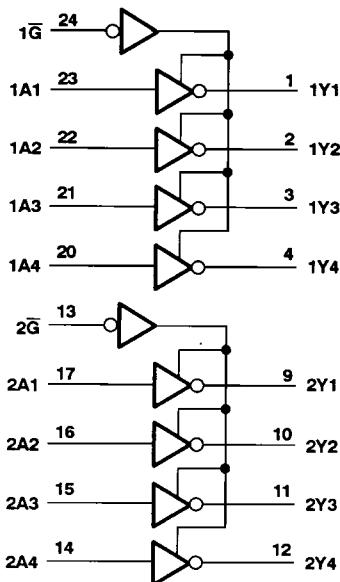
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**logic symbol<sup>†</sup>**



**logic diagram (positive logic)**



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984  
and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	± 20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	± 50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	± 50 mA
Continuous current through $V_{CC}$ or GND .....	± 200 mA
Storage temperature range .....	-65°C to 150°C

<sup>‡</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I <sub>OH</sub> = -50 mA†	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 50 mA†	5.5 V				1.65				
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.5		± 10		± 5		µA
		5.5 V		± 0.1		± 1		± 1		
	I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V							
	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	160		80		
	ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.9	1		1		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4						pF
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range,  
 V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.5	6.5	9.9	1.5	11.1	1.5	10.6	ns
			1.5	6	8	1.5	9.2	1.5	8.7	
t <sub>PZH</sub>	G	Y	1.5	7.5	11.7	1.5	13.1	1.5	12.5	ns
			1.5	7.3	11.5	1.5	12.8	1.5	12.3	
t <sub>PHZ</sub>	G	Y	1.5	7.3	9.4	1.5	10.3	1.5	10	ns
			1.5	7.9	10.3	1.5	11.2	1.5	10.8	

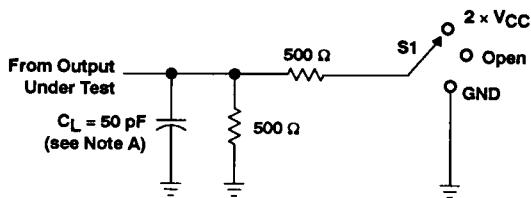
**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS			TYP	UNIT
	C <sub>pd</sub>	Outputs enabled	C <sub>L</sub> = 50 pF, f = 1 MHz		
		Outputs disabled		13	pF

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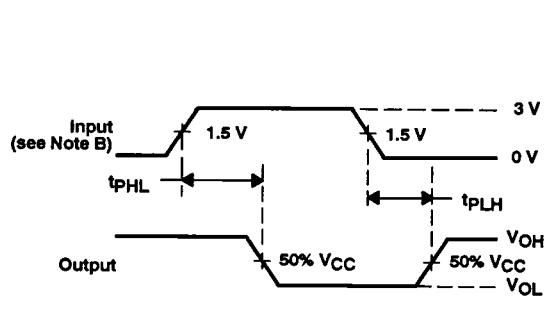
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## **PARAMETER MEASUREMENT INFORMATION**

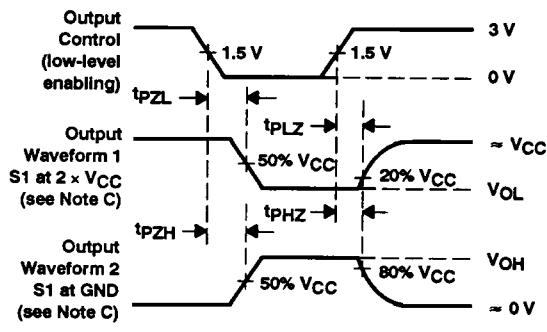


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 x V <sub>CC</sub>
tPHZ/tPZH	GND

#### **LOAD CIRCUIT**



## **VOLTAGE WAVEFORMS**



## VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**