54161, 54163, 54LS161A, 54LS163A
Counters

4-Bit Binary Counters

Product Specification

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('161)**
- **Synchronous reset ('163)**
- **Hysteresis on Clock Input (LS only)**

DESCRIPTION

Synchronous and 4-bit (54161, 54LS161A, 54163, 54LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

ORDERING INFORMATION

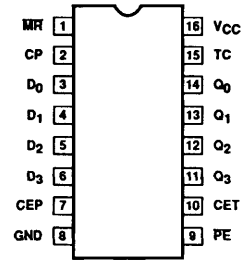
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS161A/BEA 54161/BEA 54LS163A/BEA 54163/BEA
16-Pin Ceramic FlatPack	54LS161A/BFA 54161/BFA 54LS163A/BFA 54163/BFA
20-Pin Ceramic LLCC	54LS161A/B2A 54LS163A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
CP, CET	Inputs	2UL	2LSUL
D, CEP	Inputs	1UL	1LSUL
$\overline{PE}$	Input	1UL	2LSUL
All	Outputs	10UL	10LSUL
$\overline{MR}$	Input ('161)	1UL	1LSUL
$\overline{MR}$	Input ('163)	1UL	2LSUL

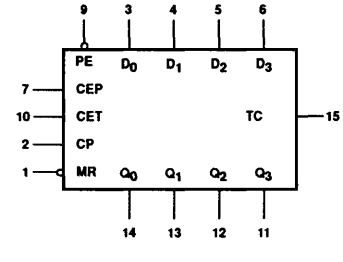
NOTE: Where a 54 Unit Load (UL) is understood to be 40µA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20µA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

A Low level at the Master Reset ($\overline{MR}$) input set all four outputs of the flip-flops (Q_0 - Q_3) in 54161, and 54LS161A to Low levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 54163, and 54LS163A, the clear function is synchronous. A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure 2).

For conventional operation of 54161 and 54163, the following transitions should be avoided.

1. High-to-Low transition on the CEP or CET input if clock is Low.
2. Low-to-High transitions on the Parallel Enable input when CP is Low, if the count enables and $\overline{MR}$ are High at or before the transition.

For 54163 there is an additional transition to be avoided.

3. Low-to-High transition on the $\overline{MR}$ input when clock is Low, if the Enable and $\overline{PE}$ inputs are High at or before the transition.

These restrictions are not applicable to 54LS161A and 54LS163A.

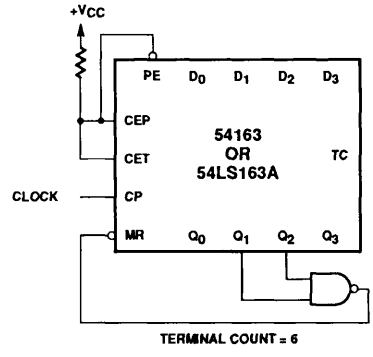
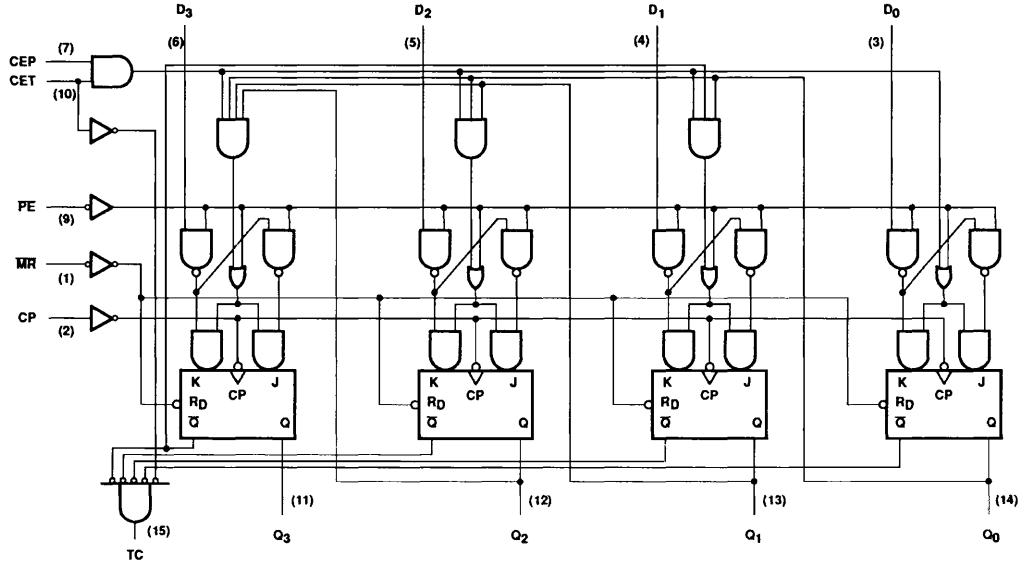


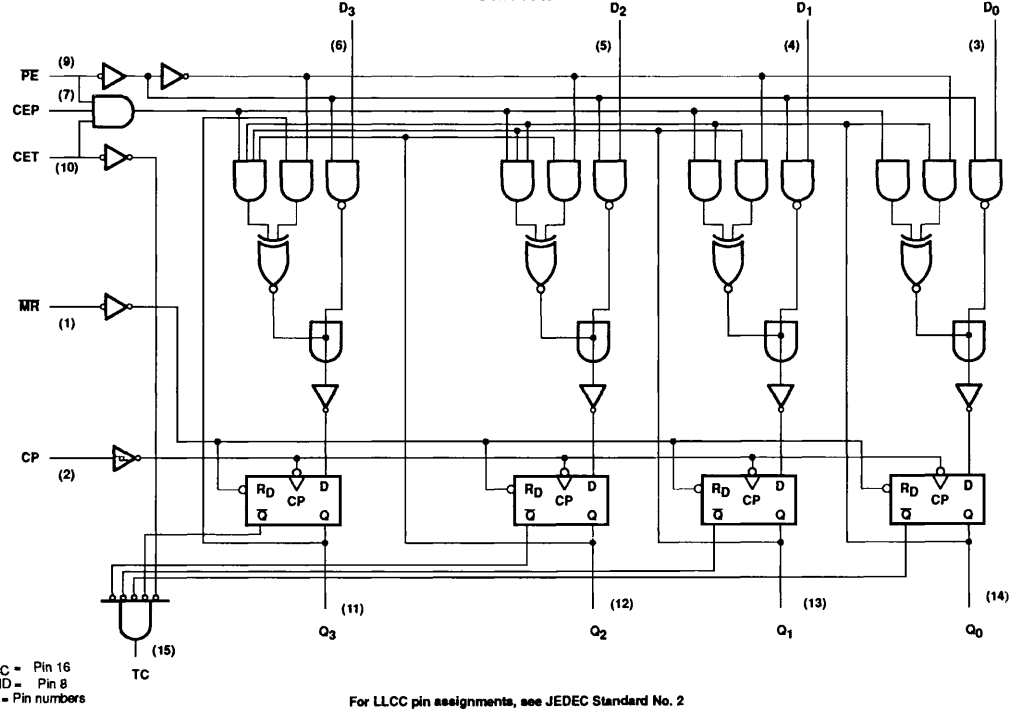
Figure 1

LOGIC DIAGRAMS

54161



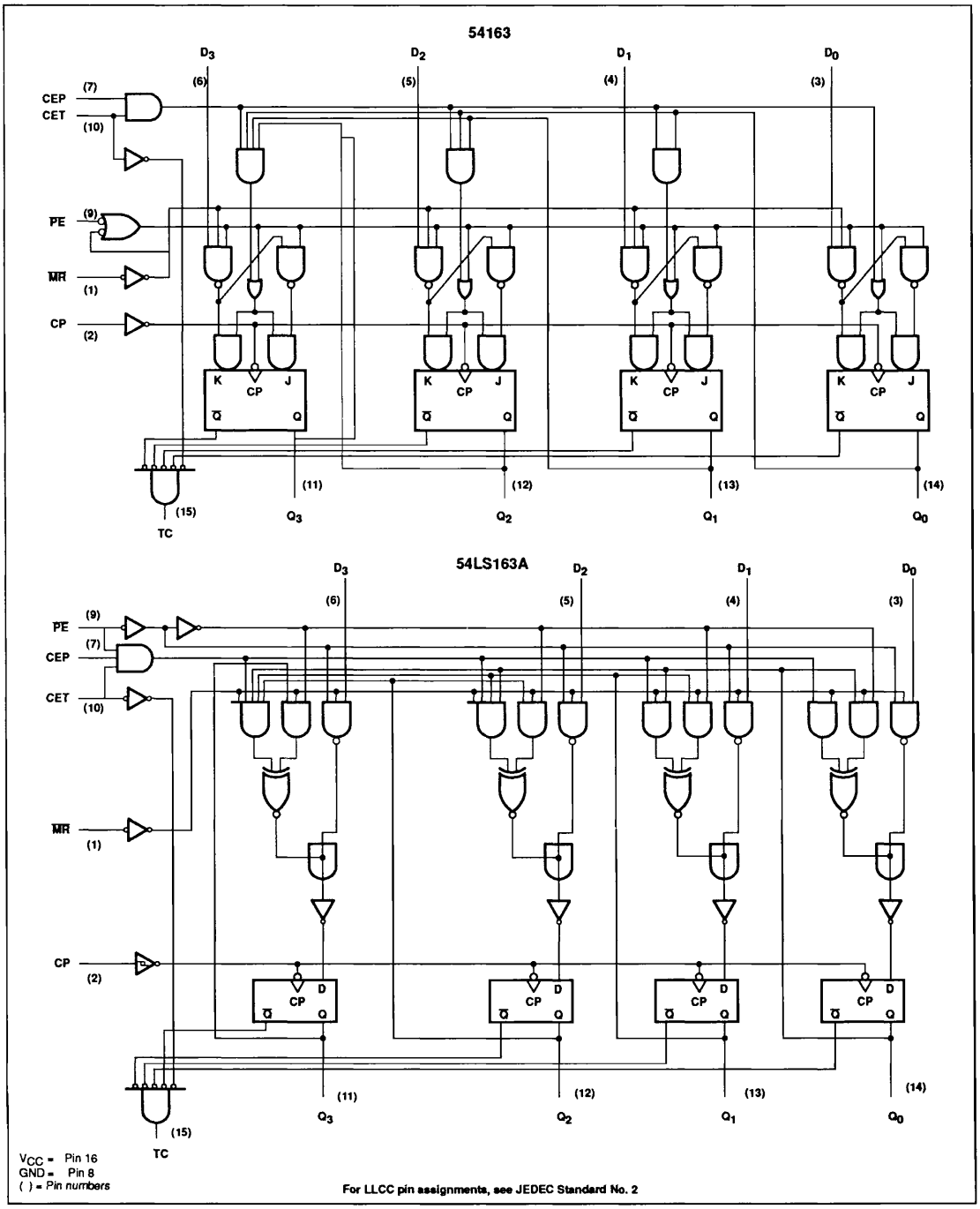
54LS161A



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAMS



MODE SELECT — FUNCTION TABLE, '161

OPERATING MODE	INPUTS						OUTPUT	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h[c]	X	count	(a)
Hold (do nothing)	H	X	l[b]	X	h[c]	X	q_n	(a)
	H	X	X	l[b]	h[c]	X	q_n	L

MODE SELECT — FUNCTION TABLE, '163

OPERATING MODE	INPUTS						OUTPUT	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h[f]	↑	X	X	l	l	L	L
	h[f]	↑	X	X	l	h	H	(d)
Count	h[f]	↑	h	h	h[f]	X	count	(d)
Hold (do nothing)	h[f]	X	l[e]	X	h[f]	X	q_n	(d)
	h[f]	X	X	l[e]	h[f]	X	q_n	L

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTES:
(a) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54161)
(b) The High-to-Low transition of CEP or CET on the 54161 should only occur while CP is High for conventional operation
(c) The Low-to-High transition of $\overline{PE}$ on the 54161 should only occur while CP is High for conventional operation
(d) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for '163)
(e) The High-to-Low transition of CEP or CET on the 54163 should only occur while CP is High for conventional operation
(f) The Low-to-High transition of $\overline{PE}$ or $\overline{MR}$ on the 54163 should only occur while CP is High for conventional operation

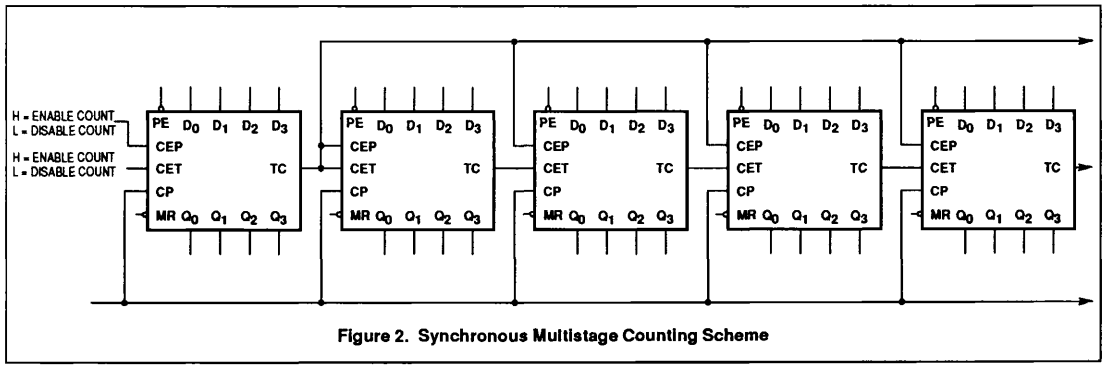


Figure 2. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-800			-400	µA
I_{OL}	Low-level output current			16			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54161, '163			54LS161A, '163A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V				1.0				mA
			V_I = 7.0V	D, CEP						0.1	mA
				$\overline{PE}$, CP, CET						0.2	mA
				$\overline{MR}$, ('LS161A)						0.1	mA
				$\overline{MR}$, ('LS163A)						0.2	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V	CP, CET			80				µA
				Other inputs			40				µA
			V_I = 2.7V	D, CEP						20	µA
				$\overline{PE}$, CP, CET						40	µA
				$\overline{MR}$, ('LS161A)						20	µA
				$\overline{MR}$, ('LS163A)						40	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V	CP, CET			-3.2				mA
				Other inputs			-1.6				mA
			V_I = 0.4V	D, CEP						-0.4	mA
				$\overline{PE}$, CP, CET						-0.8	mA
				$\overline{MR}$, ('LS161A)						-0.4	mA
				$\overline{MR}$, ('LS163A)						-0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-20		-57	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	All outputs High		59	85		18	31	mA
			I_{CCL}	All outputs Low		63	91		19	32	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		35 35		35 35	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		20 23		24 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		25 29		24 27	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		16 16		16 16	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		38		28	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('161)	Waveform 3	20		20		ns
t_W	Master Reset pulse width ('163)	Waveform 6	20		20		ns
t_s	Setup time, data to clock	Waveform 5	20		20		ns
t_h	Hold time, data to clock[5]	Waveform 5	3		3		ns
t_s	Setup time, CEP or CET to clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 5	0		0		ns
t_s	Setup time, $\overline{MR}$ to clock ('163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to clock ('163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	20		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		39 39		40 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		24 27		29 32	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		29 33		29 32	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		20 20		19 19	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		42		33	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		51 51		52 52	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		31 35		38 42	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		38 43		38 42	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		26 26		25 25	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		55		43	ns

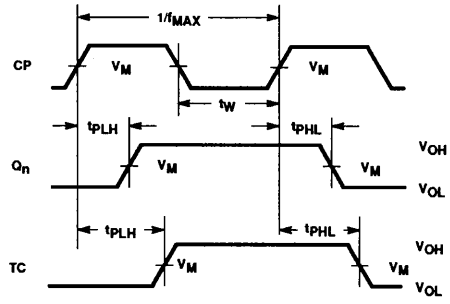
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('161)	Waveform 3	20		25		ns
t_W	Master Reset pulse width ('163)	Waveform 6	20		25		ns
t_s	Setup time, data to clock	Waveform 5	20		25		ns
t_h	Hold time, data to clock[5]	Waveform 5	5		5		ns
t_s	Setup time, CEP or CET to clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 5	0		0		ns
t_s	Setup time, $\overline{MR}$ to clock ('163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to clock ('163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

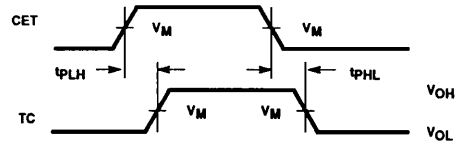
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CCH} is measured with $\overline{PE}$ input High, again with $\overline{PE}$ input Low, all other inputs High and output open. I_{CCL} is measured with Clock input High, again with Clock input Low, all other inputs low and outputs open.
5. For 15ns rise time only, Hold time must be increased by 0.3ns for each nanosecond decrease in rise time.
6. These parameters are guaranteed, but not tested.

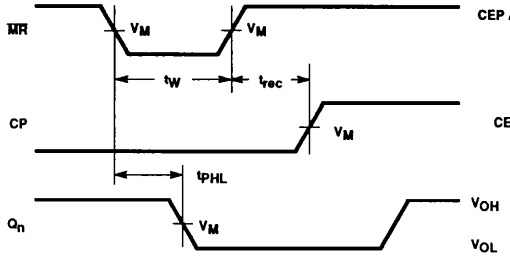
AC WAVEFORMS



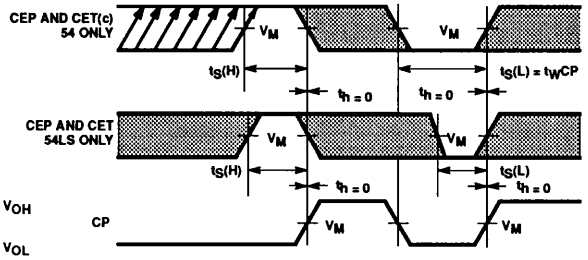
Waveform 1. Clock to Output Delays, Maximum Frequency, and Clock Pulse Width



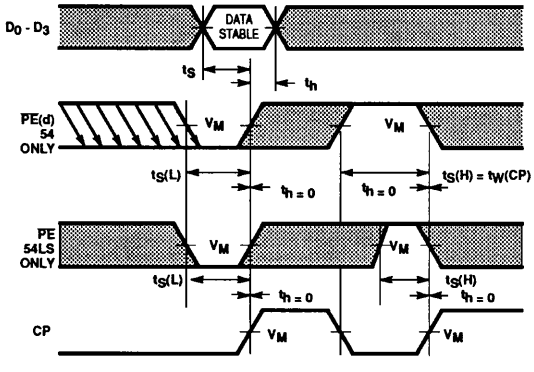
Waveform 2. Propagation Delays CET Input to TC Output



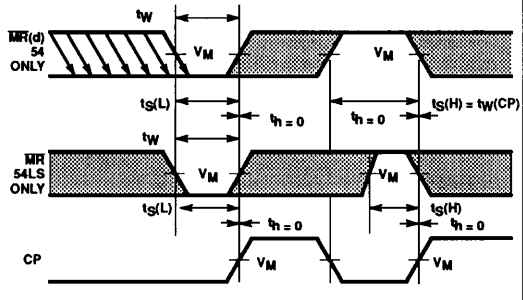
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time ('161)



Waveform 4. CEP and CET Setup and Hold Times



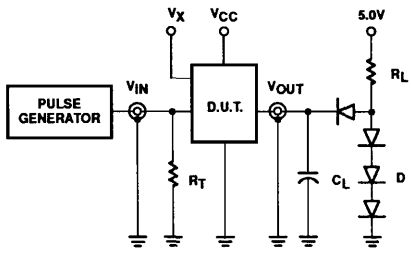
Waveform 5. Parallel Data and Parallel Enable Setup and Hold Times



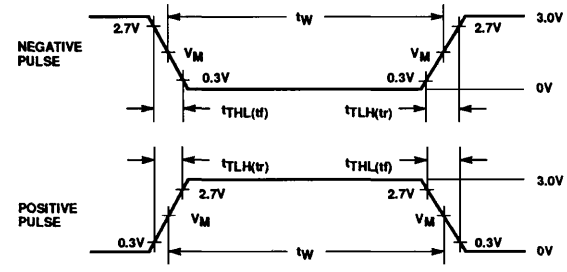
Waveform 6. Synchronous Reset Setup, Pulse Width and Hold Times ('163)

NOTE: V_M = 1.5V for 54; V_M = 1.3 for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.