FAST 74F588
Transceiver

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Non-inverting buffers**
- **Bidirectional data path**
- **B outputs sink 64mA and source 15mA**

DESCRIPTION

The 74F588 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. The B port have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 24mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active High) enables data from A ports to B ports and Receive (active Low) enables data from B ports to A ports. The Output Enable input, when High, disables both A and B ports by placing them in a high-impedance condition.

Octal Bidirectional Transceiver With IEEE-488 Termination Resistors (3 state Inputs and Outputs)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F588	4.0ns	96mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F588N
20-Pin Plastic SOL[1]	N74F588D

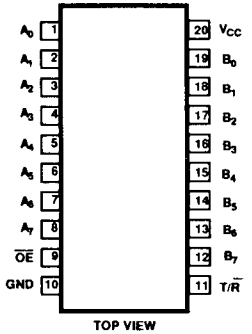
NOTE 1:
Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

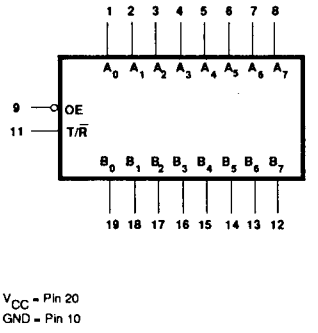
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Port A data inputs	3.5/0.117	70μA/70μA
B_0- B_7	Port B data inputs	T^2/5.33	T^2/3.2mA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	Port A outputs	150/40	3.0mA/24mA
B_0- B_7	Port B outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. T= Resistance Termination per IEEE-488 Standard

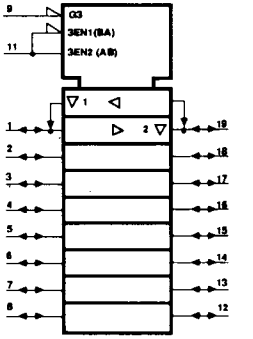
PIN CONFIGURATION



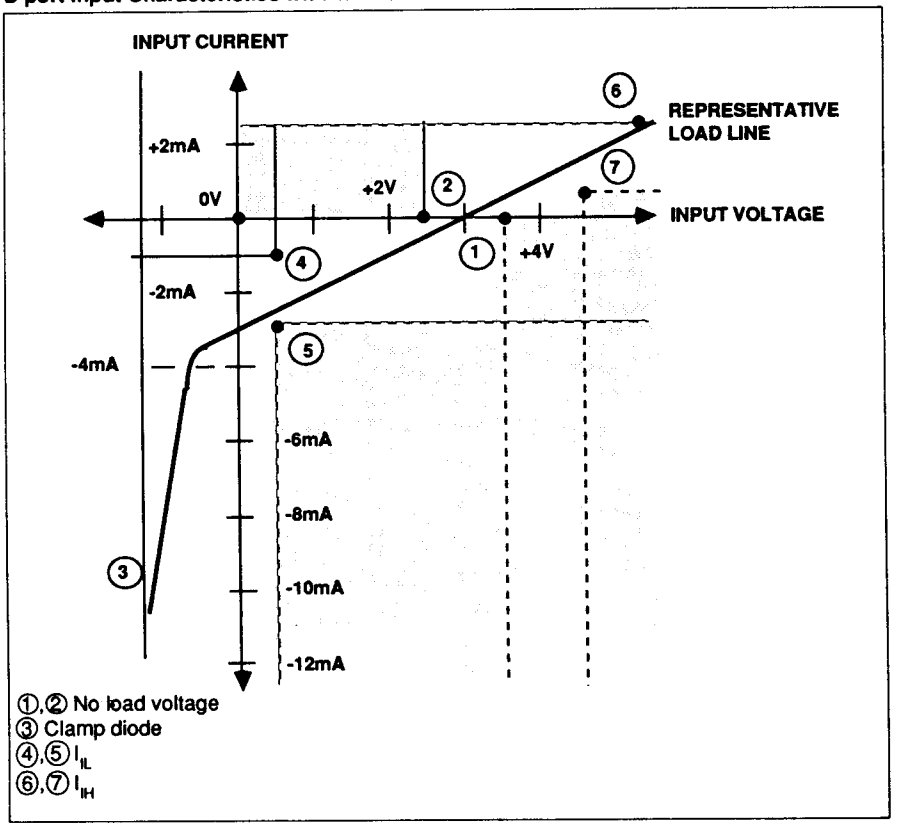
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



B port Input Characteristics with T/$\overline{R}$ Low

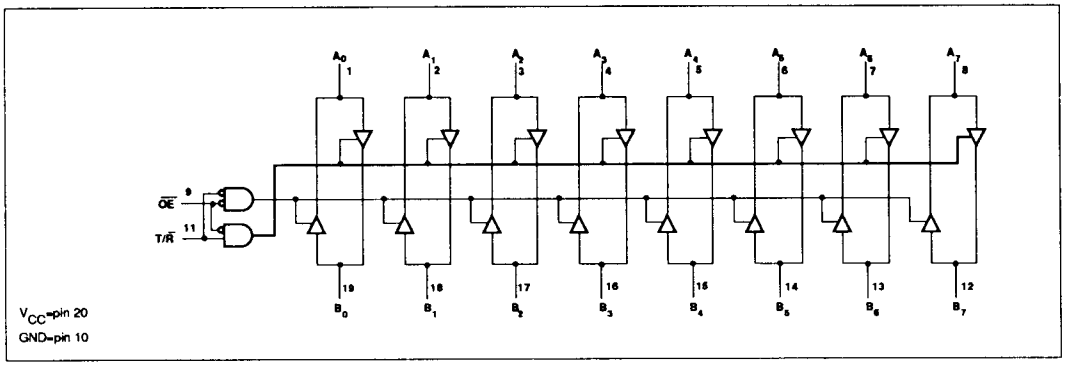


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Currebt applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{NL}	No load voltage	B_0-B_7	I_{OUT} = 0.0mA, T/$\overline{R}$ = 0.0V			2.5		3.7	mA
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_7	V_{CC} = MAX, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7	V_{CC} = MAX, V_I =2.7V, T/$\overline{R}$ =4.5V					70	µA
		B_0-B_7	V_{CC} = MAX, V_I =5.0V, T/$\overline{R}$ =0.0V			0.7			mA
			V_{CC} = MAX, V_I =5.5V, T/$\overline{R}$ =0.0V					2.5	mA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7	V_{CC} = MAX, V_I =0.5V, T/$\overline{R}$ =4.5V					-70	mA
		B_0-B_7	V_{CC} = MAX, V_I =0.4V, T/$\overline{R}$ =0.0V			-1.3		-3.2	mA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=0.0V			82	100	mA
		I_{CCL}		A_n= $\overline{OE}$ =0.0V, T/$\overline{R}$= 4.5V			110	135	mA
		I_{CCZ}		$\overline{OE}$=4.5V			95	125	mA

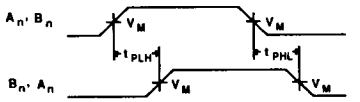
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

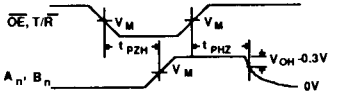
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 2.5	3.5 4.5	6.0 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	5.5 5.0	7.5 7.5	10.0 9.5	5.5 5.0	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.5	4.5 4.0	7.0 7.0	2.5 2.5	8.0 7.5	ns

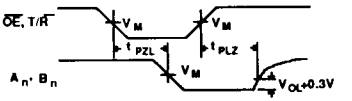
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Outputs



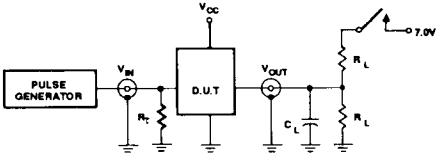
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

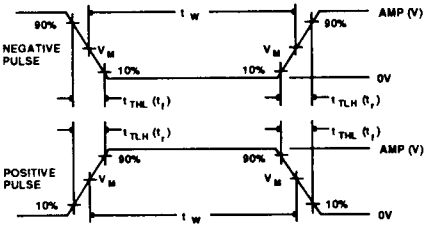
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns