National Semiconductor

74ACT845
8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

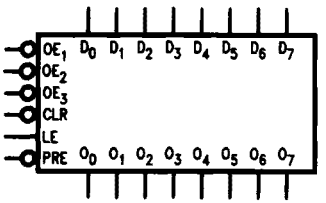
The 'ACT845 is functionally and pin compatible with AMD's Am29845.

Features

- 'ACT845 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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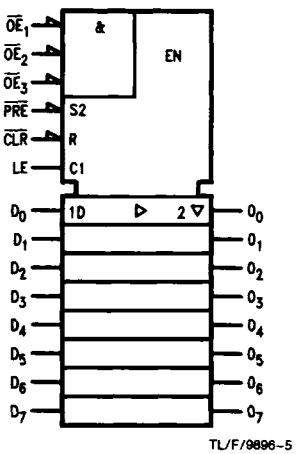

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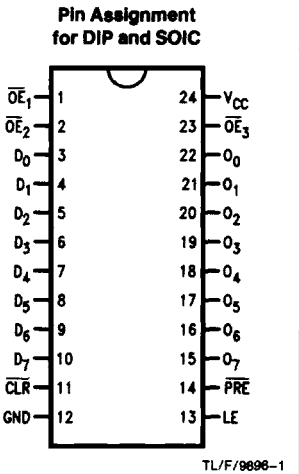
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Connection Diagram



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Functional Description

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

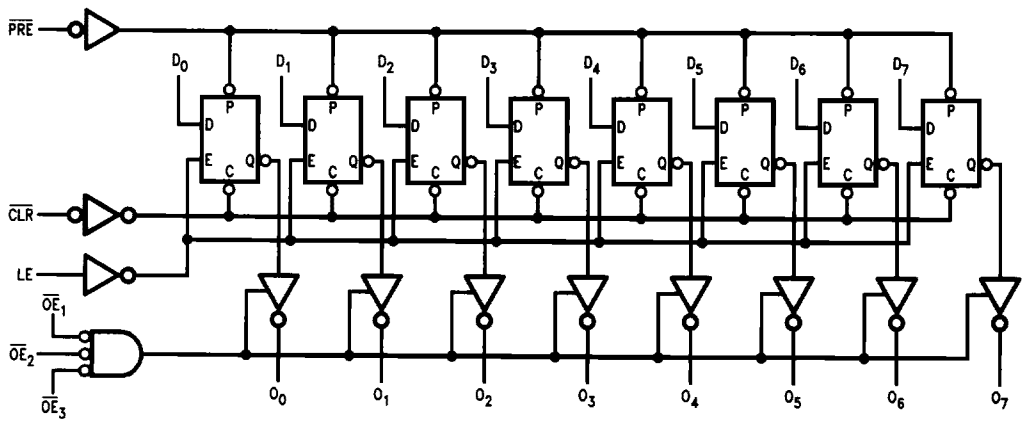
On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_n$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	74ACT T_A = 25°C		74ACT T_A = −40°C to +85°C	Units (V)	V_{CC}	Conditions
		Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	1.5 1.5	2.0 2.0	2.0 2.0	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	1.5 1.5	0.8 0.8	0.8 0.8	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.49 5.49	4.4 5.4	4.4 5.4	V	4.5 5.5	I_{OUT} = −50 μA
			3.86 4.86	3.76 4.76	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	0.001 0.001	0.1 0.1	0.1 0.1	V	4.5 5.5	I_{OUT} = 50 μA
			0.36 0.36	0.44 0.44	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current		±0.1	±1.0	μA	5.5	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current		±0.5	±5.0	μA	5.5	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	0.6		1.5	mA	5.5	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current			75	mA	5.5	V_{OLD} = 1.65V Max
I_{OHD}				−75	mA	5.5	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current		8.0	80	μA	5.5	V_{IN} = V_{CC} or Ground

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	V_{CC}* (V)	Fig. No.
		Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay D_n to O_n	2.0	5.5	9.5	2.0	10.0	ns	5.0	2-3, 4
t_{PHL}	Propagation Delay D_n to O_n	2.0	5.5	9.5	2.0	10.0	ns	5.0	2-3, 4
t_{PLH}	Propagation Delay LE to O_n	2.0	5.5	9.0	2.0	10.0	ns	5.0	2-3, 4
t_{PHL}	Propagation Delay LE to O_n	2.0	5.5	9.0	2.0	10.0	ns	5.0	2-3, 4
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.5	14.0	2.0	16.0	ns	5.0	2-3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	2.0	7.5	15.5	2.0	17.5	ns	5.0	2-3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5	2.0	10.5	ns	5.0	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5	2.0	10.5	ns	5.0	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5	2.0	11.0	ns	5.0	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5	2.0	11.0	ns	5.0	2-6
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.0	10.5	2.0	11.0	ns	5.0	2-3, 4
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	2.0	5.5	9.5	2.0	10.5	ns	5.0	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	V_{CC}* (V)	Fig. No.
		Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	−0.5	0.5	1.0	ns	5.0	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	0.5	2.0	2.0	ns	5.0	2-7
t_w	LE Pulse Width, HIGH	2.0	3.5	3.5	ns	5.0	2-4
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	8.5	10.0	ns	5.0	2-4
t_w	$\overline{CLR}$ Pulse Width, LOW	5.5	9.5	11.0	ns	5.0	2-4
t_{rec}	$\overline{PRE}$ Recovery Time	0.5	2.0	2.0	ns	5.0	2-4, 7
t_{rec}	$\overline{CLR}$ Recovery Time	0	1.0	1.0	ns	5.0	2-4, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	44	pF	V_{CC} = 5.0V