



# 54ABT/74ABT652C

## Octal Transceivers and Registers with TRI-STATE® Outputs

### General Description

The 'ABT652C consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

### Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA

- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

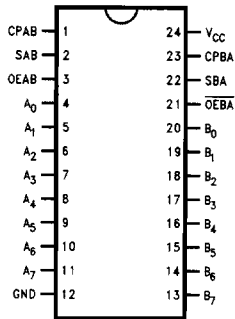
**Ordering Code:** See Section 10

### Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs/ TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

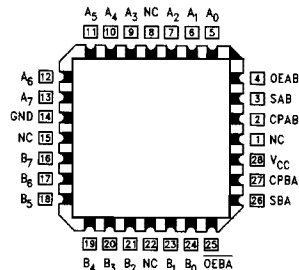
### Connection Diagrams

Pin Assignment for  
DIP, SOIC, SSOP and Flatpak



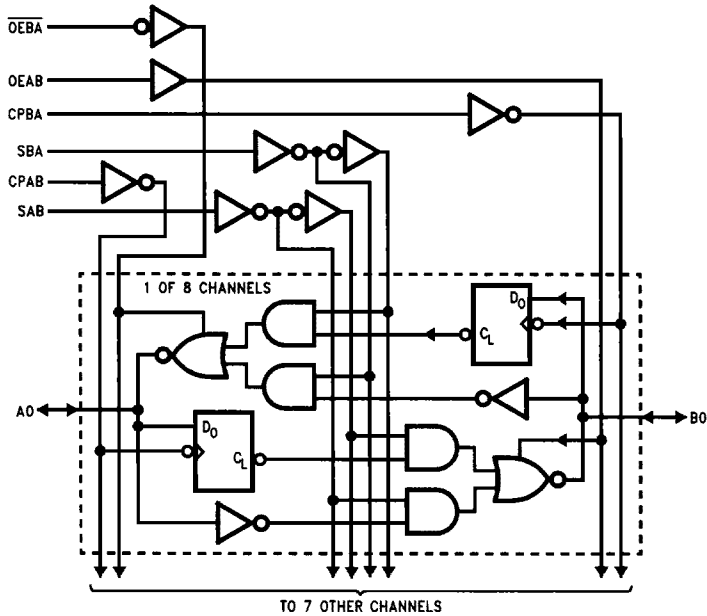
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Pin Assignment for LCC



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## Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Functional Description (Continued)

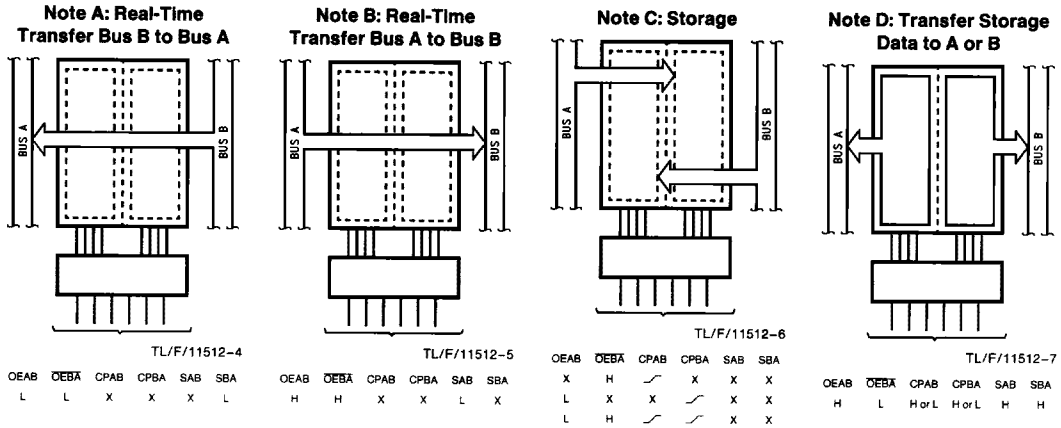


FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	/	/	X	X			Store A and B Data
X	H	/	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	/	/	X	X	Input	Output	Store A in Both Registers
L	X	H or L	/	X	X	Not Specified	Input	Hold A, Store B
L	L	/	/	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L			Real-Time B Data to A Bus
L	L	X	H or L	X	H	Input	Output	Store B Data to A Bus
H	H	X	X	L	X			Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 / = LOW to HIGH Clock Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V <sub>CC</sub>

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

## DC Electrical Characteristics

Symbol	Parameter	ABT652C			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54ABT/74ABT 54ABT 74ABT	2.5 2.0 2.0		V	Min	I <sub>OH</sub> = -3 mA, (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = -24 mA, (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = -32 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54ABT 74ABT		0.55 0.55	V	Min	I <sub>OL</sub> = 48 mA, (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test		4.75		V	0.0	I <sub>ID</sub> = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins) (Note 3) V <sub>IN</sub> = V <sub>CC</sub> (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins) (Note 3) V <sub>IN</sub> = 0.0V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			50	μA	0V-5.5V	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> ); OEBA = 2.0V and OEAB = GND = 2.0V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-50	μA	0V-5.5V	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> ); OEBA = 2.0V and OEAB = GND = 2.0V

**Note 3:** Guaranteed but not tested.

## DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT652C			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0V	V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> ); All Others GND
I <sub>CCH</sub>	Power Supply Current			250	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input			2.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V All others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open (Note 1) OEAB = OEBA = GND One bit toggling, 50% duty cycle (Note 1)

Note 1: For 8 outputs toggling, I<sub>CCD</sub> < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

## DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
							C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.6	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.2	-0.9		V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OHV</sub>	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T <sub>A</sub> = 25° (Note 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	T <sub>A</sub> = 25°C (Note 2)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	0.4	V	5.0	T <sub>A</sub> = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n - 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics (SOIC and SSOP package): See Section 2

Symbol	Parameter	74ABT			54ABT		74ABT		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Max Clock Frequency	200					200		MHz	
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	4.9			1.5	4.9	ns	2-3, 5
t <sub>PHL</sub>	Clock to Bus	1.5	3.4	4.9			1.5	4.9		
t <sub>PLH</sub>	Propagation Delay	1.5	2.6	4.5			1.5	4.5	ns	2-3, 5
t <sub>PHL</sub>	Bus to Bus	1.5	3.0	4.5			1.5	4.5		
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.0			1.5	5.0	ns	2-3, 5
t <sub>PHL</sub>	SBA or SAB to A <sub>n</sub> to B <sub>n</sub>	1.5	3.4	5.0			1.5	5.0		
t <sub>PZH</sub>	Enable Time	1.5	3.3	5.5			1.5	5.5	ns	2-4
t <sub>PZL</sub>	OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub>	1.5	3.7	5.5			1.5	5.5		
t <sub>PHZ</sub>	Disable Time	1.5	3.7	6.0			1.5	6.0	ns	2-4
t <sub>PLZ</sub>	OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub>	1.5	3.3	6.0			1.5	6.0		

**AC Operating Requirements:** See Section 2 for Waveforms

Symbol	Parameter	74ABT		54ABT		74ABT		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max	Min	Max	Min	Max		
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW Bus to Clock	1.5				1.5		ns	2-6
$t_{H(H)}$ $t_{H(L)}$	Hold Time, HIGH or LOW Bus to Clock	1.0				1.0		ns	2-6
$t_{W(H)}$ $t_{W(L)}$	Pulse Width, HIGH or LOW	3.0				3.0		ns	2-3

**Extended AC Electrical Characteristics** (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT		74ABT		74ABT		Units	Fig. No.
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 4)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 250\text{ pF}$ 1 Output Switching (Note 5)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 6)			
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Bus	1.5	5.5	2.0	7.5	2.5	10.0	ns	2-3, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay Bus to Bus	1.5	6.0	2.0	7.0	2.5	9.5	ns	2-3, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay SBA or SAB to $A_n$ or $B_n$	1.5	6.0	2.0	7.5	2.5	10.0	ns	2-3, 5
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OEBA}$ or OEAB to $A_n$ or $B_n$	1.5	6.0	2.0	8.0	2.5	11.5	ns	2-4
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OEBA}$ or OEAB to $A_n$ or $B_n$	1.5	6.0	(Note 7)		(Note 7)		ns	2-4

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

**Note 5:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 7:** The TRI-STATE delay times are dominated by the RC network (500 $\Omega$ , 250 pF) on the output and has been excluded from the datasheet.

**Skew:** See Section 2 (SOIC Package)

Symbol	Parameter	74ABT	74ABT	Units	Fig. No.
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 3)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 4)		
		Max	Max		
$t_{OSHL}$ (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-13
$t_{OSLH}$ (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-13
$t_{PS}$ (Note 5)	Duty Cycle LH-HL Skew	2.0	4.0	ns	2-14
$t_{OST}$ (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-17
$t_{PV}$ (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-20

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW ( $t_{OSHL}$ ), LOW to HIGH ( $t_{OSLH}$ ), or any combination switching LOW to HIGH and/or HIGH to LOW ( $t_{OST}$ ). This specification is guaranteed but not tested.

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and  $V_{CC}$ ) from device to device. This specification is guaranteed but not tested.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

**Note 4:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

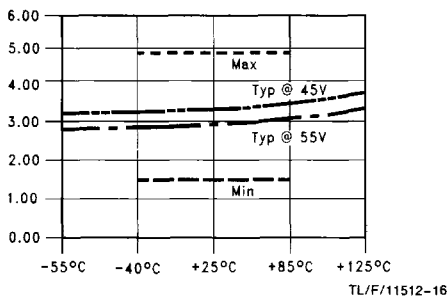
**Note 5:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

## Capacitance

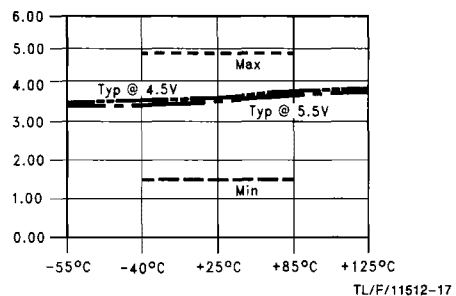
Symbol	Parameter	Typ	Units	Conditions ( $T_A = 25^\circ\text{C}$ )
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$ (non I/O pins)
$C_{I/O}$ (Note 1)	I/O Capacitance	11.0	pF	$V_{CC} = 5.0\text{V}$ ( $A_n, B_n$ )

**Note 1:**  $C_{I/O}$  is measured at frequency,  $f = 1\text{ MHz}$ , per MIL-STD-883D, Method 3012.

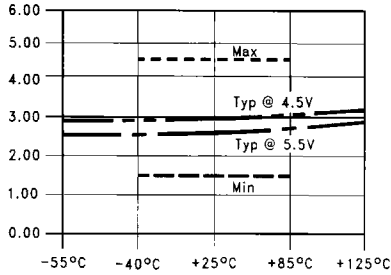
**$t_{PLH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
Clock to Bus



**$t_{PHL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
Clock to Bus

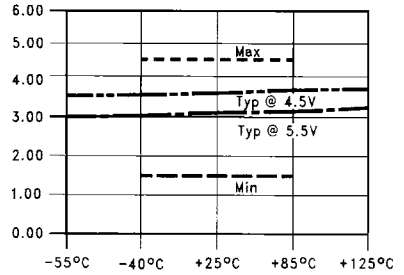


**$t_{PLH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 Bus to Bus



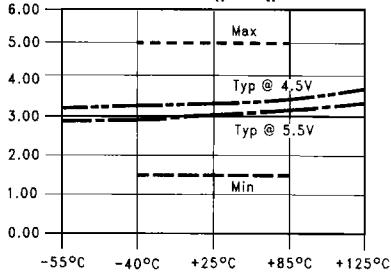
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**$t_{PHL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 Bus to Bus



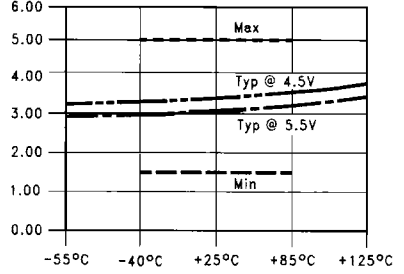
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**$t_{PLH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 SBA or SAB to  $A_n$  or  $B_n$



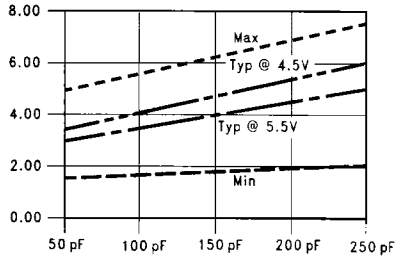
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**$t_{PHL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 SBA or SAB to  $A_n$  or  $B_n$



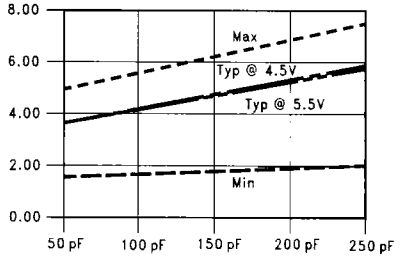
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**$t_{PLH}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



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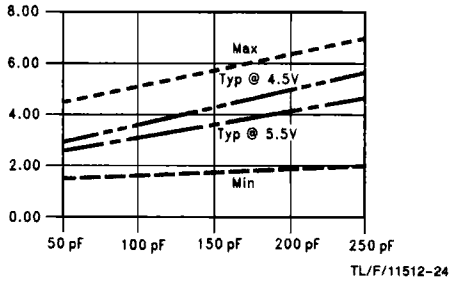
**$t_{PHL}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



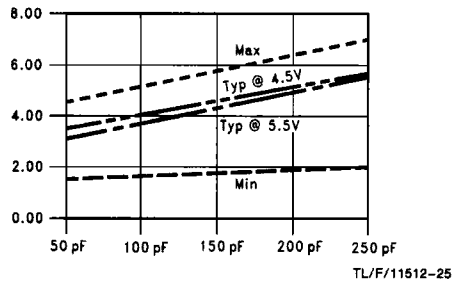
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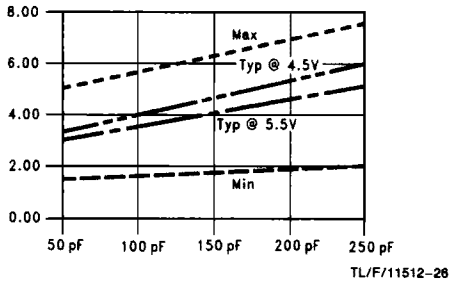
**t<sub>PLH</sub> vs Load Capacitance**  
**1 Output Switching, T<sub>A</sub> = 25°C**  
**Bus to Bus**



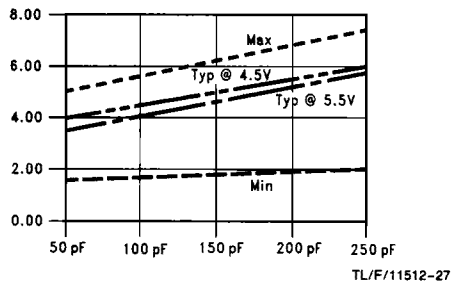
**t<sub>PHL</sub> vs Load Capacitance**  
**1 Output Switching, T<sub>A</sub> = 25°C**  
**Bus to Bus**



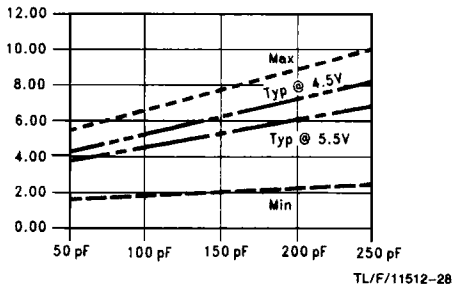
**t<sub>PLH</sub> vs Load Capacitance**  
**1 Output Switching, T<sub>A</sub> = 25°C**  
**SBA or SAB to A<sub>n</sub> or B<sub>n</sub>**



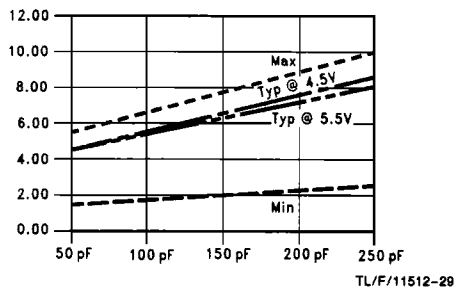
**t<sub>PHL</sub> vs Load Capacitance**  
**1 Output Switching, T<sub>A</sub> = 25°C**  
**SBA or SAB to A<sub>n</sub> or B<sub>n</sub>**



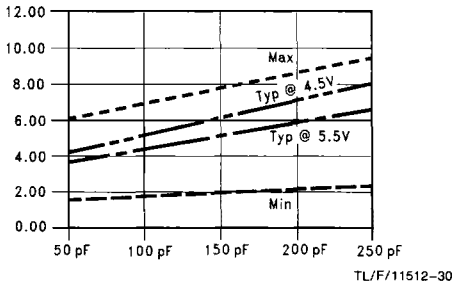
**t<sub>PLH</sub> vs Load Capacitance**  
**8 Outputs Switching, T<sub>A</sub> = 25°C**  
**Clock to Bus**



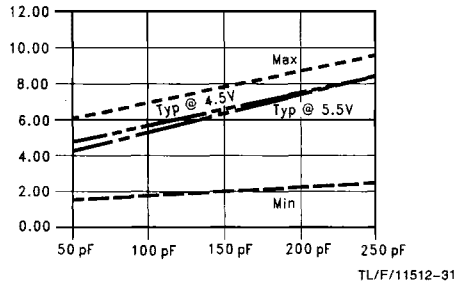
**t<sub>PHL</sub> vs Load Capacitance**  
**8 Outputs Switching, T<sub>A</sub> = 25°C**  
**Clock to Bus**



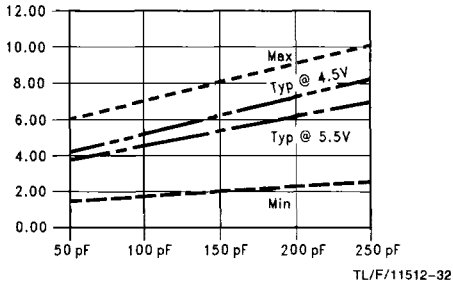
**$t_{PLH}$  vs Load Capacitance**  
**8 Outputs Switching,  $T_A = 25^\circ\text{C}$**   
**Bus to Bus**



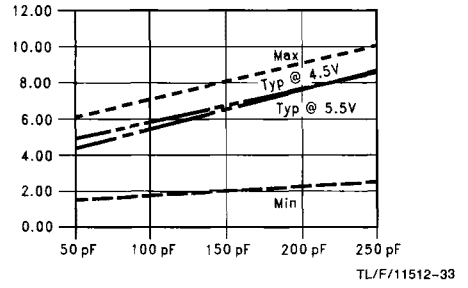
**$t_{PHL}$  vs Load Capacitance**  
**8 Outputs Switching,  $T_A = 25^\circ\text{C}$**   
**Bus to Bus**



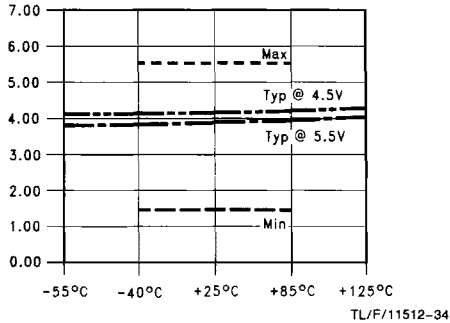
**$t_{PLH}$  vs Load Capacitance**  
**8 Outputs Switching,  $T_A = 25^\circ\text{C}$**   
**SBA or SAB to  $A_n$  or  $B_n$**



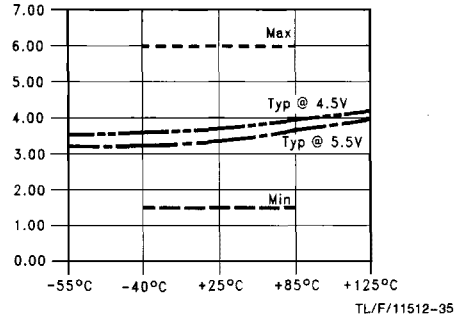
**$t_{PHL}$  vs Load Capacitance**  
**8 Outputs Switching,  $T_A = 25^\circ\text{C}$**   
**SBA or SAB to  $A_n$  or  $B_n$**



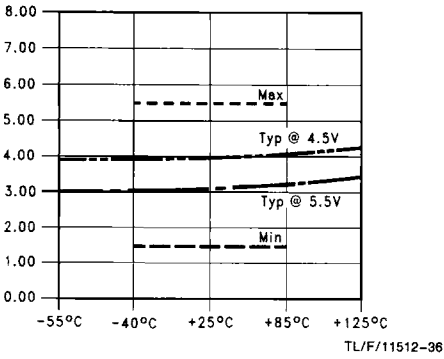
**$t_{pZL}$  vs Temperature ( $T_A$ )**  
 **$C_L = 50$  pF, 1 Output Switching**



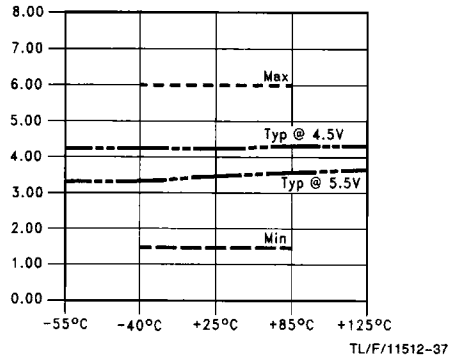
**$t_{pLZ}$  vs Temperature ( $T_A$ )**  
 **$C_L = 50$  pF, 1 Output Switching**



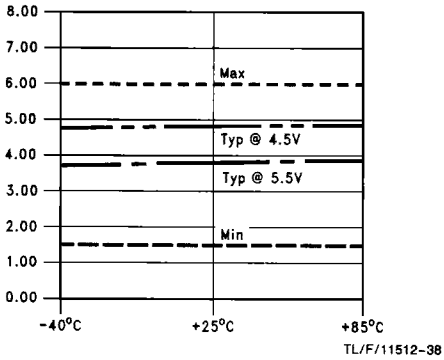
**tpZH vs Temperature (TA)**  
**CL = 50 pF, 1 Output Switching**



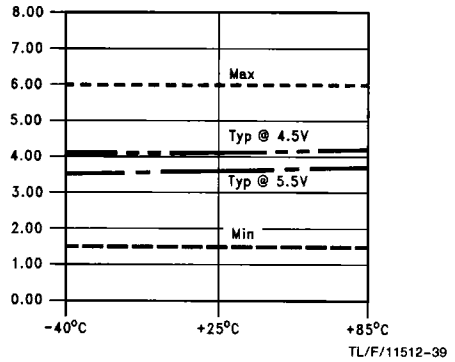
**tpHZ vs Temperature (TA)**  
**CL = 50 pF, 1 Output Switching**



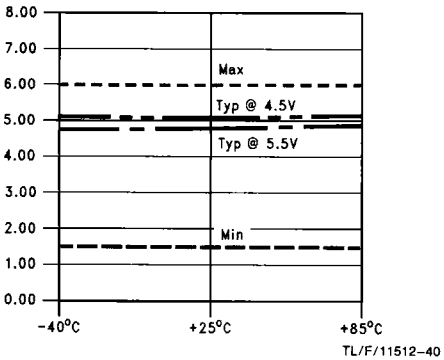
**tpZH vs Temperature (TA)**  
**CL = 50 pF, 8 Outputs Switching**



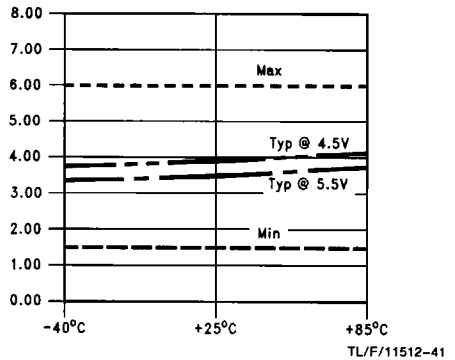
**tpHZ vs Temperature (TA)**  
**CL = 50 pF, 8 Outputs Switching**



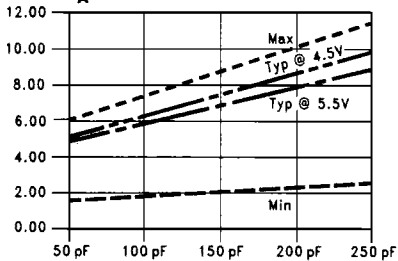
**tpZL vs Temperature (TA)**  
**CL = 50 pF, 8 Outputs Switching**



**tpLZ vs Temperature (TA)**  
**CL = 50 pF, 8 Outputs Switching**

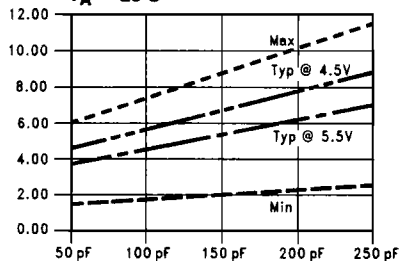


**$t_{pZL}$  vs Load Capacitance**  
**8 Outputs Switching**  
 $T_A = 25^\circ\text{C}$



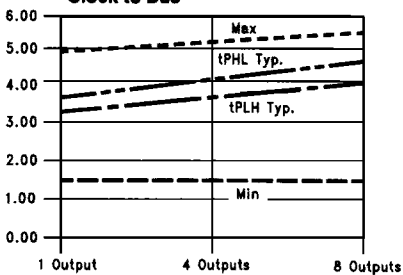
TL/F/11512-42

**$t_{pZH}$  vs Load Capacitance**  
**8 Outputs Switching**  
 $T_A = 25^\circ\text{C}$



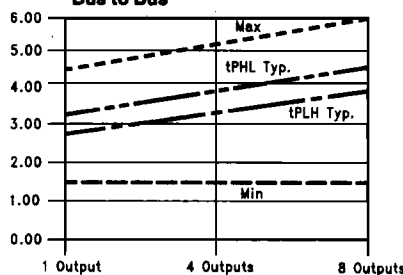
TL/F/11512-43

**$t_{pLH}$  and  $t_{pHL}$  vs Number Output Switching**  
 $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, C_L = 50\text{ pF}$   
**Clock to Bus**



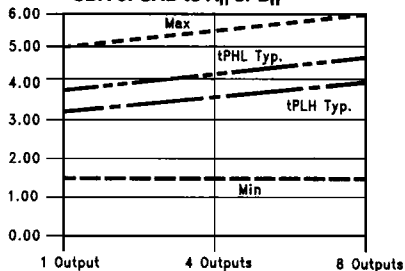
TL/F/11512-44

**$t_{pLH}$  and  $t_{pHL}$  vs Number Output Switching**  
 $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, C_L = 50\text{ pF}$   
**Bus to Bus**



TL/F/11512-45

**$t_{pLH}$  and  $t_{pHL}$  vs Number Output Switching**  
 $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}, C_L = 50\text{ pF}$   
**SBA or SAB to  $A_n$  or  $B_n$**



TL/F/11512-46