256K 3.3V Static RAM
32K x 8-Bit Low Voltage

Features

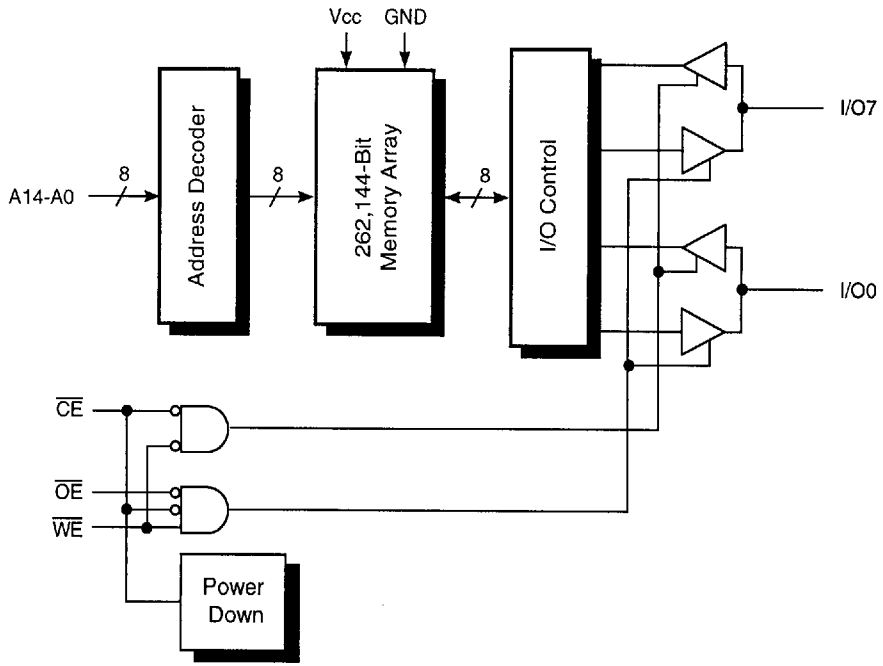
- High speed access times
  Com'l: 12, 15, 20, 25, and 35 ns
- Low power operation
  - PDM31256L
    Active: 350 mW (typ.)
    Standby: 100 mW (typ.)
- Single +3.3V (±0.3%) power supply
- Packages
  Plastic DIP (400 mil) - P
  Plastic SOJ (300 mil) - SO
  Plastic TSOP - T

Description

The PDM31256 is a high-performance CMOS static RAM organized as 32,768 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Device writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are both LOW. The PDM31256 operates from a single +3.3V power supply and all the inputs and outputs are fully TTL compatible.

The PDM31256 is available in a 28-pin 300 mil DIP, 28-pin plastic TSOP, and a 28-pin 300 mil SOJ for surface mount applications.

Functional Block Diagram



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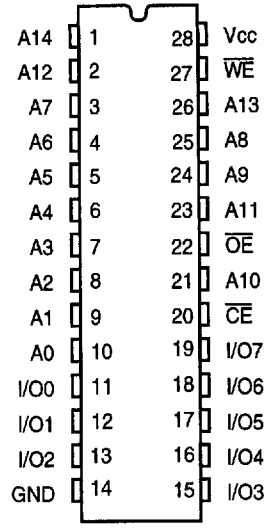
Truth Table

$\overline{OE}$	$\overline{CE1}$	$\overline{WE}$	I/O	MODE
X	H	X	Hi-Z	Standby
L	L	H	Output	Read
H	L	H	Hi-Z	Not Selected
X	L	L	Input	Write

NOTE:1.H = V_{IH}, L = V_{IL}, X = DON'T CARE

Pin Assignment

DIP, SOJ
TSOP



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

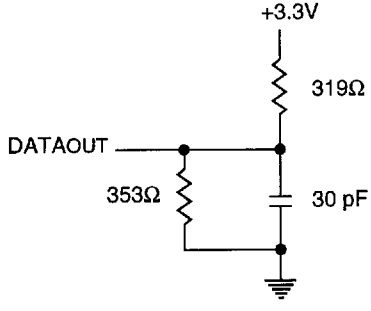


Figure 1. Output Load Equivalent

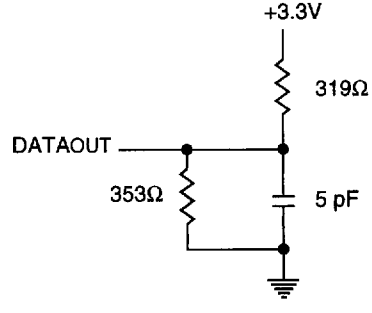


Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE and tHZOE)

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–55 to +135	°C
T_{STG}	Storage Temperature	–55 to +150	°C
T_A	Operating Temperature	0 to +70	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

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Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	6	pF

NOTE 1. This parameter is determined by device characteristics but is not production tested.

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	–1	1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ Output(s) Disabled	–1	1	µA
V_{OL}	Output Low Voltage(1)	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage(1)	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage(1,2)		2.0	5.5	V
V_{IL}	Input Low Voltage(1,2)		–0.3	0.8	V

NOTE 1. All voltages referenced to GND.
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{RC}/2$.
Undershoot: $V_{IL} \ge -2.0V$ for $t \le t_{RC}/2$.
Power-up: $V_{IH} \le +6.0V$ and $V_{CC} \le 3.1V$ for $t \le 200$ msec.

Power Supply Characteristics(1)

Symbol	Parameter	-15	-20	-25	-35	Unit
I_{CC}	Operating Current(2) $\overline{CE} \le V_{IL}$, V_{CC} = Max., f = $f_{MAX} = 1/t_{RC}$, Outputs Open	65	55	50	50	mA
I_{SB1}	Standby Current $\overline{CE} \le V_{IL}$, V_{CC} = Max., f = $f_{MAX} = 1/t_{RC}$, Outputs Open	18	15	12	12	mA
I_{SB2}	Standby Current $\overline{CE} \ge V_{CC} - 0.2V$, V_{CC} = Max., $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le GND + 0.2V$	5	5	5	5	mA

Notes 1. Typical Values are measured at 3.3V, 25°C, and 25 ns cycle time.
2. I_{CC} is dependent on output loading and cycle rates.

AC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, All Temperature Ranges)

Description		-12		-15		-20		-25		-35		
READ Cycle	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
READ Cycle Time	t_{RC}	12		15		20		25		35		ns
Address Access Time	t_{AA}		12		15		20		25		35	ns
Chip Enable Access Time	t_{ACE}		12		15		20		25		35	ns
Output Hold from Address Change	t_{OH}	3		4		4		4		4		ns
Chip Enable to Output in Low-Z(1)	t_{LZCE}	5		4		4		4		4		ns
Chip Disable to Output High-Z(1,2)	t_{HZCE}		10		8		9		9		15	ns
Chip Enable to Power Up Time	t_{PU}	0		0		0		0		0		ns
Chip Enable to Power Down Time	t_{PD}		12		15		20		25		35	ns
Output Enable Access Time	t_{AOE}		6		7		8		8		12	ns
Output Enable to Output in Low-Z	t_{LZOE}	0		0		0		0		0		ns
Output Disable to Output in High-Z(2)	t_{HZOE}		8		6		7		7		10	ns

NOTES: 1. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
2. t_{HZCE}, t_{HZOE}, and t_{HZWE} are specified with CL = 5 pF as in Fig 2. Transition is measured ±200 mV from steady state voltage.

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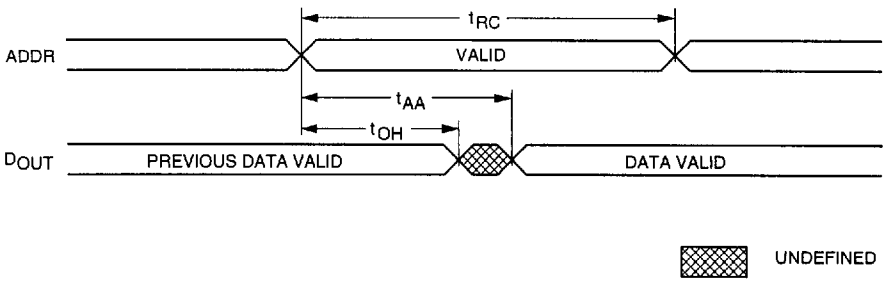
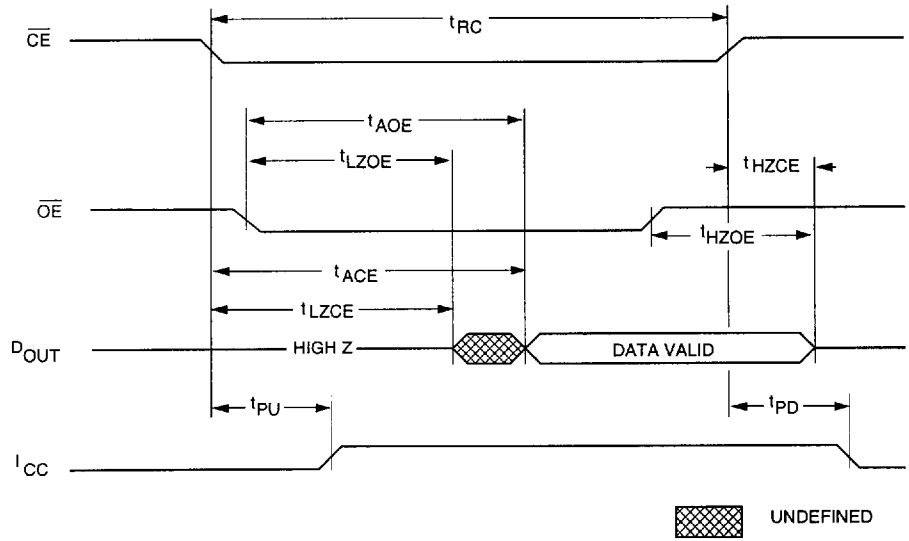
Read Cycle No. 1 (1, 2)



NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected. All chip enables ($\overline{CE}$) and output enables ($\overline{OE}$) are held in their active state.

Read Cycle No. 2 (1, 2, 3, 4)



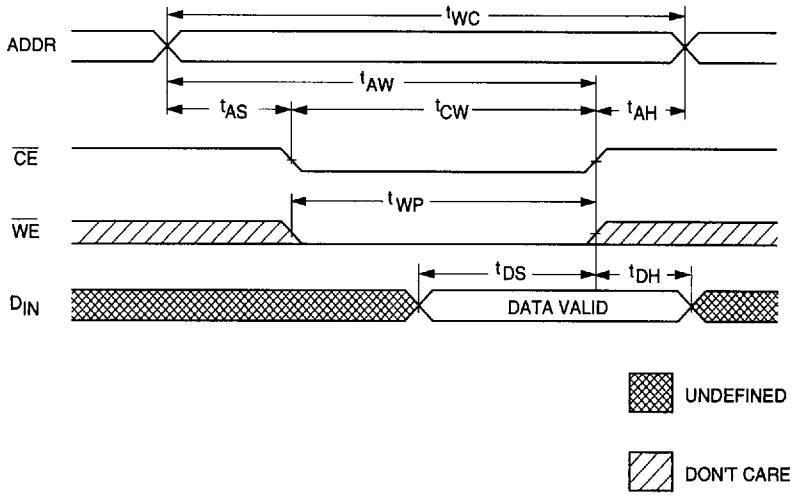
NOTES: 1. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
2. $\overline{WE}$ is High for READ cycle.
3. Address valid prior to, or coincident with, latest occuring chip enable ($\overline{CE}1$).

AC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, All Temperature Ranges)

Description		-12		-15		-20		-25		-35		
WRITE Cycle	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
WRITE Cycle Time	t_{WC}	12		15		20		25		35		ns
Chip Enable to End Write	t_{CW}		12	10		12		15		20		ns
Address Valid to End Write	t_{AW}		12	10		12		15		20		ns
Address Setup Time	t_{AS}	3		0		0		0		0		ns
Address Hold from End of Write	t_{AH}	5		0		0		0		0		ns
Write Pulse Width	t_{WP1}		10	10		12		15		20		ns
Write Pulse Width	t_{WP2}	0		12		15		15		20		ns
Data Setup Time	t_{DS}		12	8		10		10		15		ns
Data Hold Time	t_{DH}		6	0		0		0		0		ns
Write Disable to Output in Low-Z(1)	t_{LZWE}	0		3		3		3		3		ns
Write Enable to Output in High-Z(1,2)	t_{HZWE}		8		7		8		10		12	ns

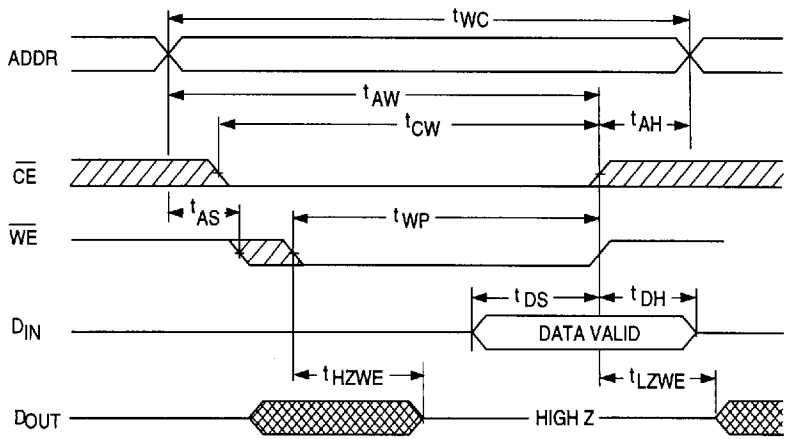
NOTES: 1. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
2. t_{HZCE}, t_{HZOE}, and t_{HZWE} are specified with CL = 5 pF as in Fig 2. Transition is measured ±200 mV from steady state voltage.

Write Cycle No. 1 (Chip Enabled Controlled)[1]



NOTES 1. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.

Write Cycle No. 2 (Write Enable Controlled)[1, 2]



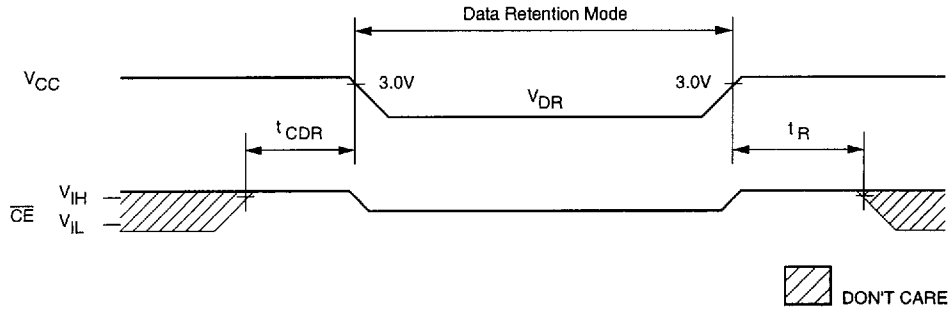
NOTES 1. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
3. Output enable ($\overline{OE}$) is inactive (High).

Data Retention Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retenetion Data		2	—	—	V
I_{CCDR}	Data Retention Current(1)	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq GND + 0.2V$ $V_{CC} = 2V$	—	100	500	µA
t_{CDR}	Chip Deselect to Data Retention Time(2)		0	—	—	ns
t_R	Operation Recovery Time(2,3)		t_{RC}	—	—	ns

NOTES 1. Typical currents are measured at 25°C.
2. This parameter is sampled.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Ordering Information

PDM XXXXX A 999 A A

	Device Type	Power	Speed	Package	Process/ Temperature Range
					Blank Commercial (0° to +70°C)
				P	28-pin 300 mil Plastic DIP
				SO	28-pin 300 mil Plastic SOJ
				T	28-pin Plastic TSOP
			12 15 20 25 35		Speed (ns)
		L			Low Power (3.3V)
	31256				256K (32K x 8) 3.3V Static RAM