HY51V18160C, HY51V16160C

1M x 16bit CMOS DRAM

PRELIMINARY

DESCRIPTION

This family is a 16M bit dynamic RAM organized 1,048,576 x 16-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60,70 or 80ns) and refresh cycle(1K Ref. or 4K Ref.) and package type (SOJ or TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high band-width, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY51V18160CJC	1K		SOJ
HY51V18160CSLJC	1K	SL-part	SOJ
HY51V18160CTC	1K		TSOP-II
HY51V18160CSLTC	1K	SL-part	TSOP-II
HY51V16160CJC	4K		SOJ
HY51V16160CSLJC	4K	SL-part	SOJ
HY51V16160CTC	4K		TSOP-II
HY51V16160CSLTC	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
  - HY51V18160C: 1K Ref.
  - HY51V16160C : 4K Ref.
- Max. Active Power Dissipation

Speed	1K	4K
60	540 mW	324 mW
70	468 mW	288 mW
80	432 mW	252 mW

- Fast access time and cycle time

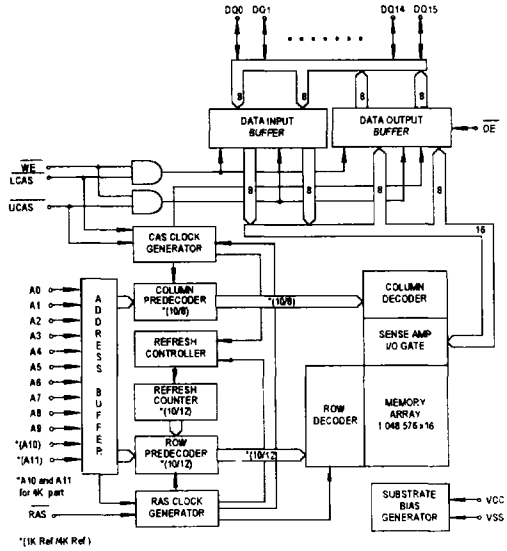
Speed	tRAC	tCAC	tPC
60ns	60ns	15ns	40ns
70ns	70ns	20ns	45ns
80ns	80ns	20ns	50ns

- Fast Page Mode Operation
- Single power supply of 3.3V ± 10%
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

Part No.	Ref.	Normal	SL-part
HY51V18160C	1K	16ms	256ms
HY51V16160C	4K	64ms	

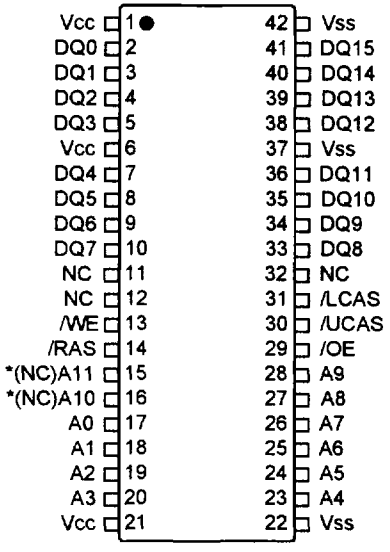
- JEDEC standard pinout
  - 42-pin Plastic SOJ (400 mil)
  - 44/50-pin Plastic TSOP-II (400mil)

BLOCK DIAGRAM

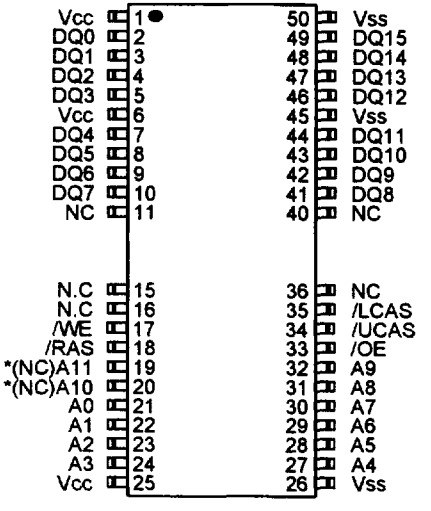


16M

PIN CONFIGURATION (Marking Side)



42-pin Plastic SOJ (400mil)



44/50-pin Plastic TSOP-II (400mil)

*(N.C) : For 1K Refresh product

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs (4K Product)
A0-A9	Address Inputs (1K Product)
DQ0-DQ15	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0℃to 70℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0℃to 70℃, Vcc=3.3V ± 0.3V and Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current 1K Ref	Max. Current 4K Ref	UNIT
I_{CC1}	Operating Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	140 130 120	90 80 70	mA
I_{CC2}	LVTTL Standby Current	/RAS=/CAS ≥ V_{IH} other inputs ≥ Vss	 SL-part	1 1	1 1	mA
I_{CC3}	/RAS-only Refresh Current	/CAS=V_{IH}, /RAS cycling tRC=tRC (min.)	60 70 80	140 130 120	90 80 70	mA
I_{CC4}	Fast Page Mode Current	/RAS=V_{IL}, /CAS, Address cycling tPC=tPC (min.)	60 70 80	90 80 70	80 70 60	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS≥Vcc-0.2V	 SL-part	500 150	500 150	μA μA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	140 130 120	90 80 70	mA
I_{CC7}	Battery Back-up Current (SL-part)	tRC=250μs (1K Ref), 62.5μs (4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE=Vcc - 0.2V Address =Vcc-0.2V or 0.2V DQ0-DQ15=Vcc-0.2V, 0.2V or open	tRAS ≤ 300ns	250	300	μA
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as Icc7		250	250	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I_{LI}	Input Leakage current (Any Input Pin)	Vss ≤ V_{IN} ≤ Vcc + 0.3 All other pins not under test=Vss	-1	1	μA
I_{LO}	Output Leakage current (Any Input Pin)	Vss ≤ V_{OUT} ≤ Vcc /RAS & /CAS at V_{IH}	-1	1	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	2.4	-	V

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(tRC and tPC).
2. Specified values are obtained with outputs unloaded.
3. Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=V_{IH} within one Fast Page mode cycle time tPC.
4. Only /RAS(max.) = 1μs is applied to refresh of battery backup but tRAS(max.) = 10μs is to applied to normal functional operation.
5. Icc5(max.) = 150μA, Icc7 and Icc8 are applied to SL-part only.
6. /CAS means /LCAS or /UCAS cycle.

AC CHARACTERISTICS

(T_A=0℃ to 70℃, Vcc=3.3V ± 0.3V and Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51V18160C / HY51V16160C						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	150	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	105	-	ns	
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	4,5,6
6	tCAC	Access Time from /CAS	-	15	-	20	-	20	ns	4,5
7	tAA	Access Time from Column Address	-	30	-	40	-	45	ns	4,6
8	tCPA	Access Time from Column Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Out Buffer Turn-Off Delay Time from /CAS	0	15	0	20	0	20	ns	7
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	2
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	/RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	/CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	/CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	/RAS to /CAS Delay Time	20	45	20	50	20	60	ns	5
19	tRAD	/RAS to Column Address Delay Time	15	30	15	35	15	40	ns	6
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	10
21	tCP	/CAS Precharge Time	10	-	10	-	10	-	ns	14
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	8
29	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	8
30	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	
31	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
32	tRWL	Write Command to /RAS Lead Time	15	-	20	-	20	-	ns	
33	tCWL	Write Command to /CAS Lead Time	15	-	20	-	20	-	ns	14
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	9
35	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	9

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY51V18160C / HY51V16160C						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (1024 cycles)	16	-	16	-	16	-	ms	
		Refresh Period (4096 cycles)	64	-	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	10
38	tCWD	/CAS to /WE Delay Time	35	-	40	-	45	-	ns	10,13
39	tRWD	/RAS to /WE Delay Time	80	-	95	-	105	-	ns	10
40	tAWD	Column Address to /WE Delay Time	55	-	60	-	65	-	ns	10
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	15
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	16
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	9
44	tCPT	/CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	12
45	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
46	tOEA	/OE Access Time	-	15	-	20	-	20	ns	
47	tOED	/OE to Data Delay Time	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	0	15	0	20	0	20	ns	7
49	tOEH	/OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	60	-	70	-	80	-	ns	10
51	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	45	-	ns	
52	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	/RAS Precharge Time (Self Refresh)	90	-	90	-	90	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70℃) is assured.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 1 TTL loads and 100pF.
5. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
7. tOFF(max.) and tOEZ(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referred to /LCAS or /UCAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
10. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD≥tCWD(min.), tRWD≥tRWD(min.) and tCPWD≥tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
11. tASC and tCAH are referred to the earlier /CAS falling edge.
12. tCP and tCPT are measured when both /LCAS and /UCAS are high state.
13. tCWD is referred to the later /CAS falling edge at Read-Modify-Write cycle.
14. tCWL must be satisfied by both /LCAS and /UCAS for 16-bit access cycles.
15. tCSR is referred to the earlier /CAS falling low before /RAS transition low.
16. tCHR is referred to the later /CAS rising high after /RAS transition low.
17. tDS, tDH is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).

CAPACITANCE

(T_A=25℃, Vcc=3.3V ± 0.3V, Vss=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A11)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /LCAS,/UCAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input /Output Capacitance (DQ0 - DQ15)	-	7	pF