bq4011/bq4011Y

32Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4011 is a nonvolatile 262,144-bit static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

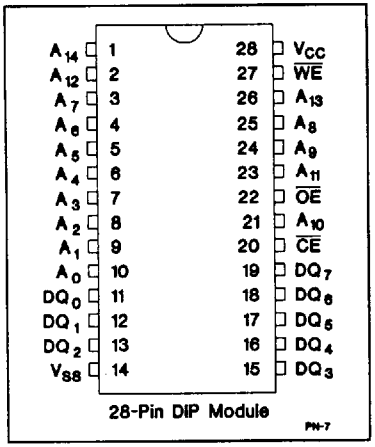
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4011 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

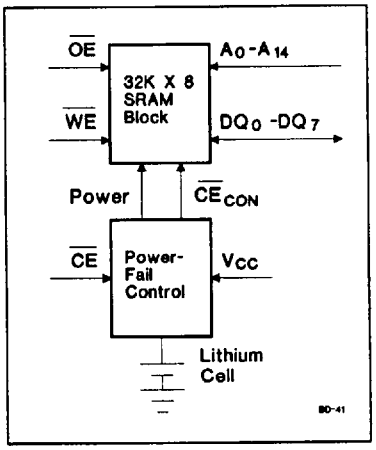
Pin Connections



Pin Names

A_0 -A_{14}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
			bq4011Y-70	70	-10%
bq4011 -100	100	-5%	bq4011Y -100	100	-10%
bq4011 -150	150	-5%	bq4011Y -150	150	-10%
bq4011 -200	200	-5%	bq4011Y -200	200	-10%

Functional Description

When power is valid, the bq4011 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4011 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4011Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4011Y/bq4011Y-xxxN
		4.75	5.0	5.5	V	bq4011
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4011
		4.30	4.37	4.50	V	bq4011Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

5

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

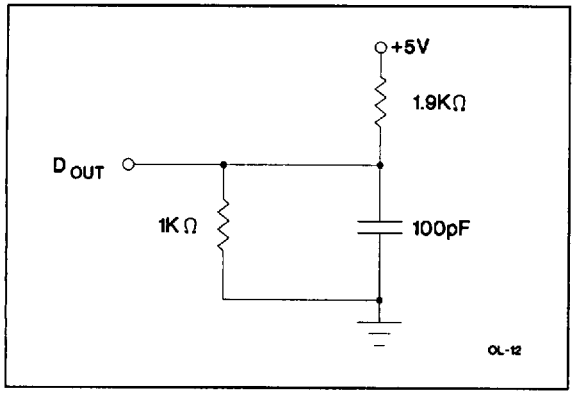


Figure 1. Output Load A

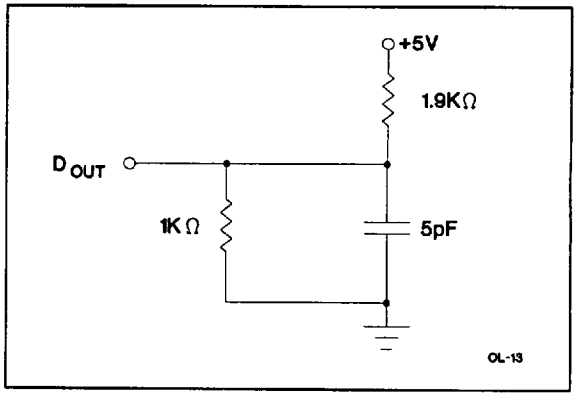
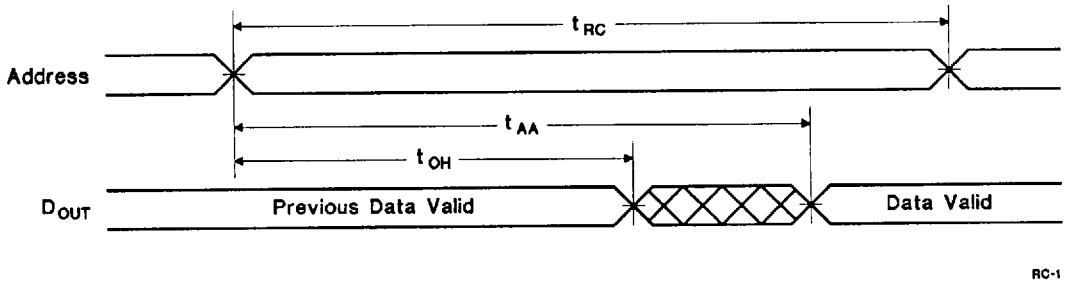


Figure 2. Output Load B

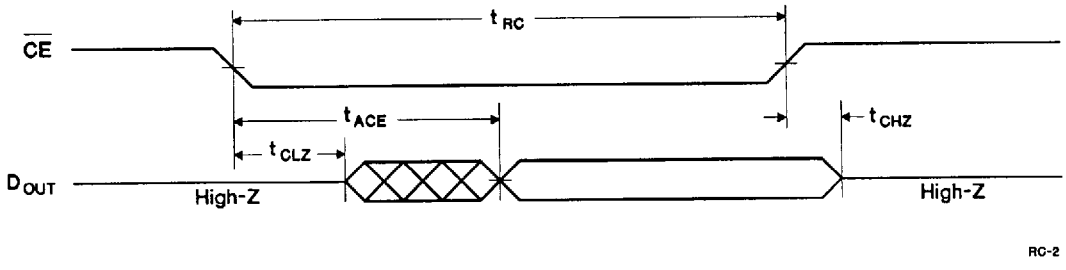
Read Cycle (T_A = TOPR, V_{CC}min ≤ V_{CC} ≤ V_{CC}max)

Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	100	-	150	-	200	-	ns	
t_{AA}	Address access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	50	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	10	-	ns	Output load A

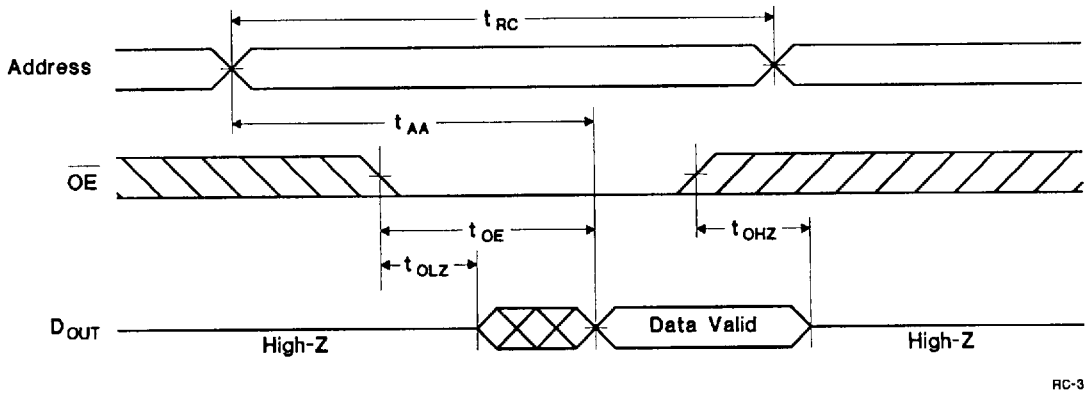
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

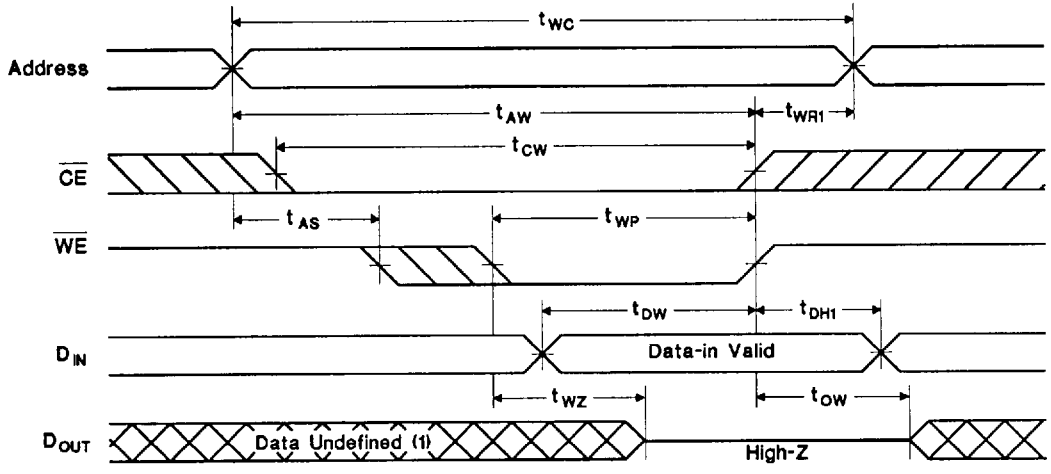
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	100	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	55	-	90	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	55	-	80	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	40	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle.(4)
t_{WZ}	Write enabled to output in high Z	0	25	0	35	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

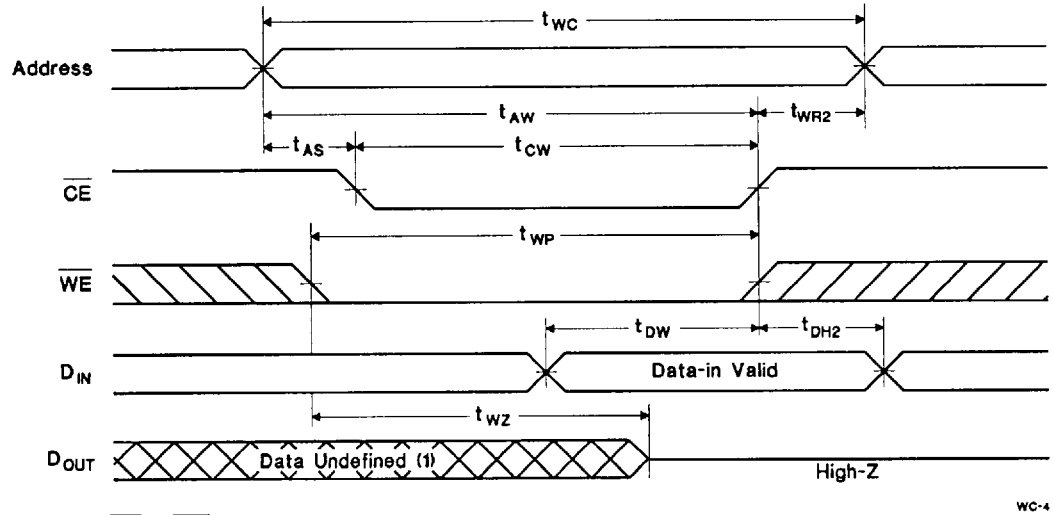
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

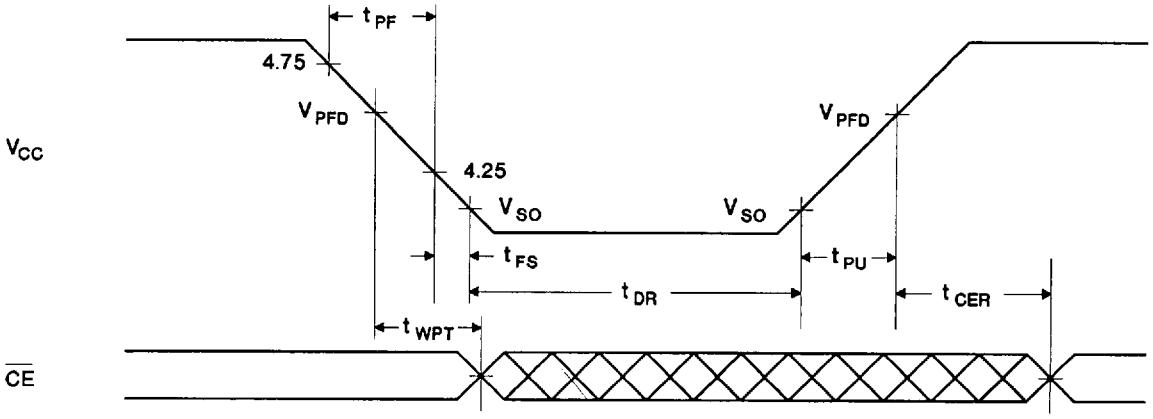
Power-Down/Power-Up Cycle (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	TA = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6	-	-	years	T_A = 25°C (2); industrial temperature range (-N) only.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



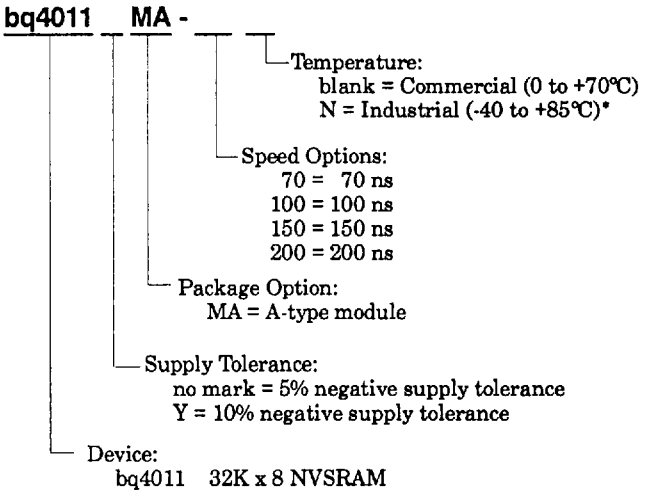
PD-8

Data Sheet Revision History

Change No.	Page No.	Description
1	5-12, 5-13, 5-14, 5-16, 5-18, 5-19	Added industrial temperature range for bq4011YMA-150N.
2	5-11, 5-14, 5-16, 5-19	Added 70 ns speed grade for bq4011-70 and bq4011Y-70 and added industrial temperature range for bq4011YMA-70N.

Notes: Change 1 = Sept 1992 B changes from Sept. 1990 A.
Change 2 = Aug. 1993 C changes from Sept. 1991 B.

Ordering Information



***Note:** Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

5