

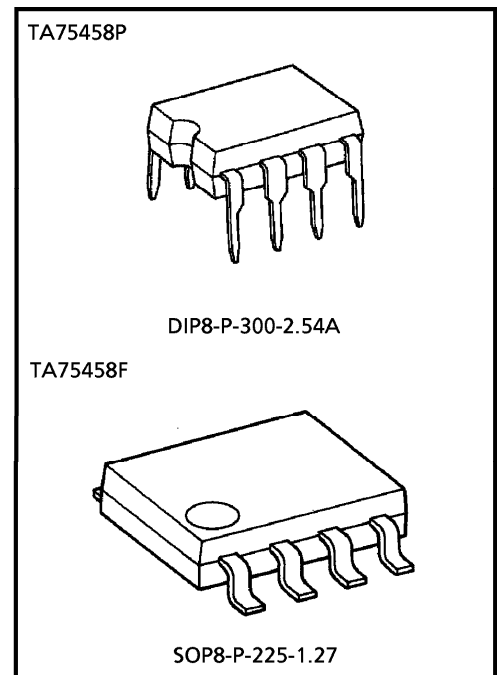
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

# TA75458P, TA75458F

## DUAL OPERATIONAL AMPLIFIER

### FEATURES

- Pair of Internally Compensated High Performance Amplifier
- No Frequency Compensation Required
- No Latch-up
- Short Circuit Protection
- Side Common Mode and Differential Voltage Range
- Low Power Consumption

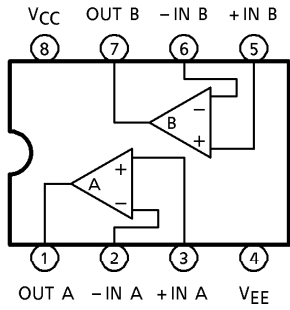


### Weight

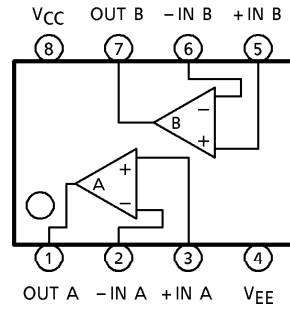
DIP8-P-300-2.54A : 0.5g (Typ.)  
SOP8-P-225-1.27 : 0.1g (Typ.)

**PIN CONNECTION (TOP VIEW)**

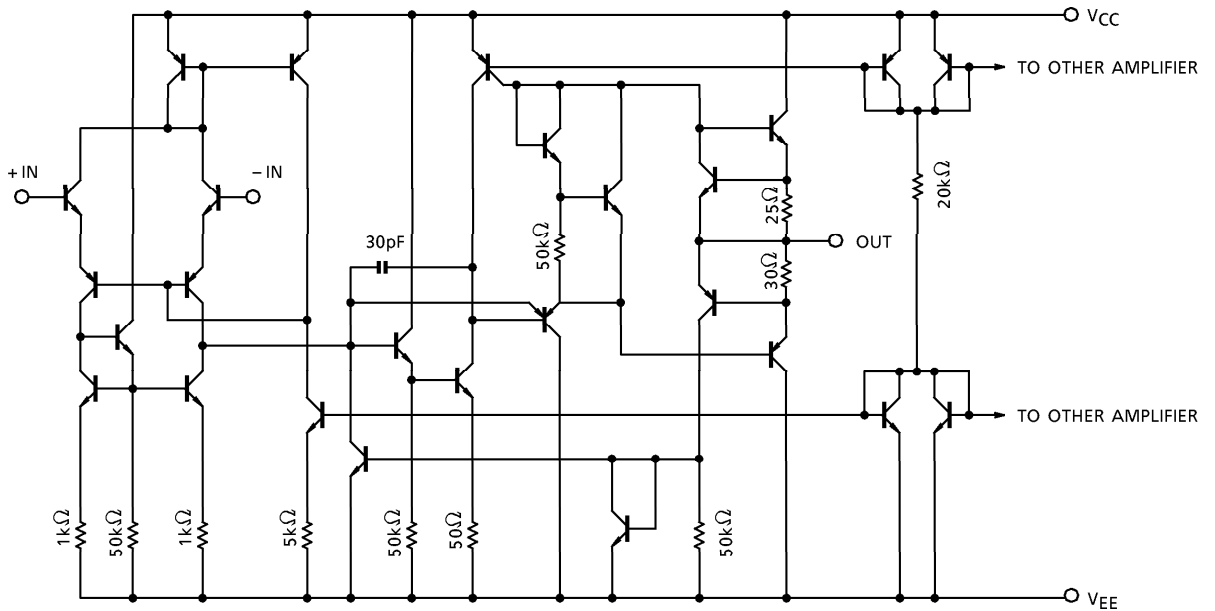
TA75458P



TA75458F



**EQUIVALENT CIRCUIT**



## MAXIMUM RATINGS (Ta = 25°C)

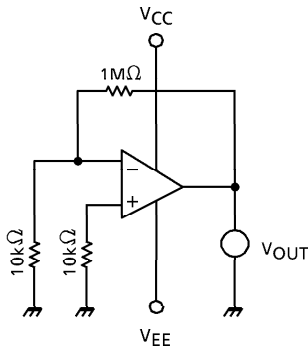
| CHARACTERISTIC             | SYMBOL                            | TA75458P                         | TA75458F                         | UNIT |
|----------------------------|-----------------------------------|----------------------------------|----------------------------------|------|
| Supply Voltage             | V <sub>CC</sub> , V <sub>EE</sub> | + 18, - 18                       | + 18, - 18                       | V    |
| Differential Input Voltage | DV <sub>IN</sub>                  | ± 30                             | ± 30                             | V    |
| Input Voltage              | V <sub>IN</sub>                   | V <sub>CC</sub> ~V <sub>EE</sub> | V <sub>CC</sub> ~V <sub>EE</sub> | V    |
| Power Dissipation          | P <sub>D</sub>                    | 500                              | 240                              | mW   |
| Operating Temperature      | T <sub>opr</sub>                  | - 40~85                          | - 30~75                          | °C   |
| Ambient Temperature        | T <sub>stg</sub>                  | - 55~125                         | - 55~125                         | °C   |

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 15V, V<sub>EE</sub> = - 15V, Ta = 25°C)

| CHARACTERISTIC                           |                            | SYMBOL                            | TEST CIRCUIT | TEST CONDITION  | MIN. | TYP. | MAX. | UNIT  |
|--|----------------------------|-----------------------------------|--------------|---|------|------|------|-------|
| Input Offset Voltage                     |                            | V <sub>IO</sub>                   | 1            | R <sub>g</sub> ≤ 10kΩ   | —    | 1    | 5    | mV    |
| Input Offset Current                     |                            | I <sub>IO</sub>                   | 2            |   | —    | 20   | 200  | nA    |
| Input Bias Current                       |                            | I <sub>I</sub>                    | 2            |   | —    | 80   | 500  | nA    |
| Common Mode Input Voltage                |                            | CMV <sub>IN</sub>                 | 3            |   | ± 12 | ± 13 | —    | V     |
| Maximum Output Voltage                   |                            | V <sub>OM</sub>                   | 4            | R <sub>L</sub> = 10kΩ   | ± 12 | ± 14 | —    | V     |
|  |                            | V <sub>OMR</sub>                  | 4            | R <sub>L</sub> = 2kΩ  | ± 10 | ± 13 | —    |       |
| Source Current                           |                            | I <sub>source</sub>               | 4            |   | —    | 20   | —    | mA    |
| Sink Current                             |                            | I <sub>sink</sub>                 | 4            |   | —    | 20   | —    | mA    |
| Differential Input Impedance             | Parallel Input Resistance  | Z <sub>Di</sub>                   | —            | f = 20Hz Open Loop  | 0.3  | 1.0  | —    | MΩ    |
|  | Parallel Input Capacitance | C <sub>i</sub>                    | —            |   | —    | 6.0  | —    | pF    |
| Output Impedance                         |                            | Z <sub>o</sub>                    | —            | f = 20Hz  | —    | 75   | —    | Ω     |
| Voltage Gain (Open Loop)                 |                            | G <sub>V</sub>                    | 7            | V <sub>OUT</sub> = ± 10V, R <sub>L</sub> = 2kΩ                                    | 86   | 100  | —    | dB    |
| Common Mode Input Signal Rejection Ratio |                            | CMRR                              | 3            | f = 100Hz   | 70   | 90   | —    | dB    |
| Supply Voltage Rejection Ratio           |                            | SVRR                              | 1            | R <sub>g</sub> ≤ 10kΩ   | —    | 30   | 150  | μV/V  |
| Power Bandwidth                          |                            | f <sub>W</sub>                    | —            | G <sub>V</sub> = 1, R <sub>L</sub> = 2kΩ<br>V <sub>OUT</sub> = 20V <sub>p-p</sub> | —    | 14   | —    | kHz   |
| Slew Rate                                |                            | SR                                | 6            | G <sub>V</sub> = 1, R <sub>L</sub> = 2kΩ  | —    | 0.8  | —    | V/μs  |
| Unity Gain Cross Frequency               |                            | f <sub>T</sub>                    | 7            | Open Loop   | —    | 1.1  | —    | MHz   |
| Power Dissipation                        |                            | P <sub>D</sub>                    | 5            | V <sub>O</sub> = 0V   | —    | 70   | 170  | mW    |
| Input Offset Voltage Drift               |                            | ΔV <sub>IO</sub> /ΔT              | 1            | R <sub>g</sub> ≤ 10kΩ, Ta = - 30~75°C   | —    | —    | 50   | μV/°C |
| Supply Current                           |                            | I <sub>CC</sub> , I <sub>EE</sub> | 5            |   | —    | 2.3  | 5.6  | mA    |

TEST CIRCUIT

(1)  $V_{IO}$ ,  $\Delta V_{IO} / \Delta T$ , SVRR



$$V_{IO} = V_{OUT} / 100 \text{ (V)}$$

$$\Delta V_{IO} / \Delta T = \{V_{IO} (25^\circ\text{C}) - V_{IO} (-30^\circ\text{C})\} / 55 \text{ (V/}^\circ\text{C)}$$

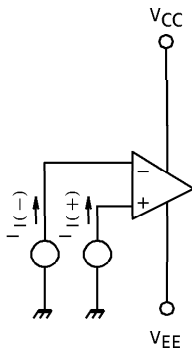
$$\Delta V_{IO} / \Delta T = \{V_{IO} (75^\circ\text{C}) - V_{IO} (25^\circ\text{C})\} / 50 \text{ (V/}^\circ\text{C)}$$

$$SVRR = (V_{IO1} - V_{IO2}) / 5 \text{ (}\mu\text{V/V)}$$

$V_{IO1}$  :  $V_{CC}$ , AT  $V_{EE} = \pm 17.5\text{V}$

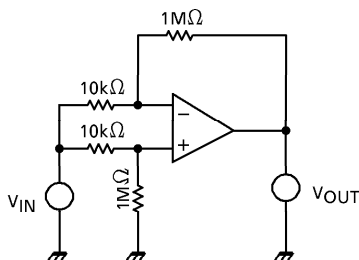
$V_{IO2}$  :  $V_{CC}$ , At  $V_{EE} = \pm 12.5\text{V}$

(2)  $I_I$ ,  $I_{IO}$



$$I_{IO} = |I_i(+)-I_i(-)|$$

(3)  $CMV_{IN}$ , CMRR



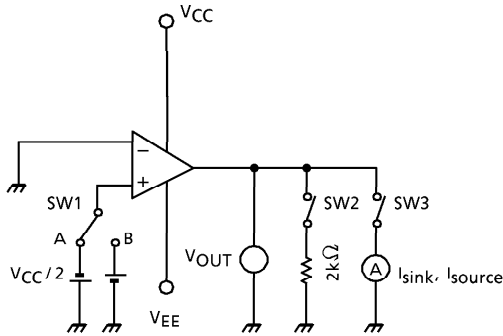
$CMV_{IN}$  :  $V_{OUT} = \pm 1\text{V (DC)}$

$V_{IN} = \text{MEASURE}$

CMRR : RATIO OF  $G_{diff}$  vs  $G_{CM}$

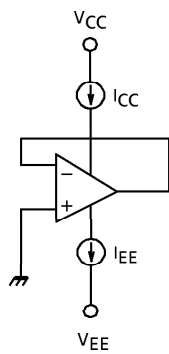
$$CMRR = 20 \log \frac{G_{diff}}{G_{CM}} \text{ (dB)}$$

(4)  $V_{OM}$ ,  $V_{OMR}$ ,  $I_{sink}$ ,  $I_{source}$



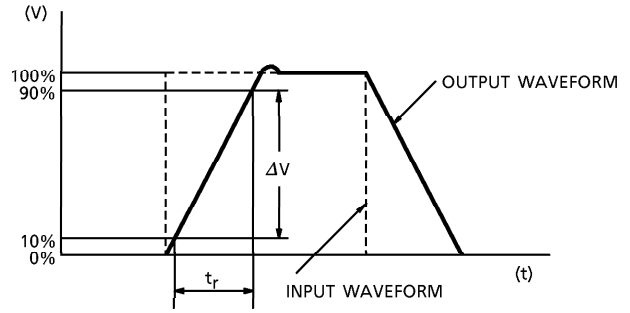
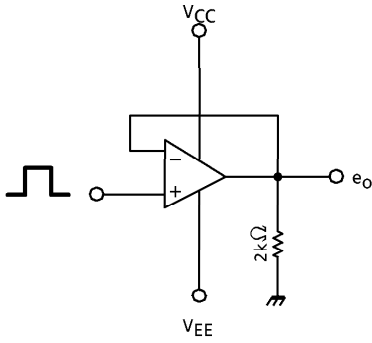
- $V_{OM}(+)$  : SW1 IS SIDE B, SW2 OFF, SW3 OFF
- $V_{OM}(-)$  : SW1 IS SIDE A, SW2 OFF, SW3 OFF
- $V_{OMR}(+)$  : SW1 IS SIDE B, SW2 ON, SW3 OFF
- $V_{OMR}(-)$  : SW1 IS SIDE A, SW2 ON, SW3 OFF
- $I_{sink}$  : SW1 IS SIDE A, SW2 OFF, SW3 ON
- $I_{source}$  : SW1 IS SIDE B, SW2 OFF, SW3 ON

(5)  $I_{CC}$ ,  $I_{EE}$ ,  $P_D$

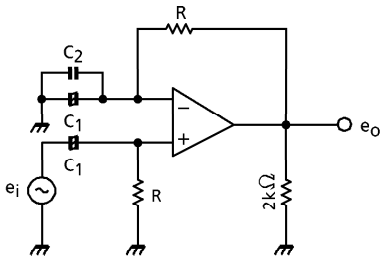


$$P_D = V_{CC} \cdot I_{CC} + V_{EE} \cdot I_{EE} \text{ (W)}$$

(6) SR



(7)  $G_V, f_T$



$G_V$

$$R \gg 1 / \omega C_1$$

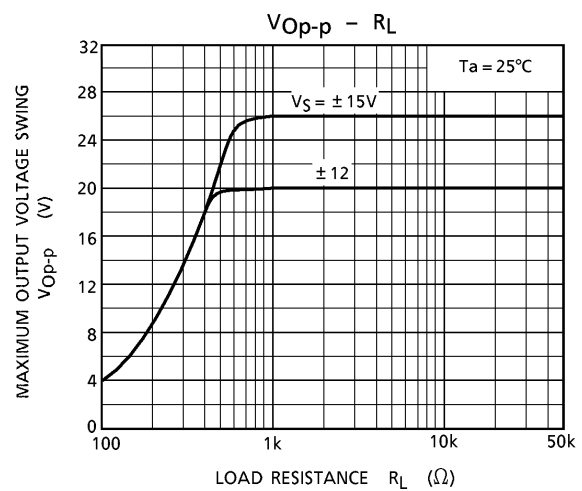
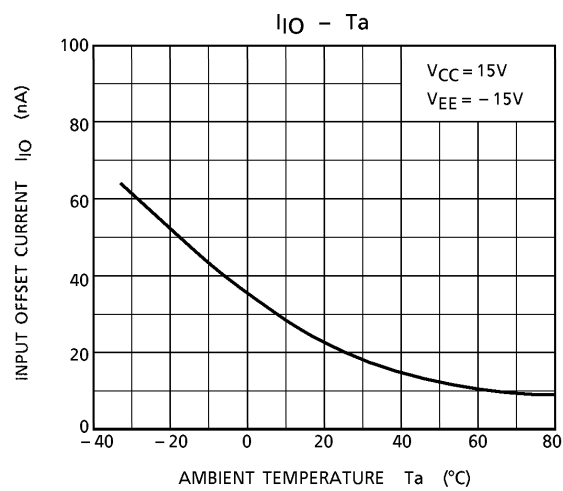
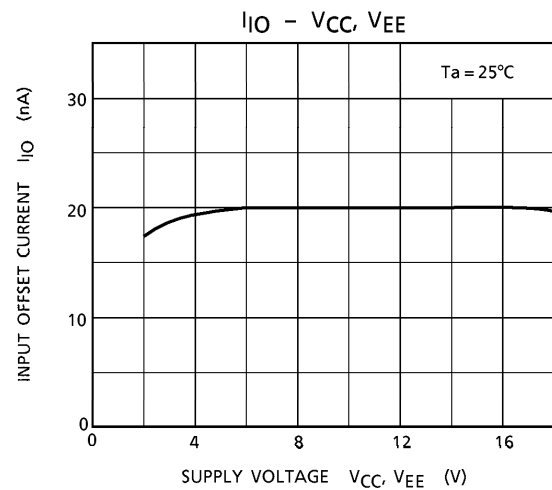
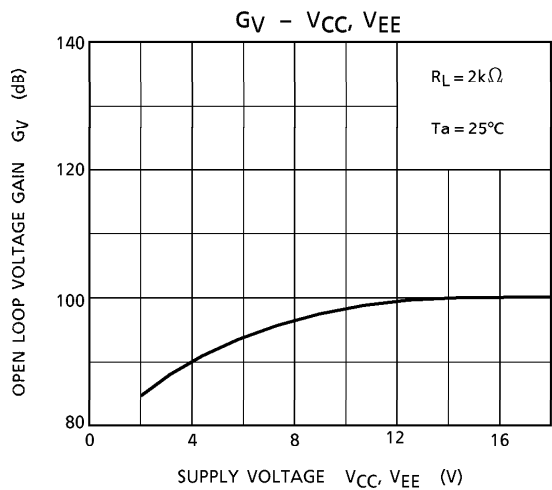
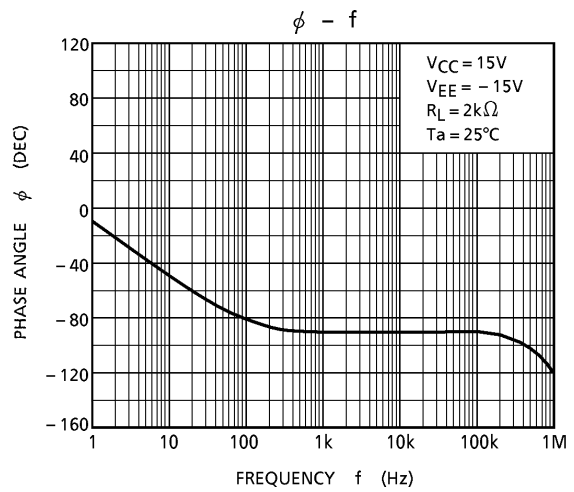
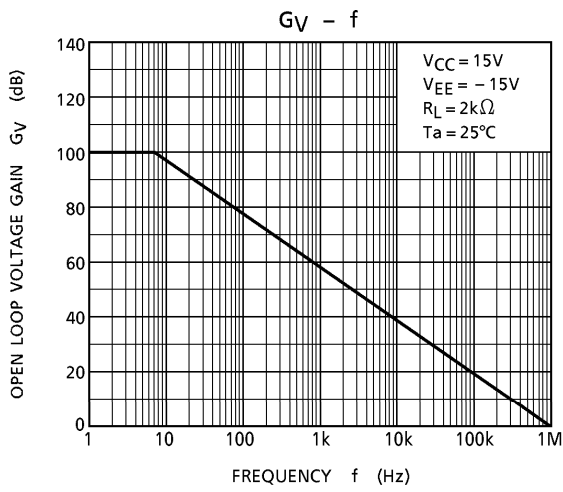
$C_1$  : COUPLING CONDENSER

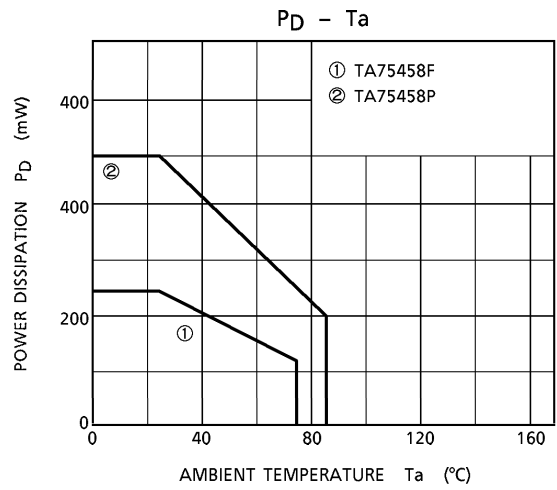
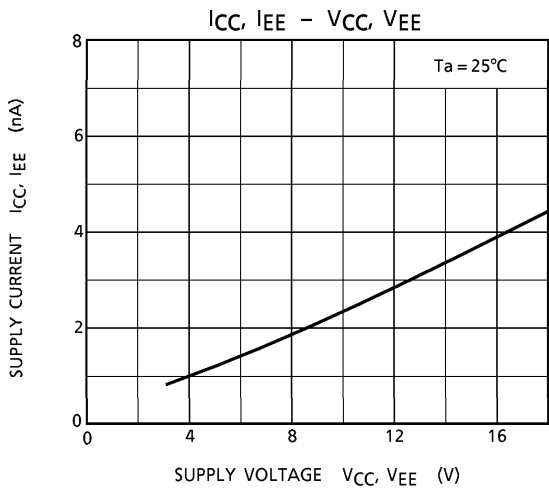
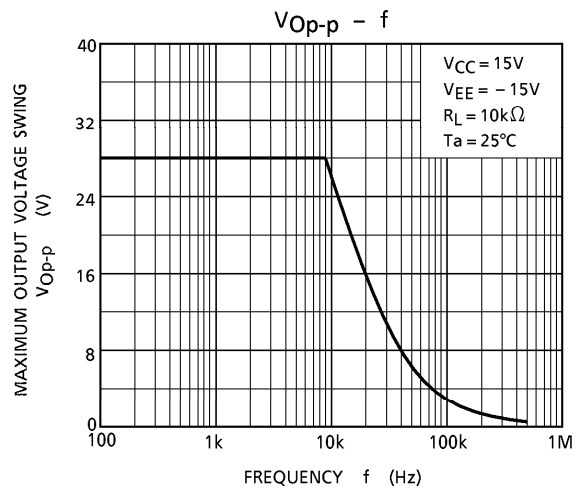
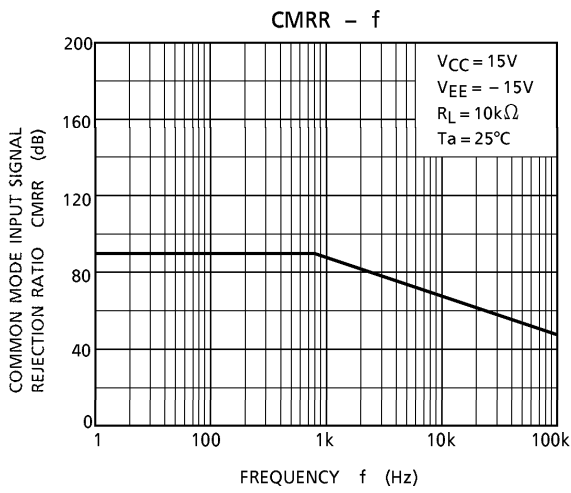
$C_2$  : HIGH FREQUENCY BYPASS CONDENSER  
0.1  $\mu$ F

$$G_V = 20 \log e_o / e_i \text{ (dB)}$$

$f_T$  INPUT FREQUENCY AT  $e_i = e_o$

CHARACTERISTICS

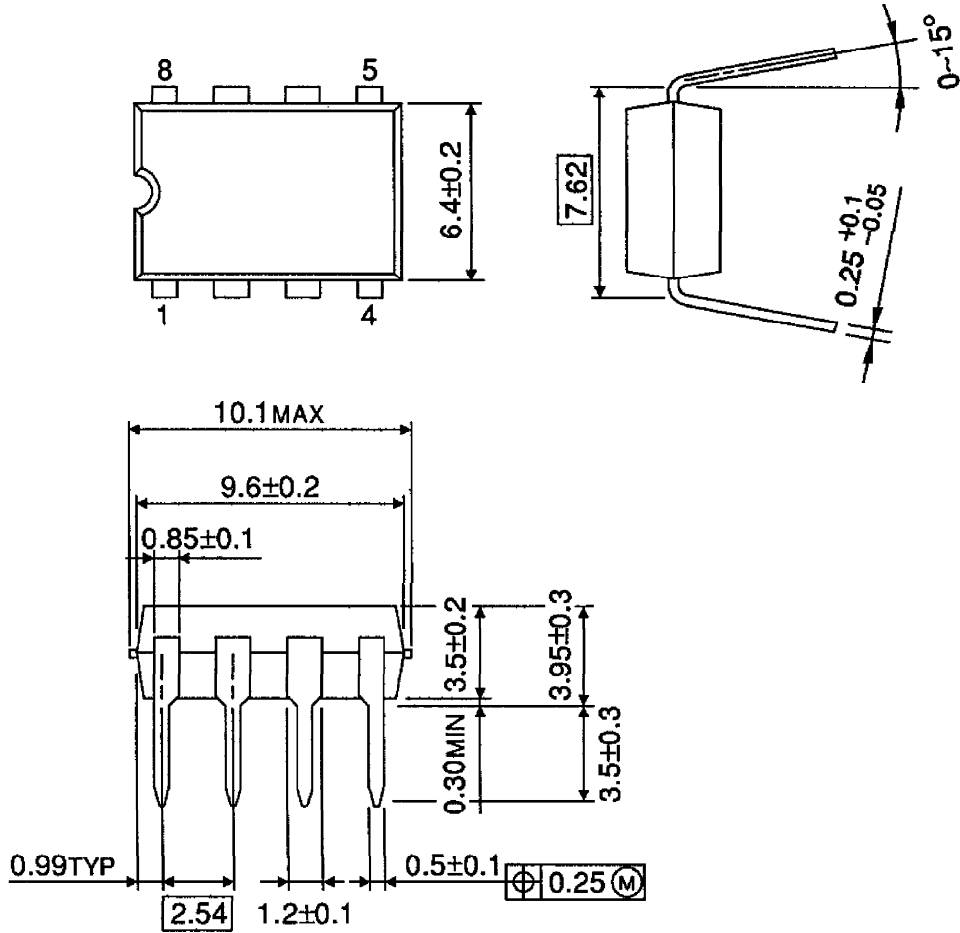






**PACKAGE DIMENSIONS**  
DIP8-P-300-2.54A

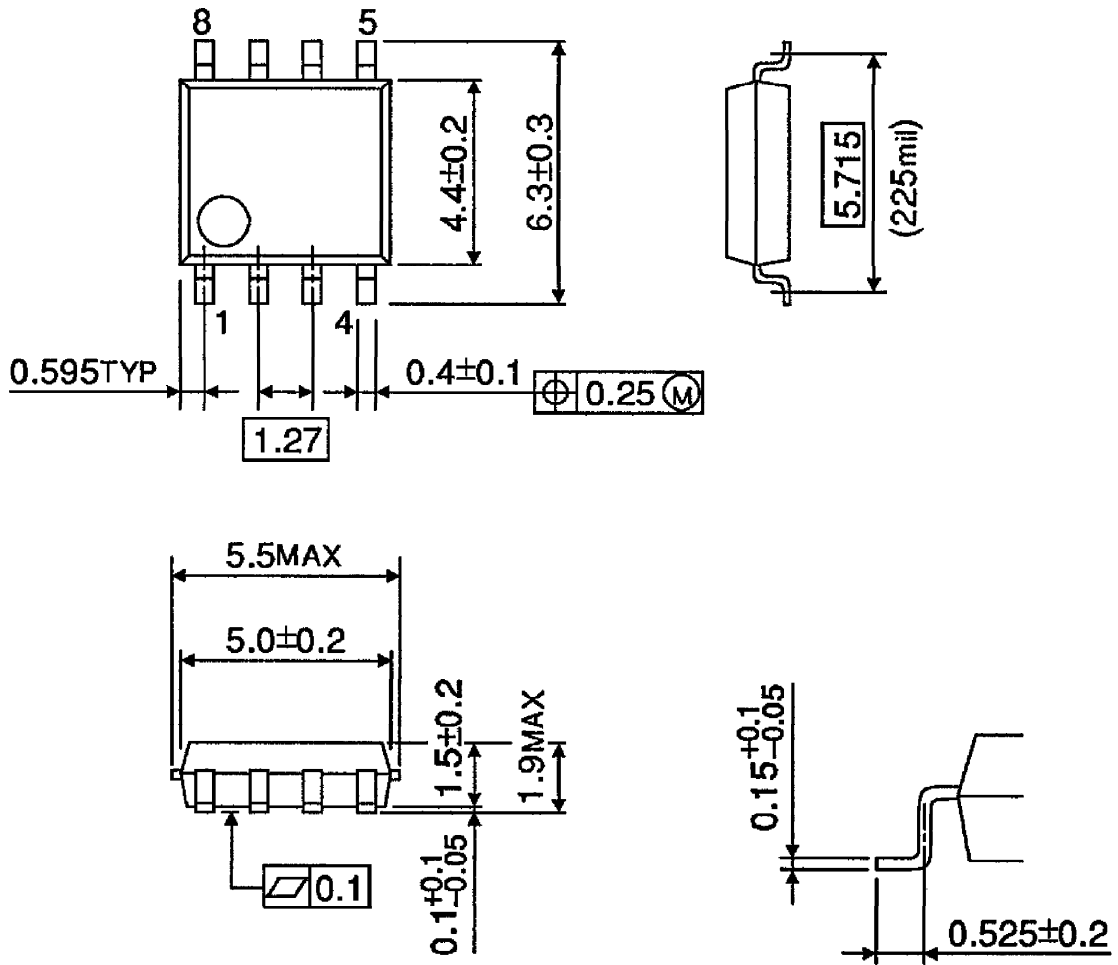
Unit : mm



Weight : 0.5g (Typ.)

PACKAGE DIMENSIONS  
SOP8-P-225-1.27

Unit : mm



Weight : 0.1g (Typ.)

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000707EBA

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