

December 1992

## CMOS Hex 'D'-Type Flip-Flop

### Features

- High Voltage Type (20V Rating)
- 5V, 10V and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1 $\mu$ A at 18V Over Full Package Temperature Range, 100nA at 18V and +25°C
- Noise Margin (Over full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

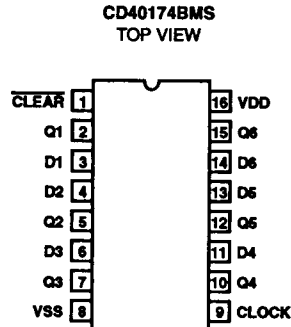
### Description

CD40174BMS consists of six identical 'D'-Type flip-flops having independent DATA inputs. The CLOCK and CLEAR inputs are common to all six units. Data is transferred to the Q outputs on the positive going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the CLEAR input.

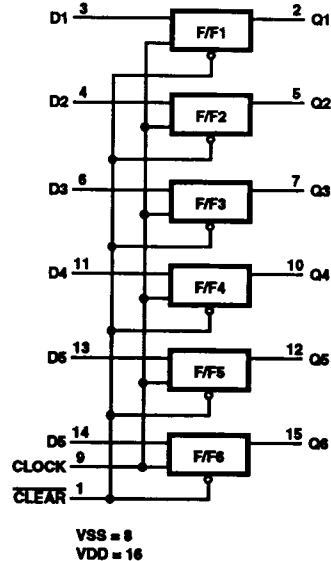
The CD40174BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

### Pinout



### Functional Diagram



# Specifications CD40174BMS

## Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . .	-0.5V to +20V (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . .	-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . .	±10mA
Operating Temperature Range . . . . .	-55°C to +125°C Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . .	-65°C to +150°C
Lead Temperature (During Soldering) . . . . .	+265°C At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

## Reliability Information

Thermal Resistance . . . . .	$\theta_{JA}$	$\theta_{JC}$
Ceramic DIP and FRIT Package . . . . .	80°C/W	20°C/W
Flatpack Package . . . . .	70°C/W	20°C/W
Maximum Package Power Dissipation (PD) at +125°C		
For TA = -55°C to +100°C (Package Type D, F, K) . . . . .	500mW	
For TA = +100°C to +125°C (Package Type D, F, K) . . . . .	Derate	
Linearity at 12mW/°C to 200mW		
Device Dissipation per Output Transistor . . . . .	100mW	
For TA = Full Package Temperature Range (All Package Types)		
Junction Temperature . . . . .	+175°C	

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
			VDD = 18V	2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
			VDD = 18V	2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

- NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
2. Go/No Go test with limits applied to inputs.

7  
LOGIC

## Specifications CD40174BMS

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay CLEAR to Output	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	3.5/1.35	-	MHz

**NOTES:**

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	μA
				+125°C	-	30	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	60	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	120	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5B	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

# Specifications CD40174BMS

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH15	VDD = 15V, VO <sub>UT</sub> = 13.5V	1, 2	+25°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VO <sub>H</sub> > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VO <sub>H</sub> > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay CLEAR to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	40	ns
		VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	80	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	130	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	15	-	μs
		VDD = 10V	1, 2, 3, 4	+25°C	15	-	μs
		VDD = 15V	1, 2, 3, 4	+25°C	15	-	μs
Minimum CLEAR Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum CLEAR Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	CLEAR	1, 2	+25°C	-	40	pF
		All others	1, 2	+25°C	-	7.5	pF

**NOTES:**

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

**7**  
LOGIC

# Specifications CD40174BMS

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.

3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

**TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	1, 7, 9	
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

# Specifications CD40174BMS

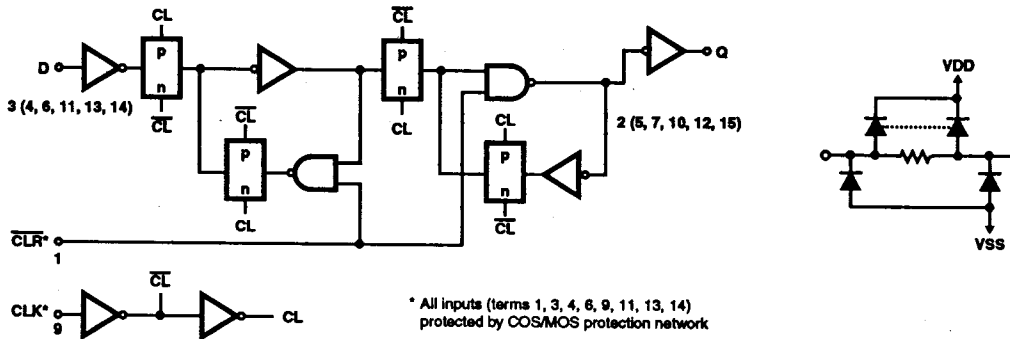
**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 5, 7, 10, 12, 15	1, 3, 4, 6, 8, 9, 11, 13, 14	16			
Static Burn-In 2 (Note 1)	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16			
Dynamic Burn-In (Note 1)	-	8	1, 16	2, 5, 7, 10, 12, 15	9	3, 4, 6, 11, 13, 14
Irradiation (Note 2)	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16			

**NOTE:**

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

## Logic Diagram



**FIGURE 1. 1 OF 6 FLIP-FLOPS  
TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS**

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
⌊	0	1	0
⌊	1	1	1
⌋	X	1	NC
X	X	0	0

1 = High Level  
2 = Low Level

X = Don't Care  
NC = No Change

Typical Performance Curves

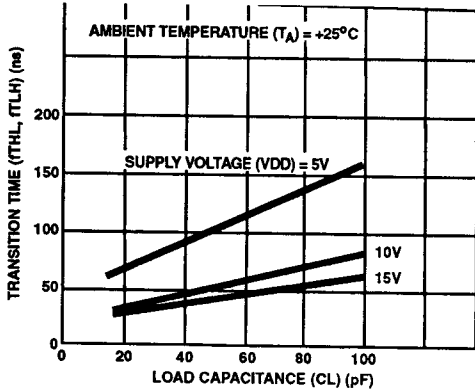


FIGURE 2. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

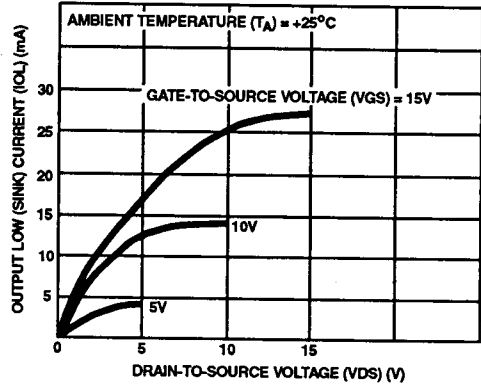


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

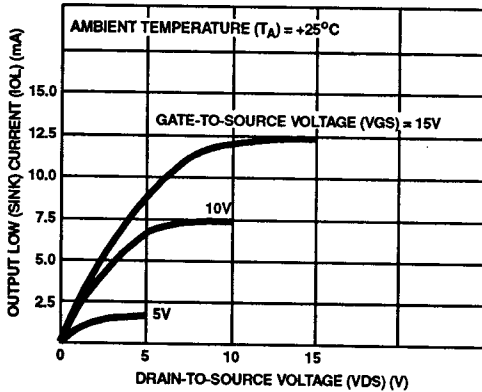


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

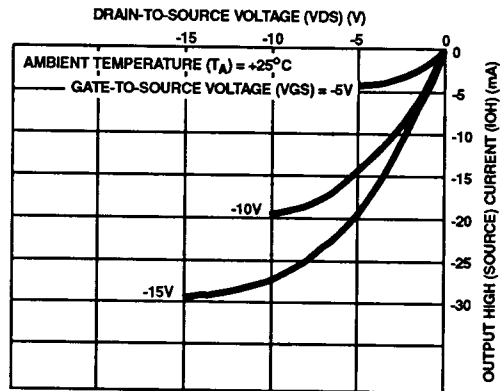


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

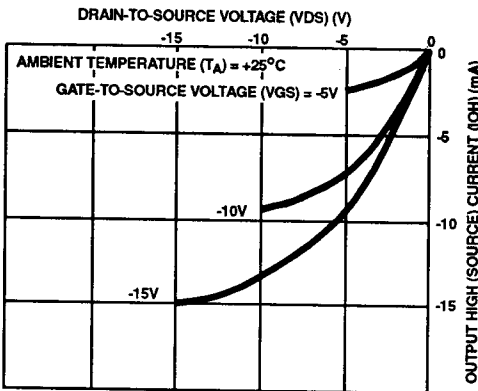


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

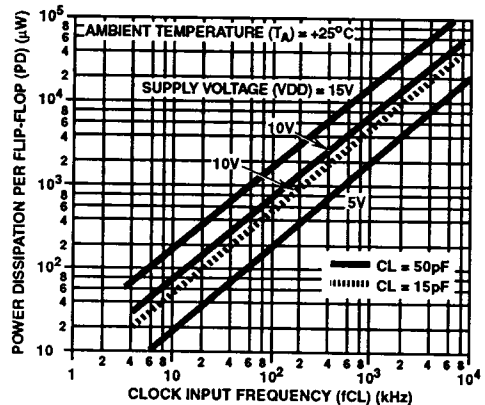


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Typical Performance Curves (Continued)

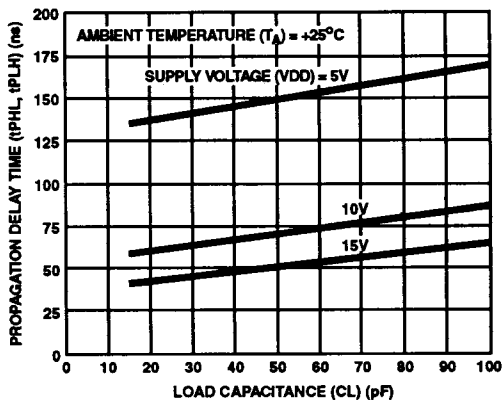


FIGURE 8. TYPICAL PROPAGATION DELAY TIME (CLOCK TO OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

Waveform

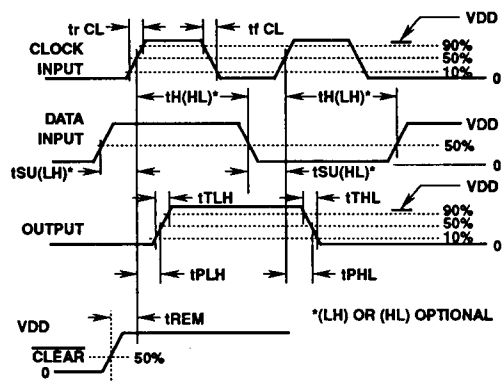
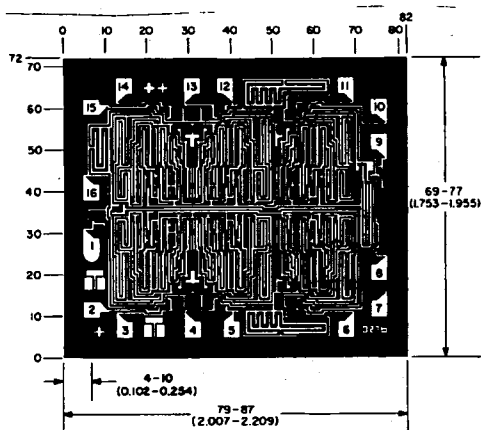


FIGURE 9. DEFINITION OF SETUP, HOLD, PROPAGATION DELAY, AND REMOVAL TIMES

Pad Layout



DIMENSIONS AND PAD LAYOUT FOR CD40174BMSH

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**METALLIZATION:** Thickness:  $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$ , AL.

**PASSIVATION:**  $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$ , Silane

**BOND PADS:** 0.004 inches X 0.004 inches MIN

**DIE THICKNESS:** 0.0198 inches - 0.0218 inches