

KM616V4002C/CL, KM616V4002CI/CLI

Preliminary
CMOS SRAM

Document Title

256Kx16 Bit High Speed Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Range.

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Preliminary.	Feb. 12. 1999	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



ELECTRONICS

256K x 16 Bit High-Speed CMOS Static RAM

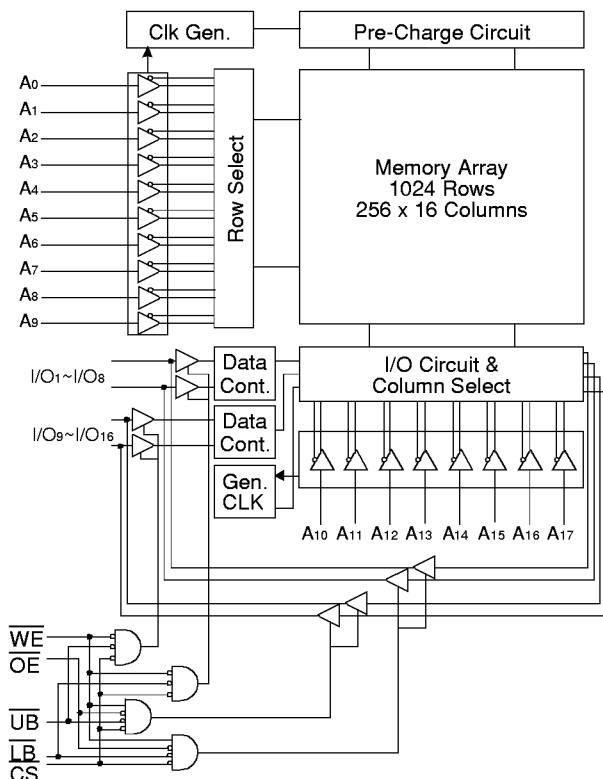
FEATURES

- Fast Access Time 10,12,15,20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 40mA(Max.)
 - (CMOS) : 10mA(Max.)
 - 0.5mA(Max.) L-ver. only
- Operating KM616V4002C/CL - 10 : 170mA(Max.)
- KM616V4002C/CL - 12 : 165mA(Max.)
- KM616V4002C/CL - 15 : 160mA(Max.)
- KM616V4002C/CL - 20 : 155mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- Standard Pin Configuration
 - KM616V4002CJ : 44-SOJ-400
 - KM616V4002CT : 44-TSOP2-400F
 - KM616V4002CF : 48-Fine pitch BGA with 0.75 Ball pitch

GENERAL DESCRIPTION

The KM616V4002C is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002C uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control(UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002C is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward or 48 Fine pitch BGA.

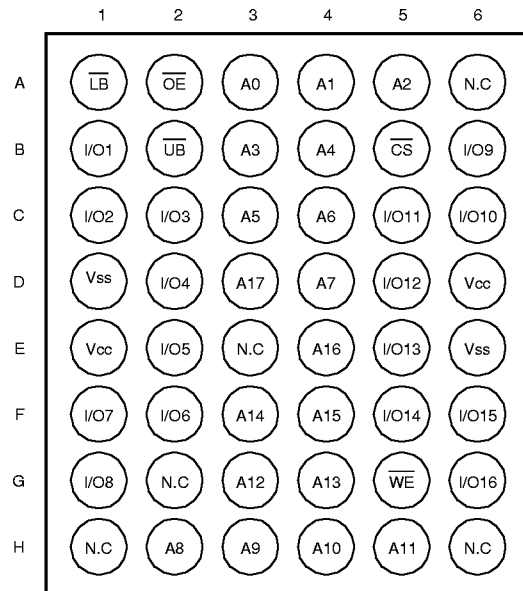
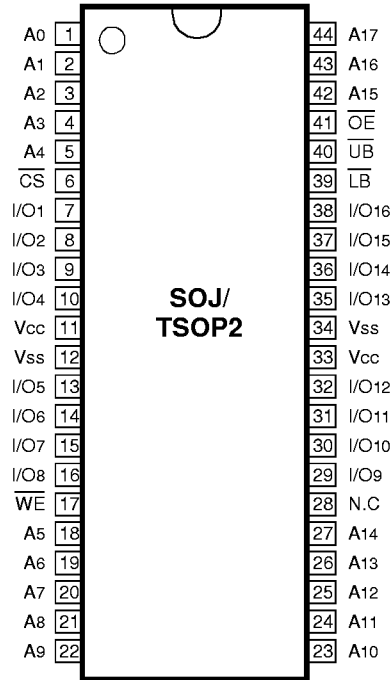
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

KM616V4002C/CL -10/12/15/20	Commercial Temp.
KM616V4002CI/CLI -10/12/15/20	Industrial Temp.

PIN CONFIGURATION (Top View)



48-CSP

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit	
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V	
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 4.6	V	
Power Dissipation	P _D	1.0	W	
Storage Temperature	T _{STG}	-65 to 150	°C	
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3.0	3.3	3.6	V
Ground	VSS	0	0	0	V
Input High Voltage	VIH	2.0	-	VCC+0.3***	V
Input Low Voltage	VIL	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** VIL(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** VIH(Max) = VCC + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(TA=0 to 70°C, VCC= 3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	VIN=VSS to VCC	-2	2	μA	
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = VSS to VCC	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty CS=VIL, VIN=VIH or VIL, IOUT=0mA	10ns	-	170	mA
			12ns	-	165	
			15ns	-	160	
			20ns	-	155	
Standby Current	ISB	Min. Cycle, CS=VIH	-	40	mA	
	ISB1	f=0MHz, CS≥VCC-0.2V, VIN≥VCC-0.2V or VIN≤0.2V	Normal	-		10
			L-ver.	-		0.5
Output Low Voltage Level	VOL	IOL=8mA	-	0.4	V	
Output High Voltage Level	VOH	IOH=-4mA	2.4	-	V	

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CIO	VIO=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

* Capacitance is sampled and not 100% tested.

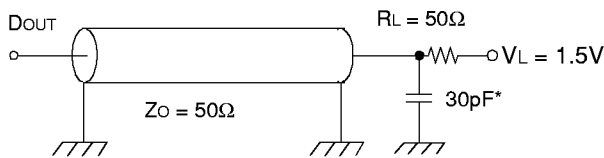
AC CHARACTERISTICS (TA=0 to 70°C, VCC=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS*

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

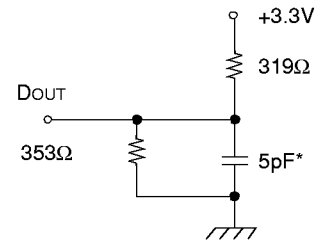
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	KM616V4002C-10		KM616V4002C-12		KM616V4002C-15		KM616V4002C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	20	-	ns
Address Access Time	tAA	-	10	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	10	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	-	9	ns
\overline{UB} , \overline{LB} Access Time	tBA	-	5	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
\overline{UB} , \overline{LB} Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	0	9	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	0	9	ns
\overline{UB} , \overline{LB} Disable to High-Z Output	tBHZ	0	5	0	6	0	7	0	9	ns
Output Hold from Address	tOH	3	-	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at industrial temperature range.

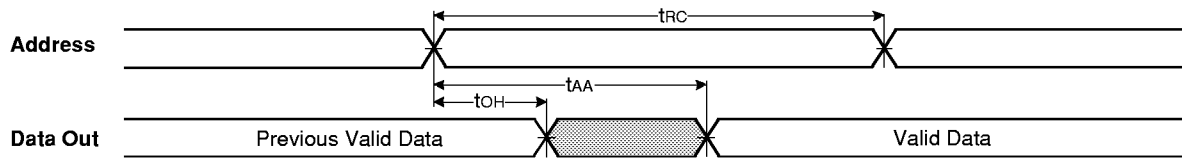
WRITE CYCLE*

Parameter	Symbol	KM616V4002C-10		KM616V4002C-12		KM616V4002C-15		KM616V4002C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	20	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of	t _{AW}	7	-	8	-	10	-	12	-	ns
Write Pulse Width(\overline{OE} High)	t _{WP}	7	-	8	-	10	-	12	-	ns
Write Pulse Width(\overline{OE} Low)	t _{WP1}	10	-	12	-	15	-	20	-	ns
\overline{UB} , \overline{LB} Valid to End of	t _{BW}	7	-	8	-	10	-	12	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	0	9	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	9	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	3	-	ns

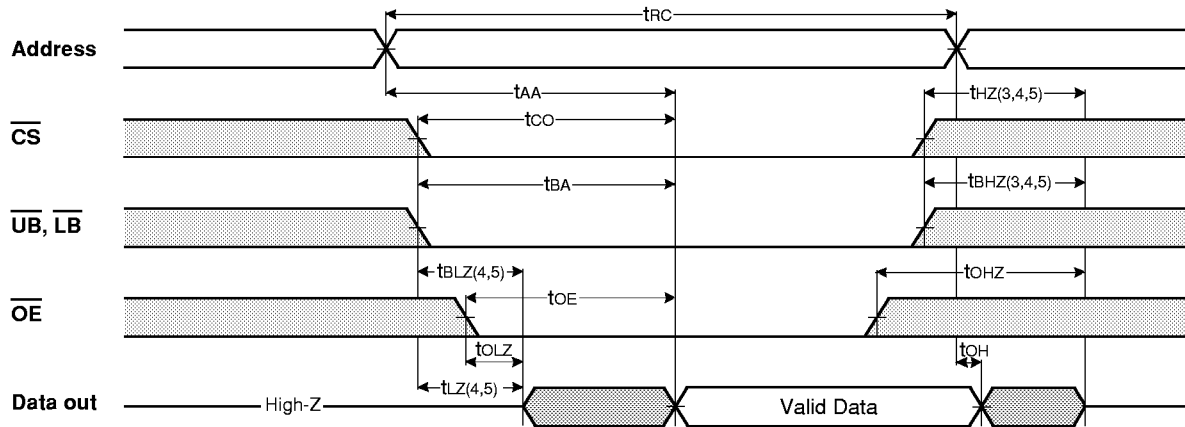
* The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} , $\overline{LB}=V_{IL}$)



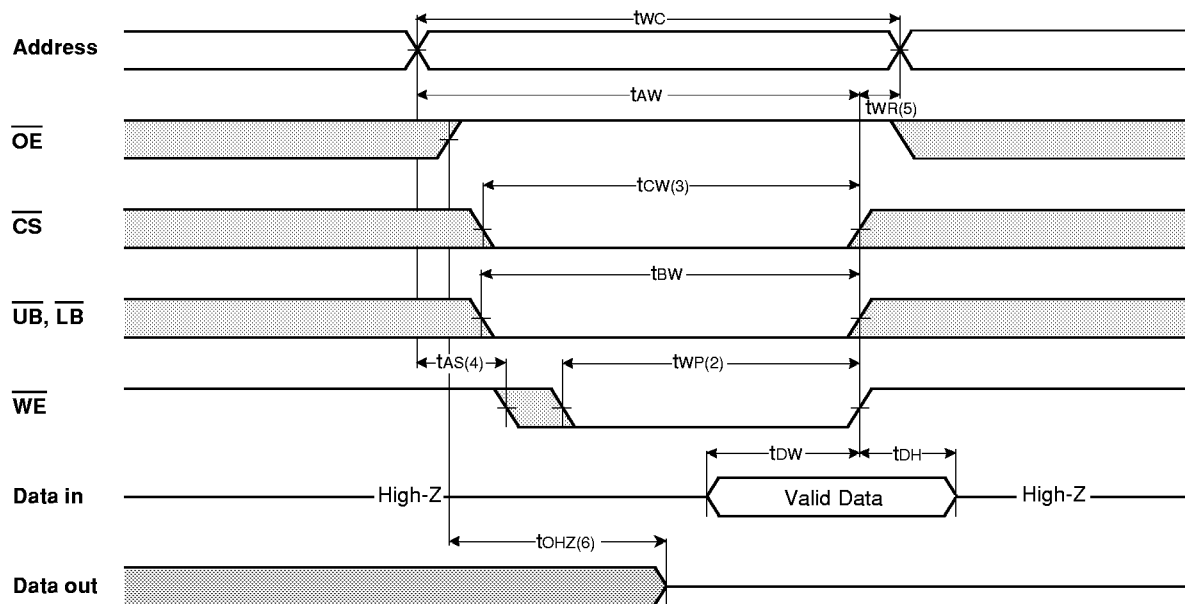
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



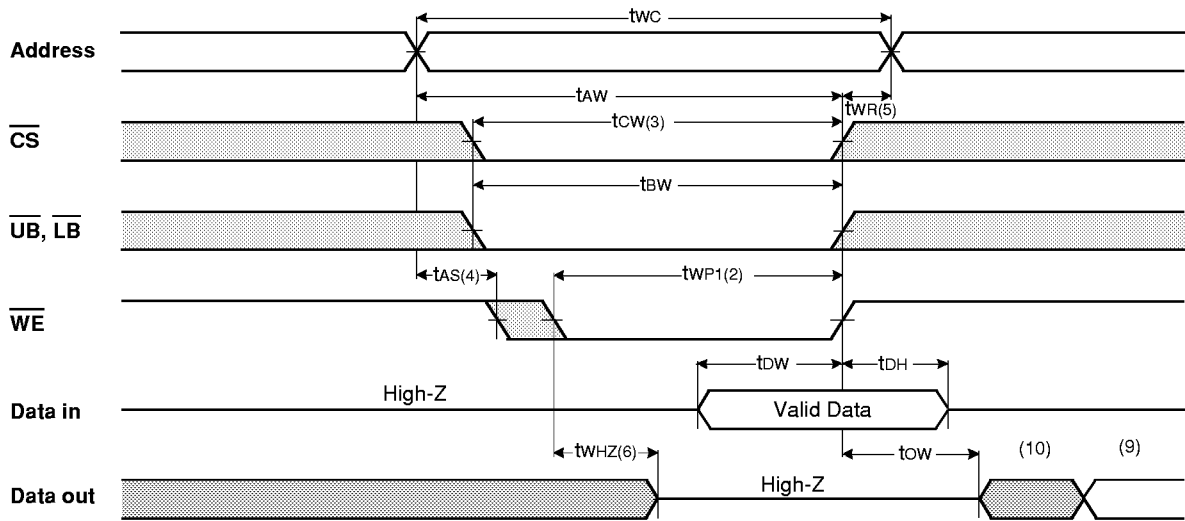
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, tHZ(Max.) is less than tHZ(Min.) both for a given device and from device to device.
5. Transition is measured $\pm 200mV$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

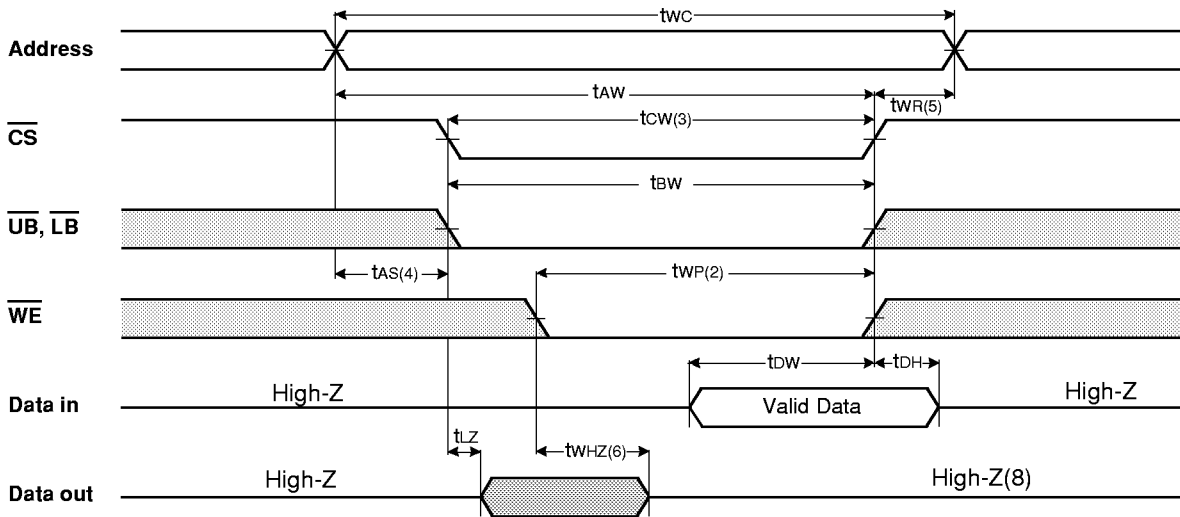
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{OE} Clock)



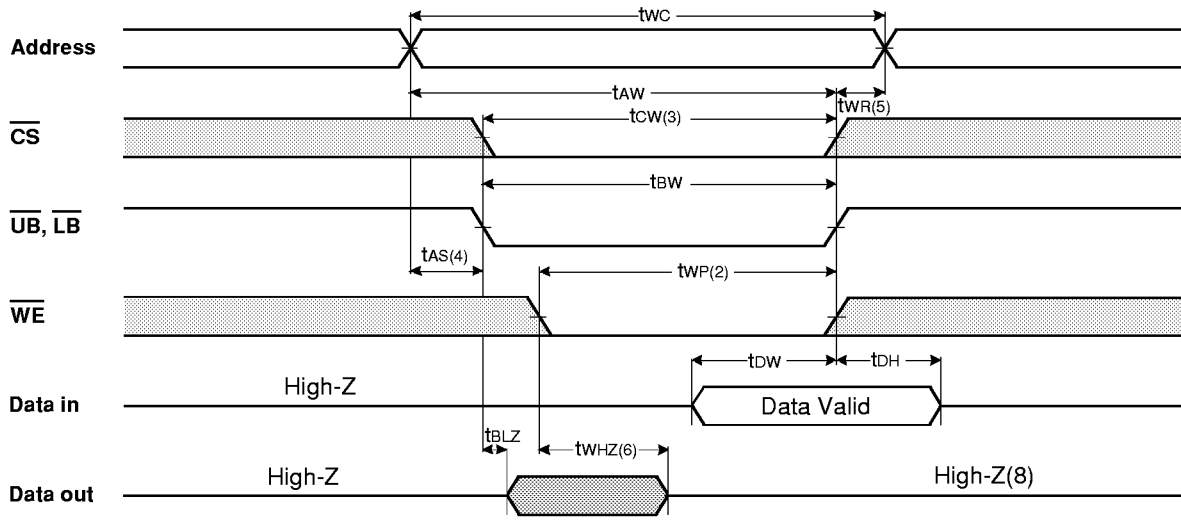
TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} = Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} = Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) (\overline{UB} , \overline{LB} Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{wp} is measured from the beginning of write to the end of write.
3. t_{cw} is measured from the later of \overline{CS} going low to end of write.
4. t_{as} is measured from the address valid to the beginning of write.
5. t_{wr} is measured from the end of write to the address change. t_{wr} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H				
L	L	L	L	H	Read	DOUT	High-Z	Icc
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

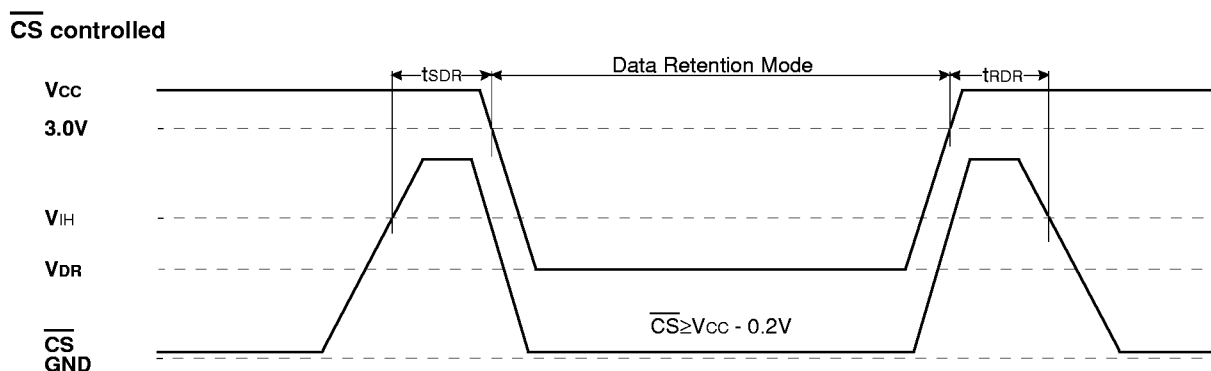
* X means Don't Care.

DATA RETENTION CHARACTERISTICS* (TA=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data Retention Current	IDR	$V_{CC} = 3.0V, \overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.4	mA
		$V_{CC} = 2.0V, \overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR	See Data Retention Wave form(below)	5	-	-	ms

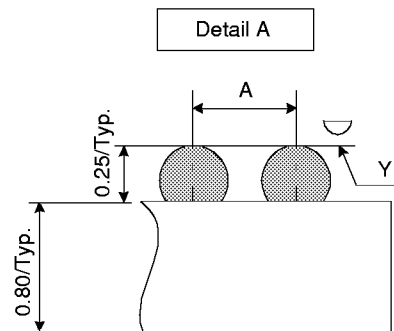
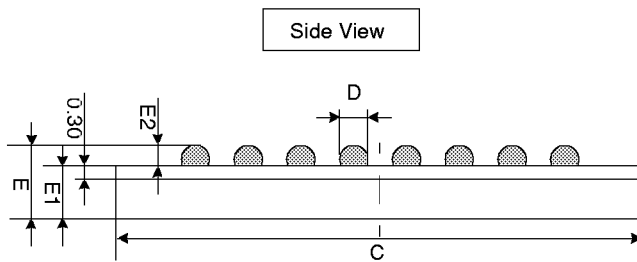
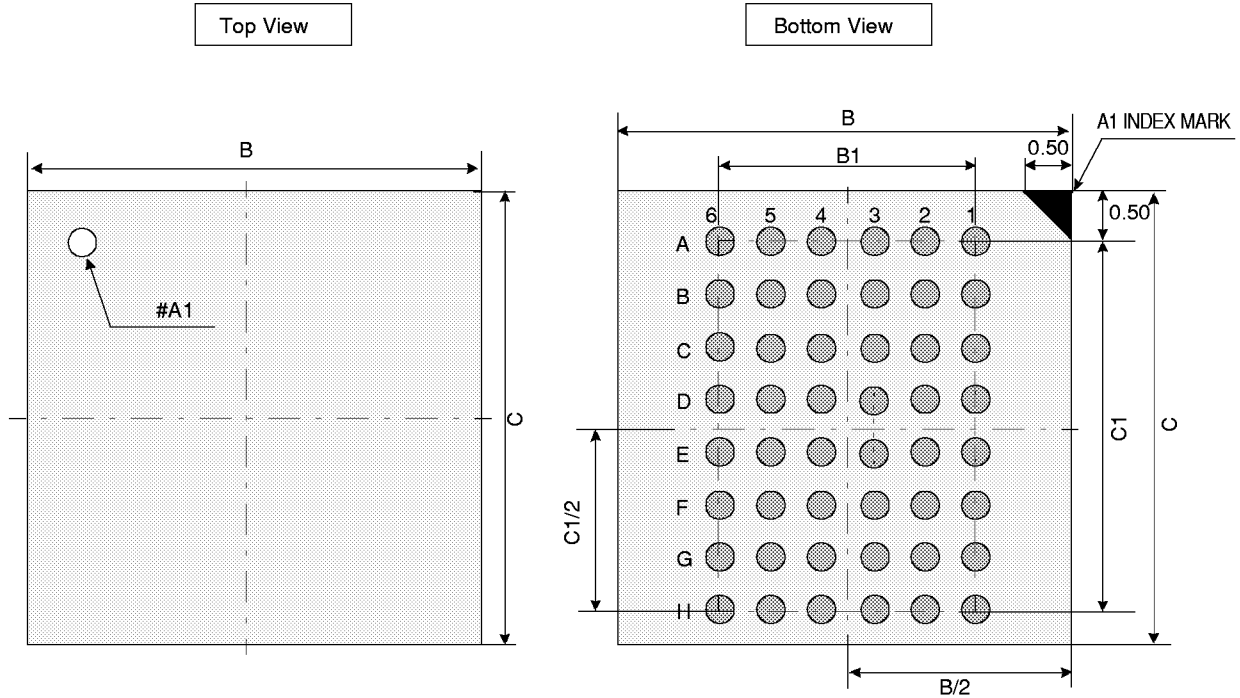
* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-Ver only.

DATA RETENTION WAVE FORM



PACKAGE DIMENSIONS

Units : millimeter.



	Min	Typ	Max
A	-	0.75	-
B	8.90	9.00	9.10
B1	-	3.75	-
C	8.90	9.00	9.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.05	1.20
E1	-	0.80	-
E2	0.20	0.25	0.30
Y	-	-	0.08

- Notes.**
1. Bump counts: 48(8row x 6column)
 2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
 3. All tolerance are +/-0.050 unless otherwise specified.
 4. Typ : Typical
 5. Y is coplanarity: 0.08(Max)