IH5341

High Reliability Dual SPST CMOS RF/Video Switch

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GENERAL DESCRIPTION

The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically $t_{on}=150ns$ and $t_{off}=80ns$, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically 40Ω–50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 packages.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5341MTW	−55°C to +125°C	10-pin TO−100

FEATURES

- **$R_{DS(on)}<75\Omega$**
- **Switch Attenuation Varies Less Than 3dB From DC to 100MHz**
- **"OFF" Isolation>70dB Typical @ 10MHz**
- **Cross Coupling Isolation>60dB @ 10MHz**
- **Compatible With TTL, CMOS Logic**
- **Wide Operating Power Supply Range**
- **Power Supply Current≤1μA**
- **"Break-Before-Make" Switching**
- **Fast Switching (80ns/150ns Typ)**

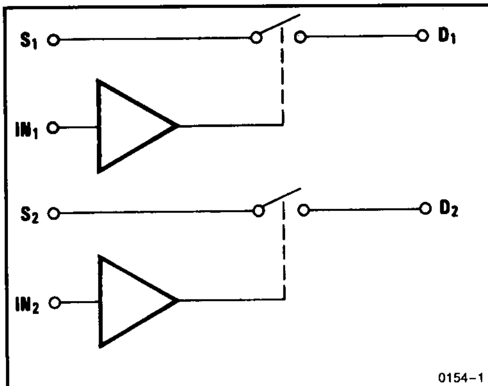
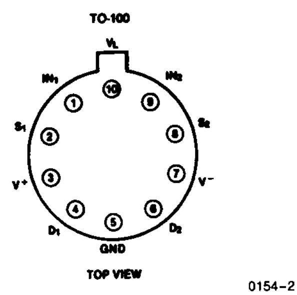


Figure 1: Functional Diagram (Switches are open for a logical "0" control input, and closed for a logical "1" control input.)



Outline dwg: TW

Figure 2: Pin Configuration

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ABSOLUTE MAXIMUM RATINGS

V^+ to Ground .... +18V
V^- to Ground .... −18V
V_L to Ground .... V^+ to V^-
Logic Control Voltage .... V^+ to V^-
Analog Input Voltage .... V^+ to V^-
Current (any Terminal) 50mA
Operating Temperature:
(M Version) .... −55°C to +125°C

Storage Temperature .... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .... 300°C
Power Dissipation 250mW
Derate above 25°C @ .... 7.5mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

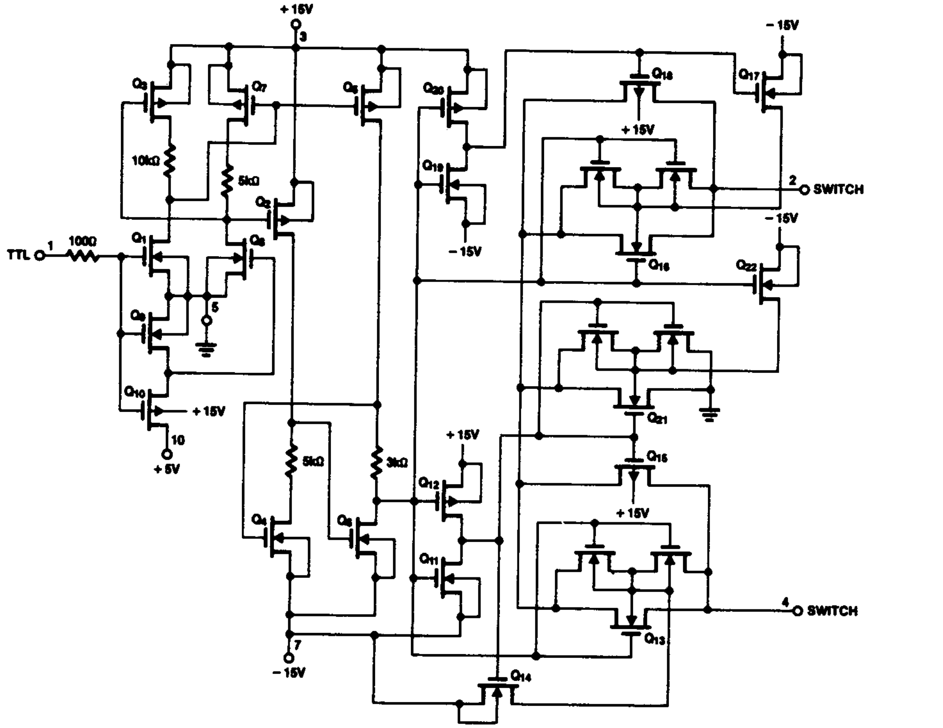

Figure 3: Equivalent Schematic Diagram IH5341ITW (½ of actual circuit on chip shown)

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DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Typ	M Grade Device			Units
				−55°C	+25°C	+125°C	
 V^+ V_L V^-	Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	(Note 3)	4.5>16 4.5>V+ −4>−16				V
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	$V_D = \pm5V$		75	75	100	Ω
		$I_S = 10mA$, $V_{IN} \geq 2.4V$ $V_D = \pm10V$		125	125	175	
$R_{DS(on)}$	Switch "ON" Resistance	$V^+ = V_L = +5V$, $V_{IN} = 3V$ $V^- = -5V$, $V_D = \pm3V$ $I_S = 10mA$		250	250	350	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	$I_S = 10mA$, $V_D = \pm5V$	5				
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		>2.4 <0.8				V
$I_{D(off)}$ or $I_{S(off)}$	Switch "OFF" Leakage (Notes 2 and 4)	$V_{S/D} = \pm5V$ $V_{IN} \leq 0.8V$			±0.5	50	nA
		$V_{S/D} = \pm14V$			±0.5	50	
$I_{D(on)}$ + $I_{S(on)}$	Switch "ON" Leakage	$V_{S/D} = \pm5V$ $V_{IN} \geq 2.4V$			±1	50	
		$V_{S/D} = \pm14V$			±1	100	
I_{IN}	Input Logic Current	$V_{IN} \geq 2.4V$ or $< 0V$	0.1	±1	±1	10	µA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	
I^-	Negative Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	
I_L	Logic Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	

NOTES: 1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified (Note 5).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Switch "ON" Time	See Figure 4		150	300	ns
t_{off}	Switch "OFF" Time	See Figure 4		80	150	
OIRR	"OFF" Isolation Rejection Ratio	See Figure 5 (Note 6)		70		dB
CCRR	Cross Coupling Rejection Ratio	See Figure 6 (Note 6)		60		
f_{3dB}	Switch Attenuation 3dB Frequency	See Figure 7 (Note 6)		100		

NOTES: 5. All AC parameters are sample tested only.
6. Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

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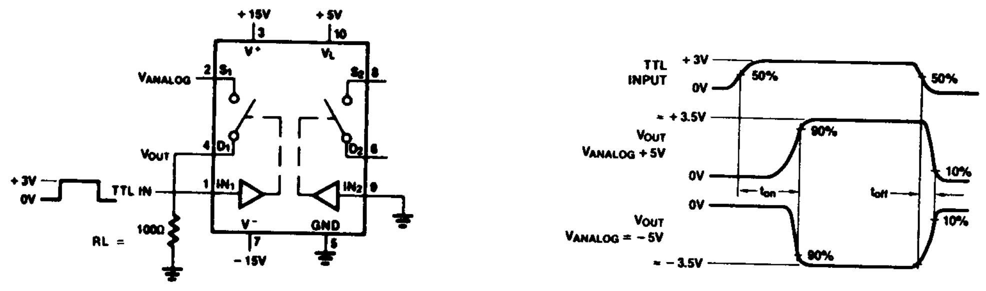
TEST CIRCUITS



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Note: Only one channel shown. Other acts identically.

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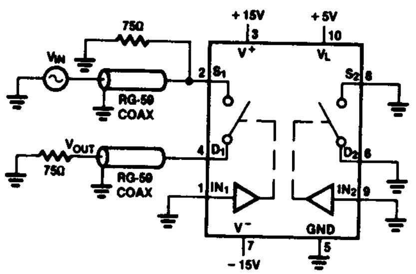
Figure 4: Switching Time Test Circuit and Waveforms



$V_{IN} = \pm 5V\ (10V_{p\text{-}p})$ @ f = 10MHz

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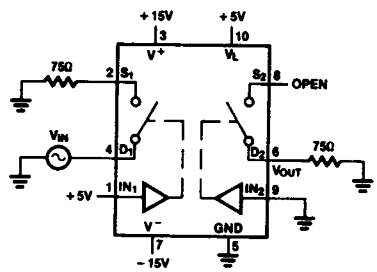
$$OIRR = 20\log \frac{V_{IN}}{V_{OUT}}$$

Note: Only one channel shown. Other acts identically.

Figure 5: OFF Isolation Test Circuit



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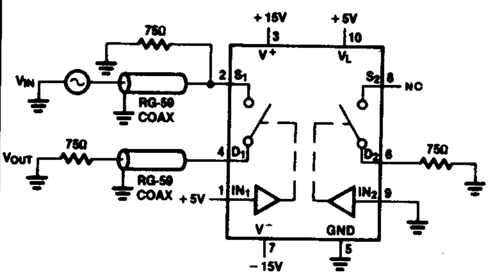
$V_{IN} = 225mVrms$ @ f = 10MHz

$$CCRR = 20\log \frac{V_{IN}}{V_{OUT}}$$

Figure 6: Cross-Coupling Rejection Test Circuit



$$ATTN: = 20\ \log_{10} \frac{R_L}{R_{DS(on)} + R_L}$$

Nominally, at DC, this ratio is equal to −4dB. When the attenuation reaches −1dB, the frequency at which this occurs is f_{3dB}.

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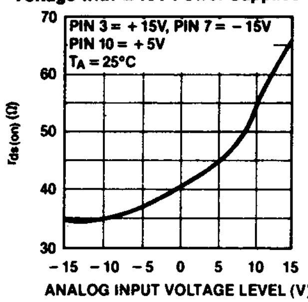
Note: Only one channel shown. Other acts identically.

Figure 7: Switch Attenuation Versus Frequency, Test Circuit

TYPICAL PERFORMANCES CHARACTERISTICS

$R_{DS(on)}$ Versus Analog Input Voltage with ± 15V Power Supplies



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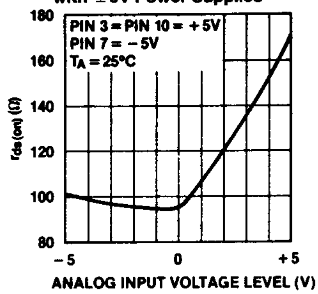
$R_{DS(on)}$ Versus Analog Input Level with ± 5V Power Supplies



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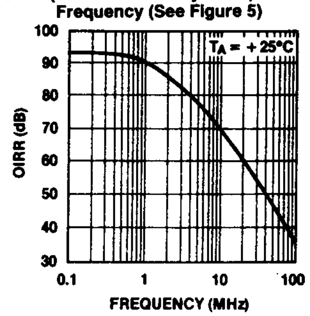
OIRR (OFF Isolation Rejection) Versus Frequency (See Figure 5)



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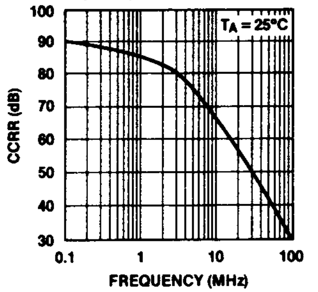
CCRR (Cross Coupling Rejection) Versus Frequency (See Figure 6)



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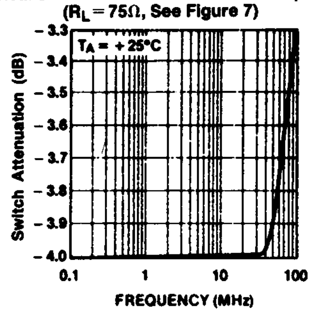
Typical Switch Attenuation Versus Frequency (R_L = 75Ω, See Figure 7)



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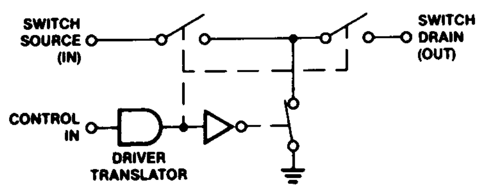

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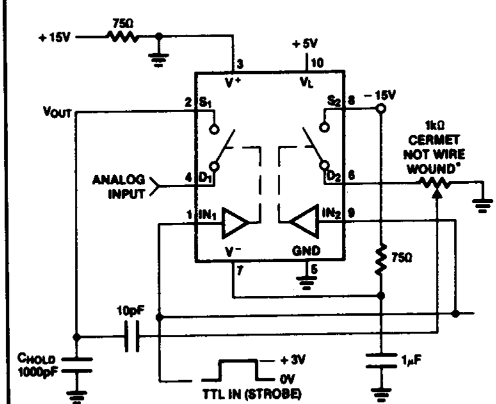
Figure 8: Internal Switch Configuration



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*Adjust pot for 0mV$_{p-p}$ step @ V_{OUT} with no analog (AC) signal present

Figure 9: Charge Injection Compensation

DETAILED DESCRIPTION

As can be seen in Figure 8, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than a single series switch does, especially at high frequencies. The result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, giving very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.

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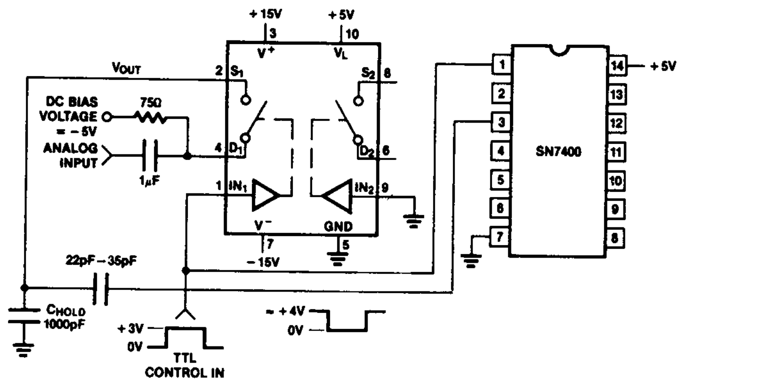

Figure 10: Alternative Compensation Circuit

APPLICATIONS

Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 9 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the −5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 10. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to −5V as shown in the figure. The choice of −5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.

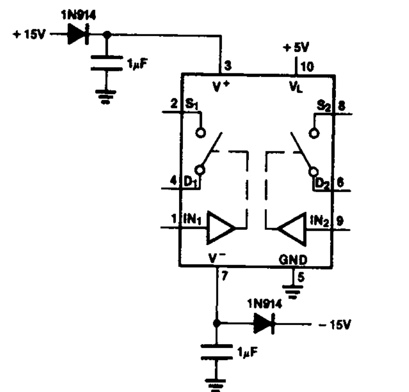

Figure 11: Overvoltage Protection Circuit

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 11.