Signetics

74AC/ACT11534

Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State), INV

Product Specification

ACL Products

FEATURES

- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11534 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11534 device is an 8-bit, edge-triggered register coupled to eight 3-State, inverting output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's $\overline{Q}$ output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF		7.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	75	92	pF
			Disabled	65	82	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		100	70	MHz

Note:

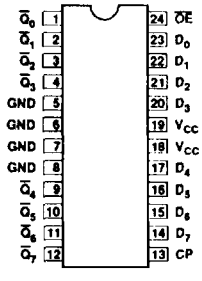
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

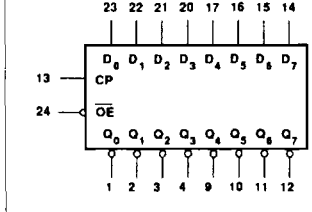
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11534N 74ACT11534N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11534D 74ACT11534D

PIN CONFIGURATION

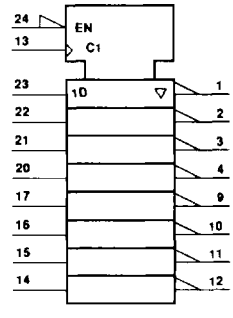
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State inverting buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

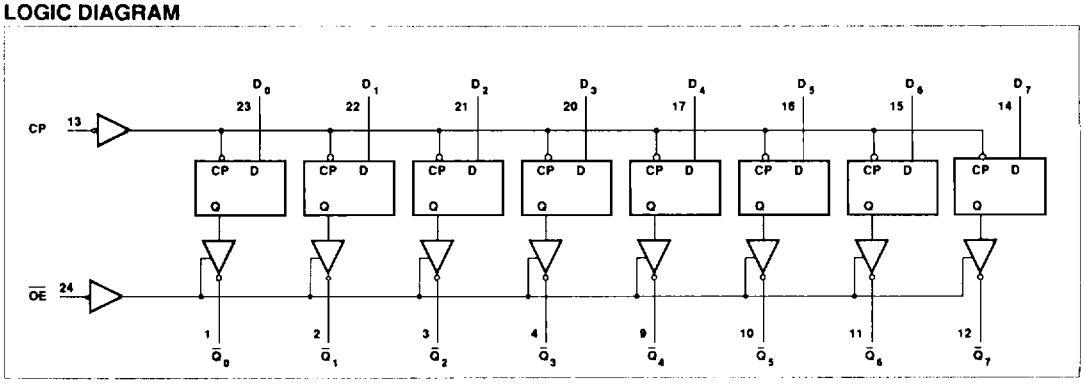
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_n$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11534			74ACT11534			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11534 T_A = +25°C		74AC11534 T_A = -40°C to +85°C		74ACT11534 T_A = +25°C		74ACT11534 T_A = -40°C to +85°C		UNIT
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	50	75		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	1	1.5 1.5	11.0 11.0	15.3 15.7	1.5 1.5	17.6 17.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 9.0	12.8 12.6	1.5 1.5	14.6 14.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.6 13.0	1.5 1.5	13.3 13.8	ns
t_W	Clock pulse width High or Low	1	10.0			10.0		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

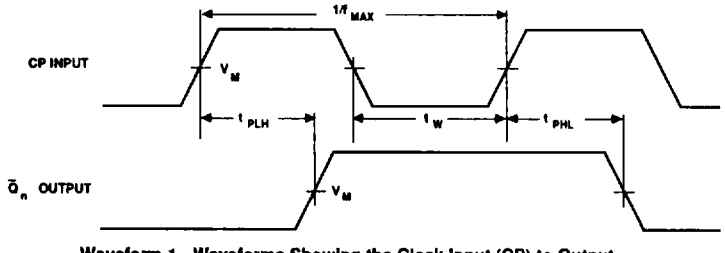
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	1	1.5 1.5	7.0 7.0	10.3 10.7	1.5 1.5	11.7 12.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.0 6.0	9.2 9.2	1.5 1.5	10.4 10.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.1 8.8	1.5 1.5	11.6 9.2	ns
t_W	Clock pulse width High or Low	1	6.5			6.5		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	4.5			4.5		ns

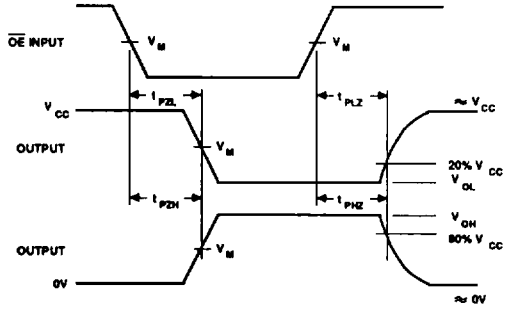
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	55	70		55		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{O}_n$	1	1.5 1.5	8.5 8.5	12.7 13.3	1.5 1.5	14.5 15.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	12.0 12.2	1.5 1.5	13.3 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.9 11.2	1.5 1.5	13.5 12.0	ns
t_W	Clock pulse width High or Low	1	9.0			9.0		ns
t_S	Setup time D_n to CP	3	3.0			3.0		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

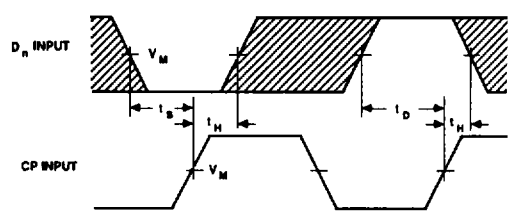
AC WAVEFORMS



Waveform 1. Waveforms Showing the Clock Input (CP) to Output ($\overline{O}_n$) Propagation Delays and Clock Input (CP) Pulse Width



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

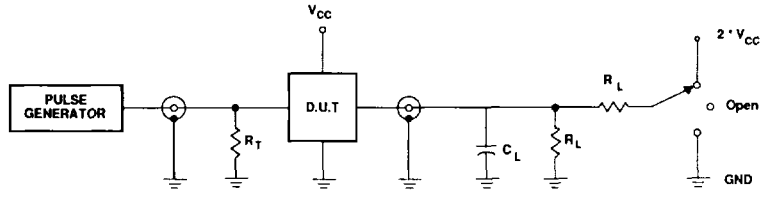


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for D_n Input to CP Input

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns