

Description

Q-Tech’s Leadless Chip Carrier crystal oscillators consist of a source clock square wave generator, logic output buffers and/or logic divider stages, and a round AT high-precision quartz crystal built in a ceramic true SMD package.

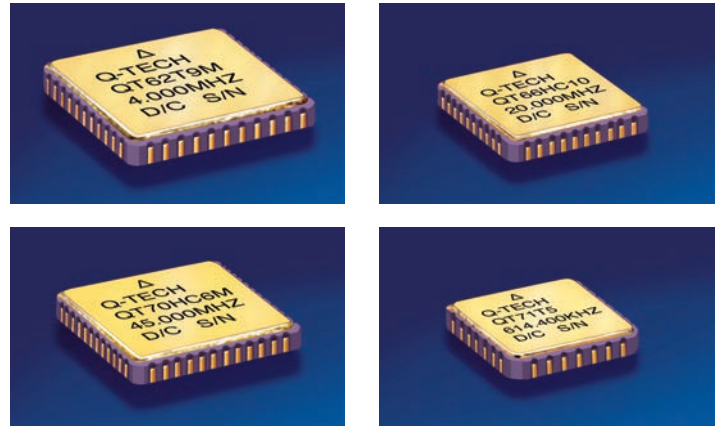
Features

- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- USML Registration # M17677
- Wide frequency range from 732.4Hz to 150MHz
- Available as QPL MIL-PRF-55310/19 (QT66T), /20 (QT62T), and /29 (QT66HCD)
- Choice of packages and pin outs
- Choice of supply voltages
- Choice of output logic options (CMOS, ACMOS, HCMOS, LVHCMOS, TTL, ECL, PECL, and LVPECL)
- AT-Cut crystal
- True SMD hermetically sealed package
- Tight or custom symmetry available
- Low height available
- External tuning capacitor option
- Fundamental and third overtone designs
- Tristate function option D
- Four-point crystal mounts
- Custom design available tailors to meet customer’s needs
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant



Applications

- Designed to meet today’s requirements for all voltage applications
- Wide military clock applications
- Industrial controls
- Microcontroller driver



Ordering Information

(Sample part number)

QT62HCD9M-20.000MHz

Q	T	62	HC	D	9	M	-	20.000MHz
----------	----------	-----------	-----------	----------	----------	----------	----------	------------------

Solder Dip Option:
T = Standard
S = Solder Dip (*)

Package:
(See page 3)

Logic & Supply Voltage:
C = CMOS +5.0V to +15.0V(**)
AC = ACMOS +5.0V
HC = HCMOS +5.0V
T = TTL +5.0V
L = LVHCMOS +3.3V
N = LVHCMOS +2.5V
R = LVHCMOS +1.8V
Z = Z output

Tristate Option:
Blank = No Tristate
D = Tristate

Output Frequency

Screening Option:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

Frequency vs. Temperature Code:

1	= ± 100ppm at 0°C to +70°C
3(**)	= ± 5ppm at 0°C to +50°C
4	= ± 50ppm at 0°C to +70°C
5	= ± 25ppm at -20°C to +70°C
6	= ± 50ppm at -55°C to +105°C
9	= ± 50ppm at -55°C to +125°C
10	= ± 100ppm at -55°C to +125°C
11	= ± 50ppm at -40°C to +85°C
12	= ± 100ppm at -40°C to +85°C

(*) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost
 (**) Please specify supply voltage when ordering CMOS
 (***) Requires an external capacitor

For frequency stability vs. temperature options not listed herein, please request a custom part number.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Packaging Options

- Standard packaging in anti-static plastic tube
- Optional Tape and Reel

Other Options Available For An Additional Charge

- P. I. N. D. test (MIL-STD 883, Method 2020)

Specifications subject to change without prior notice.



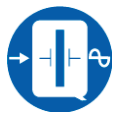
Electrical Characteristics

Parameters		C	AC	HC	T	L (*)
Output freq. range (Fo)	QT62, 70	732.4Hz — 15MHz		732.4Hz — 85MHz		732.4Hz — 85MHz
	QT66	732.4Hz — 15MHz				732.4Hz — 125MHz
	QT71	100kHz — 15MHz				100kHz — 125MHz
	QT75	N/A				15kHz — 150MHz
Supply voltage (Vdd)		5V ~ 15Vdc ± 10%		5.0Vdc ± 10%		3.3Vdc ± 10%
Maximum Applied Voltage (Vdd max.)		-0.5 to +18Vdc		-0.5 to +7.0Vdc		-0.5 to +5.0Vdc
Freq. stability (ΔF/ΔT)				See Option codes		
Operating temp. (Topr)				See Option codes		
Storage temp. (Tsto)				-62°C to + 125°C		
Operating supply current (Idd) (No Load)	F and Vdd dependent 3 mA max. at 5V up to 5MHz 25 mA max. at 15V up to 15MHz			20 mA max. - 732.4Hz ~ < 16MHz 25 mA max. - 16MHz ~ < 40MHz 35 mA max. - 40MHz ~ < 60MHz 45 mA max. - 60MHz ~ 85MHz		3 mA max. - 732.4Hz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ ≤150MHz
Symmetry (50% of output waveform or 1.4Vdc for TTL)		45/55% max. Fo < 4MHz 40/60% max. Fo ≥ 4MHz		45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz		
Rise and Fall times (with typical load)	30ns max. (Measured from 10% to 90%)			15ns max. Fo < 15kHz 6ns max. Fo 15kHz ~ 39.999MHz 3ns max. Fo 40MHz ~ 160 MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)		
Output Load		15pF // 10kΩ		10TTL Fo < 20MHz 6TTL Fo ≥ 20MHz		15pF // 10kΩ
Start-up time (Tstup)		10ms max.				
Output voltage (Voh/Vol)		0.9 x Vdd min.; 0.1 x Vdd max.		2.4V min.; 0.4V max.		0.9 x Vdd min.; 0.1 x Vdd max.
Output Current (Ioh/Iol)		± 1mA typ. at 5V ± 6.8mA typ. at 15V	± 24mA	± 8 mA	-1.6mA / TTL +40μA / TTL	± 4mA.
Enable/Disable Tristate function Pin 1	Call for details			VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance		VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance
Jitter RMS 1σ (at 25°C)				8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz		15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz
Aging (at 70°C)		± 5ppm max. first year / ± 2ppm typ. per year thereafter				

(*) Available in 2.5Vdc (N) or 1.8Vdc (R)

Z - Output logic can drive up to 200 pF load with typical 6ns rise & fall times (tr, tf)

ECL, PECL, LVPECL are available. Please contact Q-Tech for details.



Q-TECH
CORPORATION

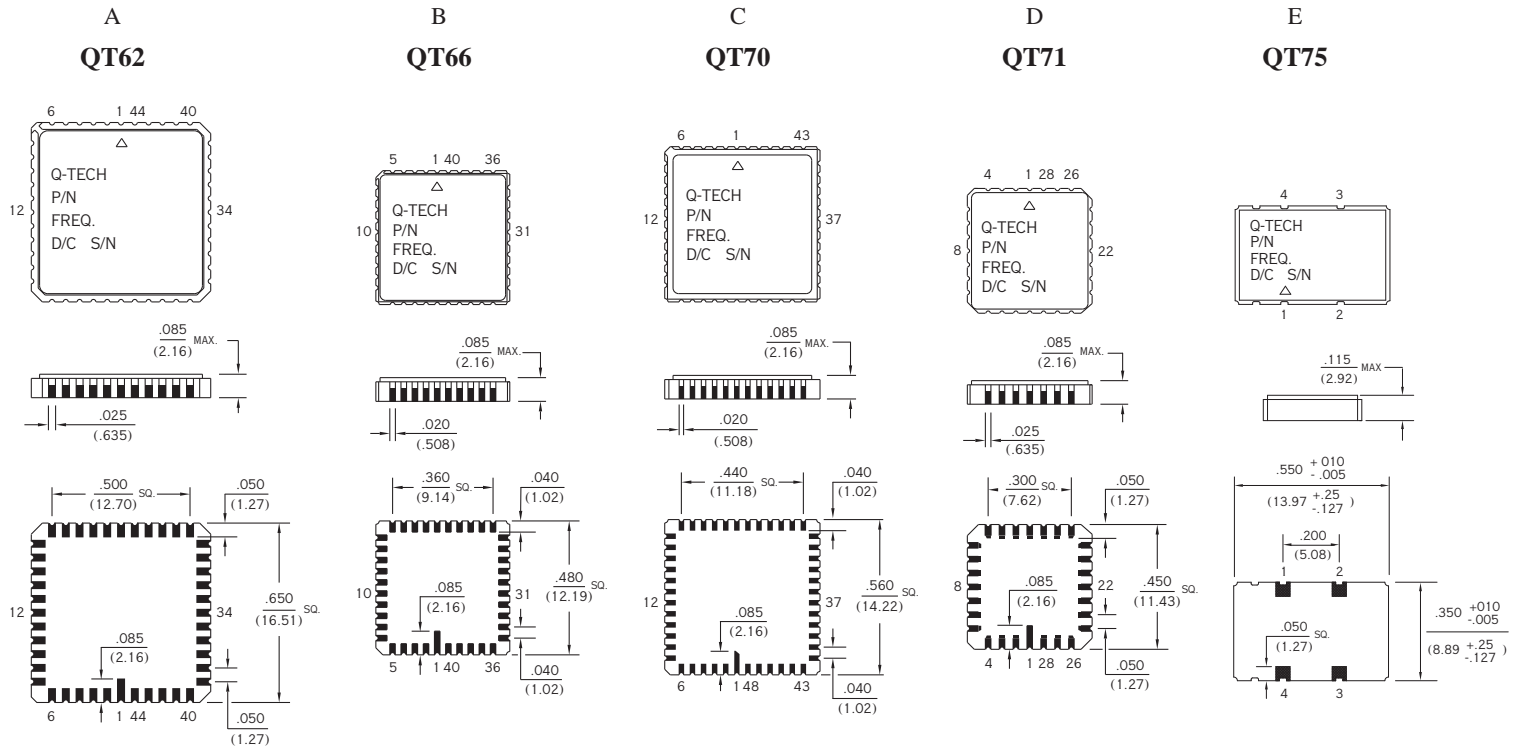
LEADLESS CHIP CARRIER

CRYSTAL CLOCK OSCILLATORS

18 to 15Vdc - 732.4Hz to 150MHz

Package Outline and Pin Connections

Dimensions are in inches (mm)



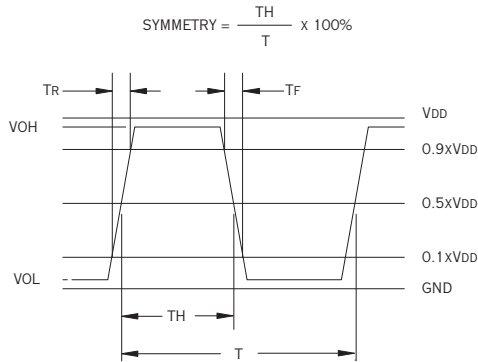
QT #	Conf	Vcc	GND	Case	Output	E/D or N/C	Equivalent MIL-PRF-55310 Configuration
QT62	A	6 & 12	34 & 40	34 & 40	42	41	/20 = QT62T
QT66	B	4 & 10	31 & 37	31 & 37	39	32	/19 = QT66T /29 = QT66HCD
QT70	C	5	44	44	47	N/A	N/A
QT71	D	4 & 8	22 & 26	22 & 26	28	27	N/A
QT75	E	4	2	2	3	1	N/A

Please contact factory for pin connections on external capacitor (code 3).

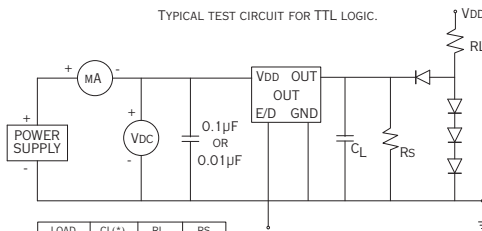
Package Information

- Package material (Header): 91% AL_2O_3
(Metalization): Tungsten
- Lead finish: Gold Plated – 50 μ ~ 80 μ inches
Nickel Underplate – 100 μ ~ 250 μ inches
- Cover: Kovar, Gold Plated – 60 μ ~ 90 μ inches
Nickel Underplate – 50 μ ~ 100 μ inches
With attached Preform – 80% Au, 20% Sn
- Package to lid attachment: Seam weld
- Weight: 2.0g typ., 3.0g max.

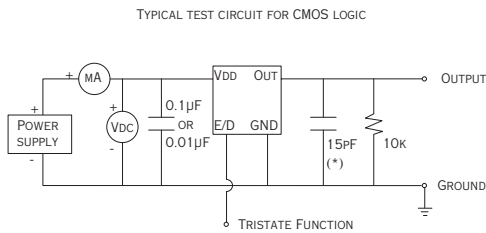
Output Waveform (Typical)



Test Circuit



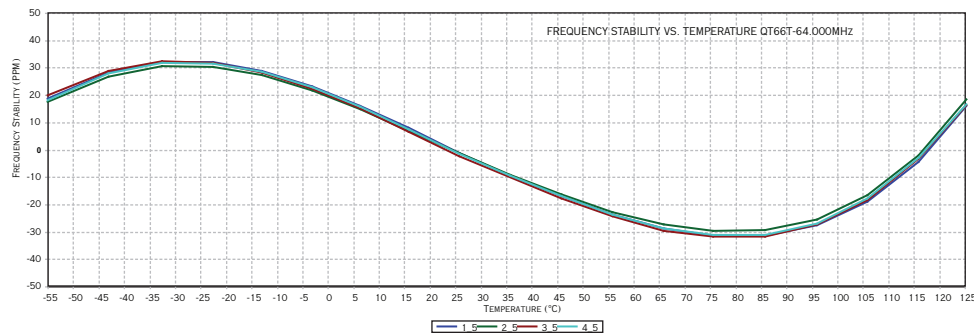
(*) CL INCLUDES THE LOADING EFFECT OF THE OSCILLOSCOPE PROBE.



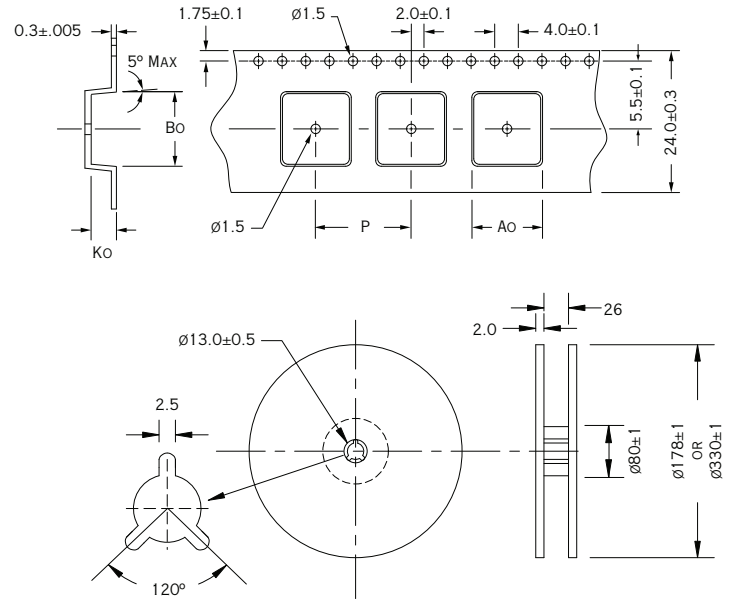
(*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Frequency vs. Temperature Curve



Tape and Reel



Dimensions are in mm. Tape is compliant to EIA-481-A.

QT#	P (mm)	Ao (mm)	Bo (mm)	Ko (mm)	Reel size (Diameter in mm)	Qty per reel (pcs)
QT62	20	17	17.30	2.70	178mm	100
					330mm	600
QT66	16	12.57	12.57	2.54	178mm	280
					330mm	1,200
QT71	16	12.00	12.00	3.00	178mm	280
					330mm	1,200
QT75	12	9.50	14.60	3.40	178mm	250
					330mm	1,000

Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

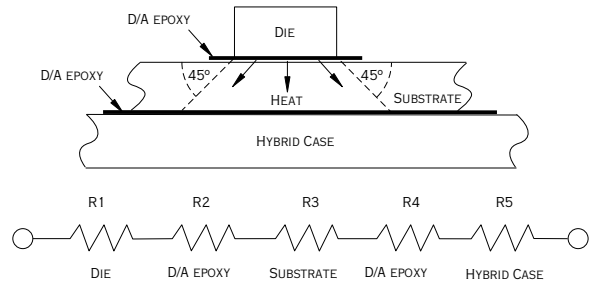
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance R_T (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in °C/W.

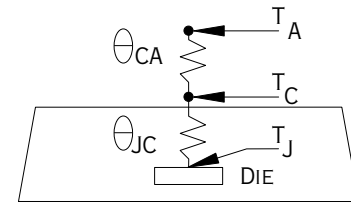
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- $PD(max) = (T_J(max) - T_A) / \theta_{JA}$
- With $T_J = 175^\circ C$ (Maximum junction temperature of die)
- $PD(max) = (175 - 25) / 130 = 1.15W$



(Figure 1)



$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

(Figure 2)

Environmental Specifications

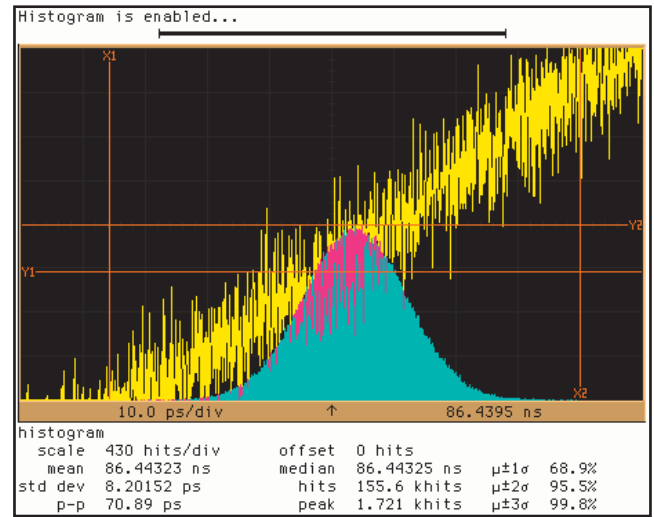
Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our Leadless Chip Carrier packages. Q-Tech can also customize screening and test procedures to meet your specific requirements. The Leadless Chip Carrier packages are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ± 1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Please contact Q-Tech for higher shock requirements

Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT66T-24MHz, at 5.0Vdc.



RMS jitter (1σ): 8.20ps Peak-to-peak jitter: 70.89ps

Phase Noise and Phase Jitter Integration

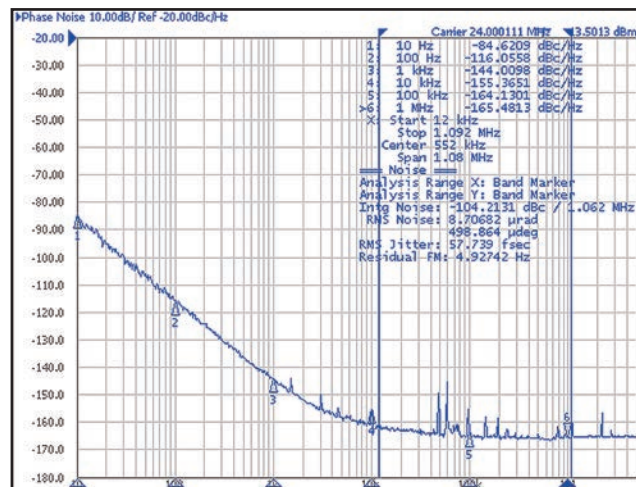
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting $L(f)$ back to $S\phi(f)$ over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int L(f)$	Integrated single side band phase noise (dBc)
$S\phi(f) = (180/\pi) \times \sqrt{2} \int L(f) df$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = $S\phi(f) / (f_{osc} \cdot 360^\circ)$	Jitter (in seconds) due to phase noise. Note $S\phi(f)$ in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT66T10M, 5.0Vdc, 24MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT66T10M, 5.0Vdc, 24MHz



Revision History (Old ECO Format)

ECO	REV	REVISION SUMMARY	Page
9935	G	Revert From: ECCN: 3A001.b.10 Back To: ECCN: EAR99	1
10850	H	Change freq range for QT71 for AC, HC, & T logic From: 100kHz to 85MHz To: 732.4Hz to 85MHz	2
		----- Added document # QPDS-0011 to footer	All

Revision History

DCO	REV	REVISION SUMMARY	Page(s)	Date
8832	-	Change Document number to QPDS-0139 due to duplicate document numbers Was QPDS-0011 (Revision H, April 2013) (ECO# 10850)	ALL	10/05/18
14395	A	Remove QT76 and QT77 options due to obsolescence of package	ALL	01/13/22
		Update Q-Tech address information (footer)	ALL	