4043B
4044B

QUAD 3-STATE R-S LATCHES: QUAD NOR R-S LATCH-4043B
QUAD NAND R-S LATCH-4044B

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 3-LEVEL OUTPUTS WITH COMMON OUTPUT ENABLE
- SEPARATE SET and RESET INPUT for EACH LATCH
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- NOR and NAND CONFIGURATIONS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4043B, HCC 4044B,** (extended temperature range) and the **HCF 4043B, HCF 4044B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, ceramic flat package, and plastic micropackage. The **HCC/HCF 4043B** types are quad cross-coupled 3-state COS/MOS NOR latches and the **HCC/HCF 4044B** types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD} *	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

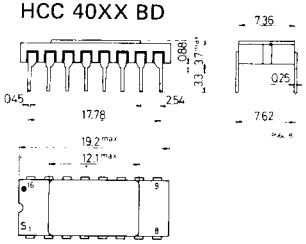
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

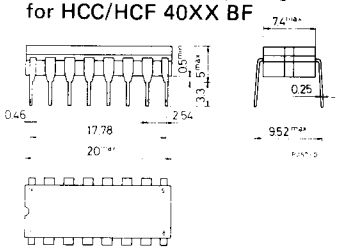
HCC 40XX BD for dual in-line ceramic package
HCC 40XX BF for dual in-line ceramic package, frit seal
HCC 40XX BK for ceramic flat package
HCF 40XX BE for dual in-line plastic package
HCF 40XX BF for dual in-line ceramic package, frit seal
HCF 40XX BM for plastic micropackage

MECHANICAL DATA (dimensions in mm)

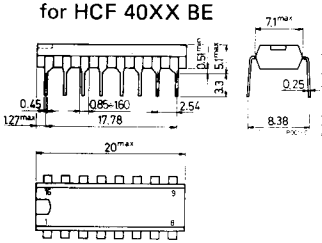
Dual in-line ceramic package
HCC 40XX BD



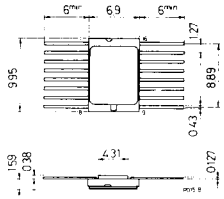
Dual in-line ceramic package
for HCC/HCF 40XX BF



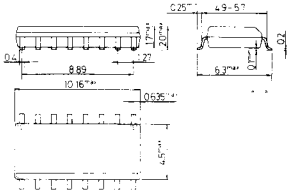
Dual in-line plastic package
for HCF 40XX BE



Ceramic flat package
for HCC 40XX BK

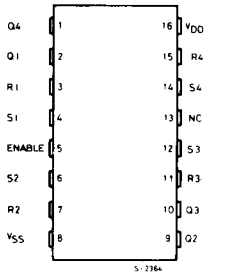


Plastic micropackage
for HCF 40XX BM

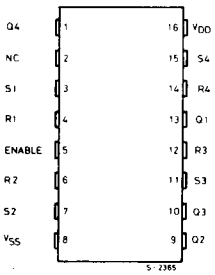


CONNECTION DIAGRAMS

For **4043B**

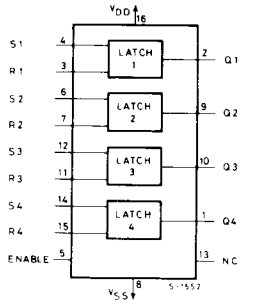


For **4044B**

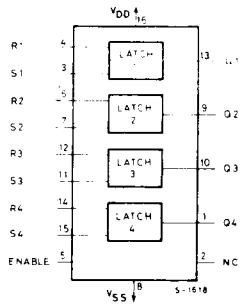


FUNCTIONAL DIAGRAMS

For **4043B**



For **4044B**

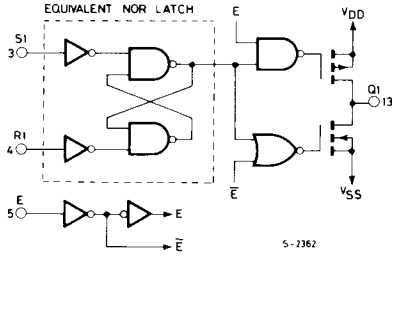


RECOMMENDED OPERATING CONDITIONS

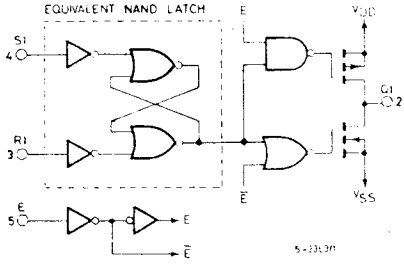
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAMS

For **4043B**

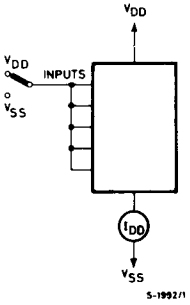


For **4044B**

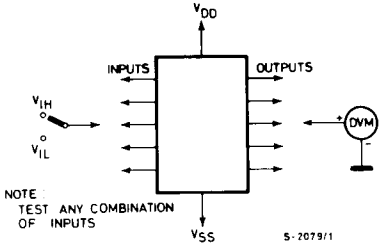


TEST CIRCUITS

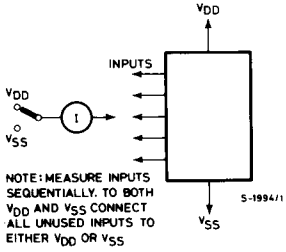
Quiescent device current



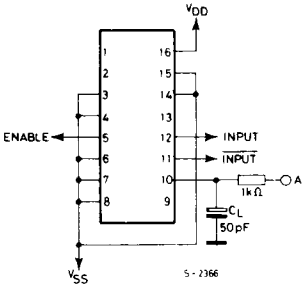
Input voltage



Input current

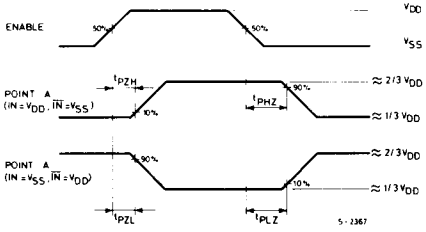


ENABLE propagation delay time and waveforms



TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

Z = HIGH IMPEDANCE



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

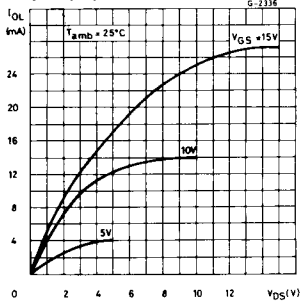
Parameter			Test conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Values T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent current	HCC types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		HCF types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		$\pm$0.1		$\pm 10^{-5}$	$\pm$0.1		$\pm$ 1	μA
		HCF types	0/15			15		$\pm$0.3		$\pm 10^{-5}$	$\pm$0.3		$\pm$ 1	
I_{OH}	3-state output	HCC types	0/18	0/18		18		$\pm$0.4		$\pm 10^{-4}$	$\pm$0.4		$\pm$ 12	μA
		HCF types	0/15	0/15		15		$\pm$1.0		$\pm 10^{-4}$	$\pm$1.0		$\pm$7.5	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

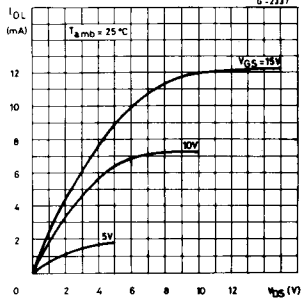
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (SET or RESET to Q)	5		150	300	ns
		10		70	140	
		15		50	100	
t_{PZH}, t_{PHZ}	3-State propagation delay time (ENABLE to Q)	5		115	230	ns
		10		55	110	
		15		40	80	
t_{PLZ} t_{PZL}	Propagation delay time	5		90	180	ns
		10		50	100	
		15		35	70	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_W	Pulse width (SET or RESET)	5	160	80		ns
		10	80	40		
		15	40	20		

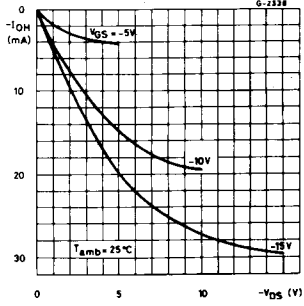
Typical output low (sink) current



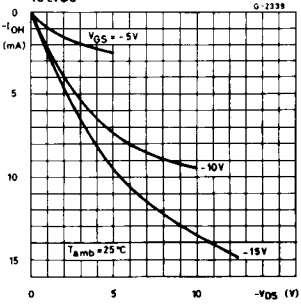
Minimum output low (sink) current characteristics



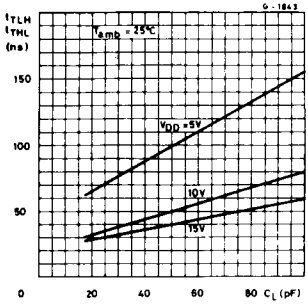
Typical output high (source) current characteristics



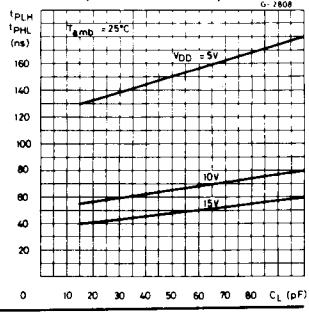
Minimum output high (source) current characteristics



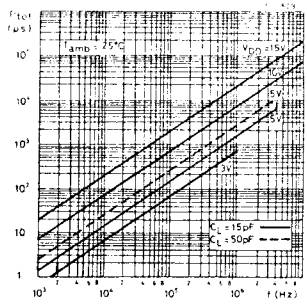
Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance (SET, RESET to Q, $\overline{Q}$)

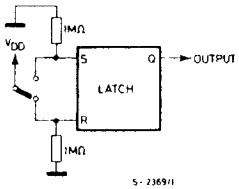


Typical power dissipation/ device vs. frequency

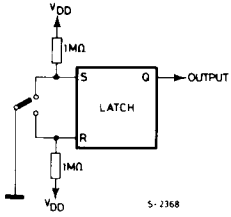


Switch bounce eliminator

for **4043B**



for **4044B**



APPLICATIONS

Multiple bus storage