54F/74F377

Octal D Flip-Flop With Clock Enable

Description

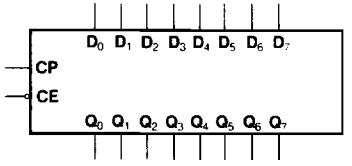
The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

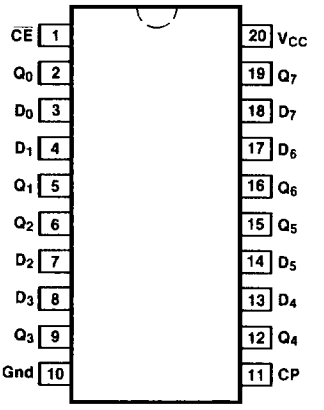
- **Ideal for Addressable Register Applications**
- **Clock Enable for Address and Data Synchronization Applications**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **See 'F273 for Master Reset Version**
- **See 'F373 for Transparent Latch Version**
- **See 'F374 for 3-State Version**

Ordering Code: See Section 5

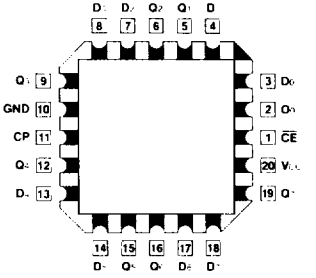
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

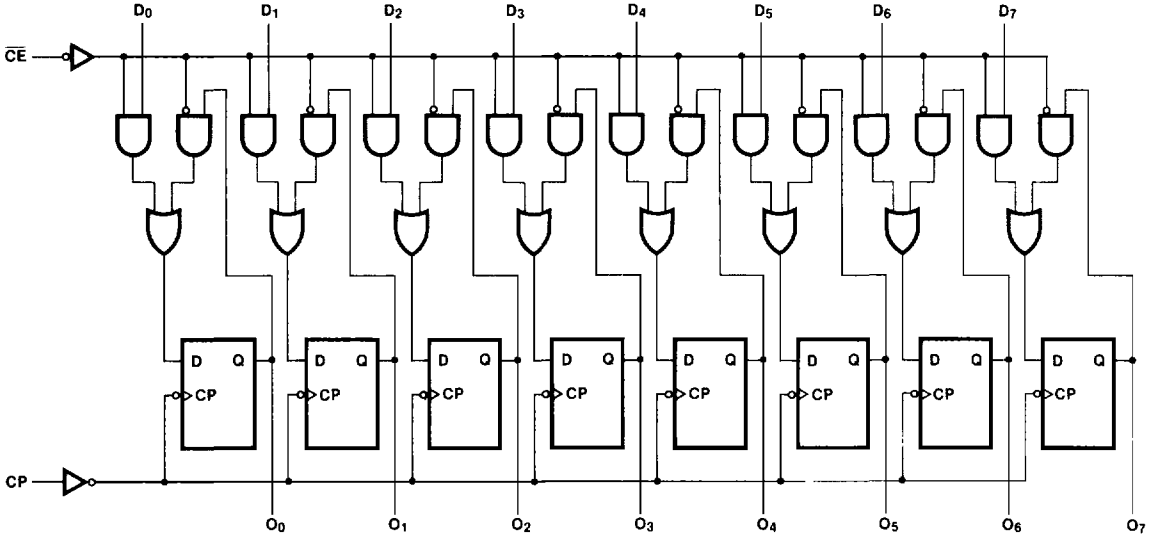
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{CE}$	Clock Enable (Active LOW)	0.5/0.375
Q_0-Q_7	Data Outputs	25/12.5
CP	Clock Pulse Input	0.5/0.375

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		35	50	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			40	60		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		11.0 12.0						ns	3-1 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0							ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.0 1.0							ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.0 3.0							ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CE}$ to CP	1.0 1.0							ns	3-5
$t_w(L)$	Clock Pulse Width, LOW	4.0							ns	3-7