

74F657

Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and 3-STATE Outputs

General Description

The 'F657 contains eight non-inverting buffers with 3-STATE outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA (20 mA mil) at the A port and 64 mA (48 mA mil) at the B port.

- Combines 'F245 and 'F280A functions in one package
- 3-STATE outputs
- B Outputs sink 64 mA (48 mA mil)
- 12 mA source current, B side
- Input diodes for termination effects

Features

- 300 Mil 24-pin slimline DIP

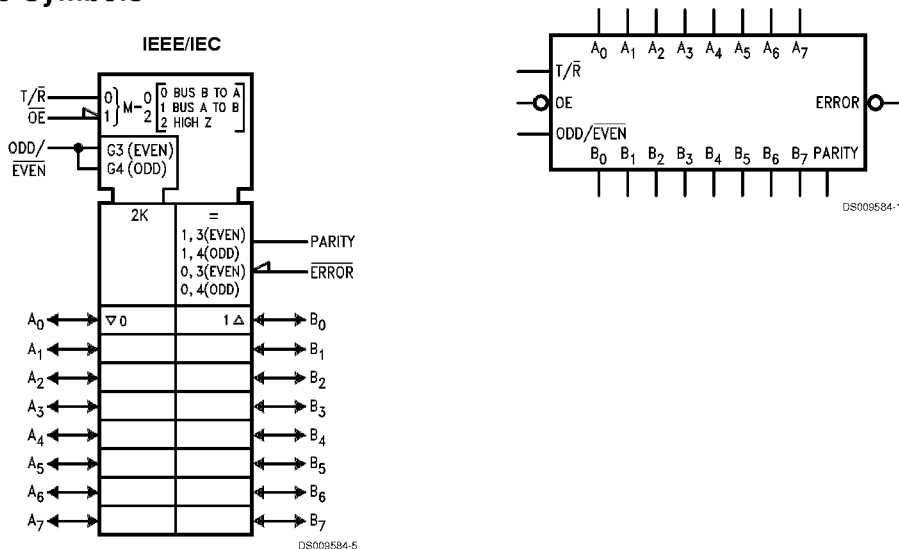
Ordering Code:

Commercial	Military	Package Number	Package Description
74F657SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F657SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
75F657SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F657FM (Note 2)	W24C	24-Lead Cerpack
	54F657LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

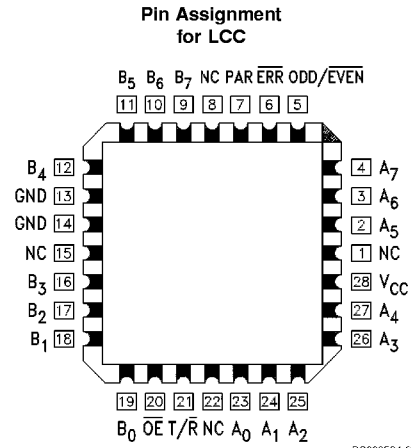
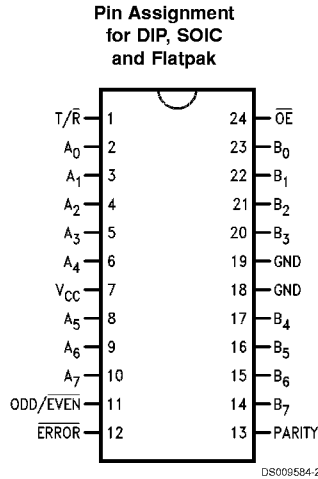
Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



Connection Diagrams



Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0 – A_7	Data Inputs/ 3-STATE Outputs	4.5/0.15 150/40 (33.3)	90 μ A/– 90 μ A –3 mA/24 mA (20 mA)
B_0 – B_7	Data Inputs/ 3-STATE Outputs	3.5/0.117 600/106.6 (80)	70 μ A/–70 μ A –12 mA/64 mA (48 mA)
T/\bar{R}	Transmit/Receive Input	2.0/0.067	40 μ A/–40 μ A
\overline{OE}	Enable Input	2.0/0.067	40 μ A/–40 μ A
PARITY	Parity Input/ 3-STATE Output	3.5/0.117 600/106.6 (80)	70 μ A/–70 μ A –12 mA/64 mA (48 mA)
$\overline{ODD/EVEN}$	$\overline{ODD/EVEN}$ Parity Input	1.0/0.033	20 μ A/–20 μ A
\overline{ERROR}	Error Output	600/106.6 (80)	–12 mA/64 mA (48 mA)

Functional Description

The Transmit/Receive (T/\bar{R}) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable (\overline{OE}) input disables the parity and \overline{ERROR} outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/\bar{R} HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select ($\overline{ODD/EVEN}$). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/\bar{R} LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is

HIGH, then \overline{ERROR} will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the \overline{ERROR} will be LOW indicating an error.

Functional Description (Continued)

Function Table

Number of Inputs That Are High	Inputs			Input/Output	Outputs	
	\overline{OE}	T/R	ODD/EVEN	Parity	ERROR	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

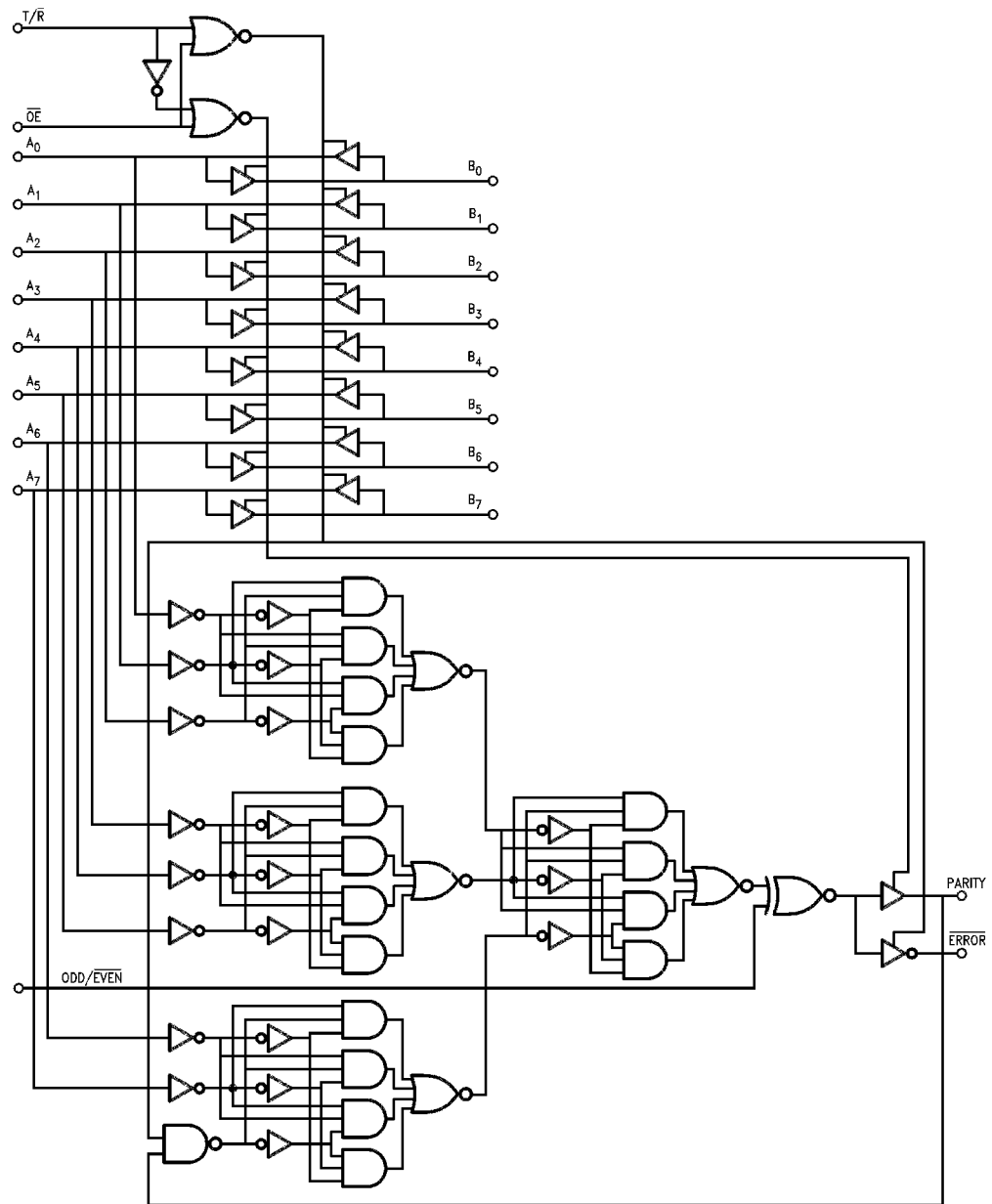
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Function Table

Inputs		Outputs
\overline{OE}	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Functional Block Diagram



2 GROUND PINS
1 V_{CC} PIN

DS009584-4

Absolute Maximum Ratings (Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max)

twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions	
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage						Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage					Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54F 10%V _{CC}	2.5		V	Min	I _{OH} = -1 mA (A _n)	
		54F 10% V _{CC}	2.4				I _{OH} = -3 mA (A _n , B _n , Parity, $\overline{\text{ERROR}}$)	
		54F 10% V _{CC}	2.0				I _{OH} = -12 mA (B _n , Parity, $\overline{\text{ERROR}}$)	
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA (A _n)	
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA (A _n , B _n , Parity, $\overline{\text{ERROR}}$)	
		74F 10% V _{CC}	2.0				I _{OH} = -15 mA (B _n , Parity, $\overline{\text{ERROR}}$)	
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA (A _n)	
V _{OL}	Output LOW Voltage	54F 10% V _{CC}	0.5		V	Min	I _{OL} = 20 mA (A _n)	
		54F 10% V _{CC}	0.55				I _{OL} = 48 mA (B _n , Parity, $\overline{\text{ERROR}}$)	
		74F 10% V _{CC}	0.5				I _{OL} = 24 mA (A _n)	
		74F 10% V _{CC}	0.55				I _{OL} = 64 mA (B _n , Parity, $\overline{\text{ERROR}}$)	
I _{IH}	Input HIGH Current				μA	Max	V _{IN} = 2.7V (ODD/EVEN)	
								V _{IN} = 2.7V (T/R, $\overline{\text{OE}}$)
I _{BVI}	Input HIGH Current Breakdown Test	100			μA	V _{CC} = 0	V _{IN} = 7.0V (T/R, $\overline{\text{OE}}$, ODD/EVEN)	
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	1.0			mA	Max	V _{IN} = 5.5V (Parity, B _n)	
		2.0						V _{IN} = 5.5V (A _n)
I _{IL}	Input LOW Current				μA	Max	V _{IN} = 0.5V (ODD/EVEN)	
								V _{IN} = 0.5V (T/R, $\overline{\text{OE}}$)
I _{OZH}	Output Leakage Current	50			μA	Max	V _{OUT} = 2.7V ($\overline{\text{ERROR}}$)	
I _{OZL}	Output Leakage Current	-50			μA	Max	V _{OUT} = 0.5V ($\overline{\text{ERROR}}$)	
I _{IH} + I _{OZH}	Output Leakage Current	70			μA	Max	V _{I/O} = 2.7V (B _n , Parity)	
		90						V _{I/O} = 2.7V (A _n)
I _{IL} + I _{OZL}	Output Leakage Current	-70			μA	Max	V _{I/O} = 0.5V (B _n , Parity)	
		-90						V _{I/O} = 0.5V (A _n)
I _{OS}	Output Short-Circuit Current	-60	-150		mA	Max	V _{OUT} = 0V (A _n)	
		-100	-225					V _{OUT} = 0V (B _n , Parity, $\overline{\text{ERROR}}$)
I _{CEX}	Output HIGH Leakage Current	250			μA	Max	V _{OUT} = V _{CC} ($\overline{\text{ERROR}}$)	
		1.0						V _{OUT} = V _{CC} (B _n , Parity)
		2.0						V _{OUT} = V _{CC} (A _n)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n , Parity, $\overline{\text{ERROR}}$)
I _{CCH}	Power Supply Current		101	125	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		112	150	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		109	145	mA	Max	V _O = HIGH Z

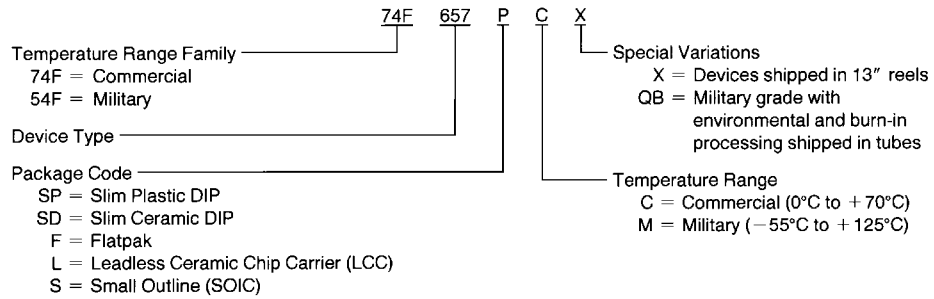
AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	4.5	8.0	2.5	9.5	2.5	9.0	ns
t _{PHL}	A _n to B _n , B _n to A _n	3.0	4.9	7.5	3.0	8.5	3.0	8.0	
t _{PLH}	Propagation Delay	6.5	10.1	14.0	5.5	18.0	6.0	16.0	ns
t _{PHL}	A _n to Parity	7.0	10.9	15.0	5.5	20.5	6.0	16.5	
t _{PLH}	Propagation Delay	4.5	7.8	11.0	4.0	14.0	4.0	13.0	ns
t _{PHL}	ODD/EVEN to PARITY	4.5	8.8	12.0	4.5	16.5	4.5	13.5	
t _{PLH}	Propagation Delay	4.5	7.5	11.0	4.0	14.0	4.0	13.0	ns
t _{PHL}	ODD/EVEN to $\overline{\text{ERROR}}$	4.5	8.2	12.0	4.5	16.5	4.5	13.5	
t _{PLH}	Propagation Delay	8.0	14.0	20.5	7.5	27.0	7.5	23.0	ns
t _{PHL}	B _n to $\overline{\text{ERROR}}$	8.0	15.0	21.5	7.5	28.5	7.5	23.5	
t _{PLH}	Propagation Delay	7.0	10.8	15.5	6.0	20.0	6.0	17.0	ns
t _{PHL}	PARITY to $\overline{\text{ERROR}}$	7.5	11.8	16.5	6.5	22.0	7.5	18.5	
t _{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t _{PZL}	$\overline{\text{OE}}$ to A _n /B _n	4.0	6.5	10.0	3.5	13.5	3.5	11.0	
t _{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t _{PLZ}	$\overline{\text{OE}}$ to A _n /B _n	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t _{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t _{PZL}	$\overline{\text{OE}}$ to $\overline{\text{ERROR}}$ (Note 5)	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t _{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t _{PLZ}	$\overline{\text{OE}}$ to $\overline{\text{ERROR}}$	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t _{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t _{PZL}	$\overline{\text{OE}}$ to PARITY	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t _{PHZ}	Output Disable Time	1.0	4.6	8.0	1.0	9.5	1.0	9.0	ns
t _{PLZ}	$\overline{\text{OE}}$ to PARITY	1.0	5.1	7.5	1.0	8.5	1.0	8.0	

Note 5: These delay times reflect the 3-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable times). VALID data at the $\overline{\text{ERROR}}$ pin \geq (A to PARITY) + (Output Enable Time).

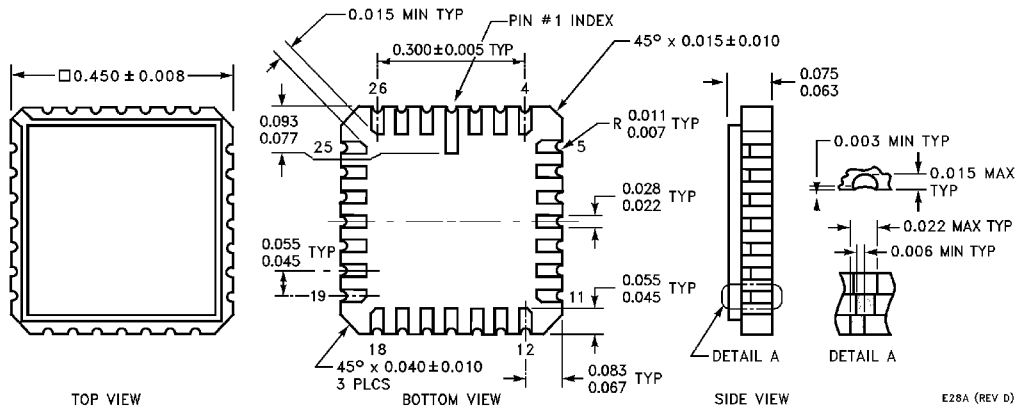
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



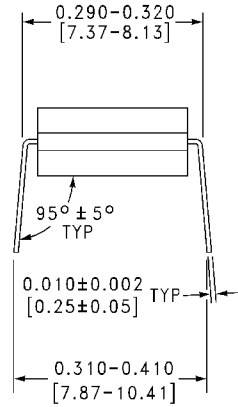
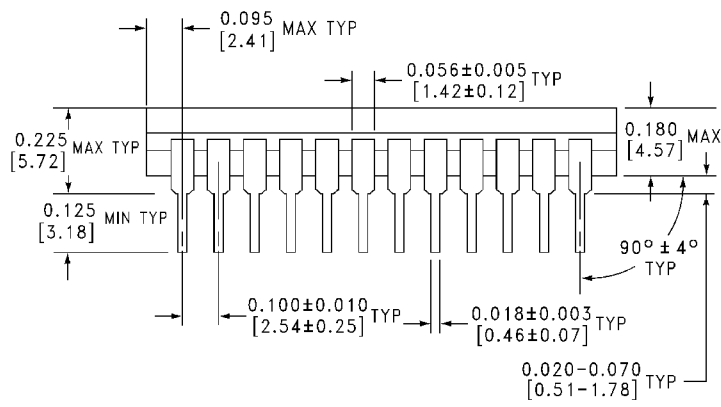
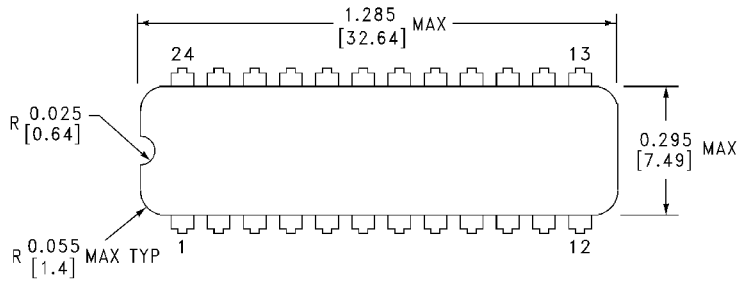
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Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Ceramic Leadless Chip Carrier (L)
Package Number E28A

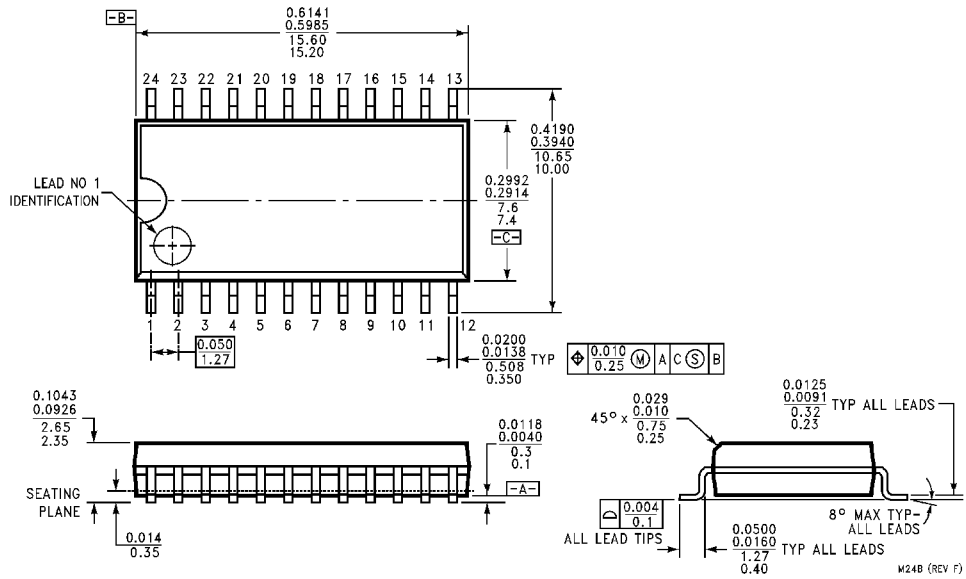
E28A (REV D)



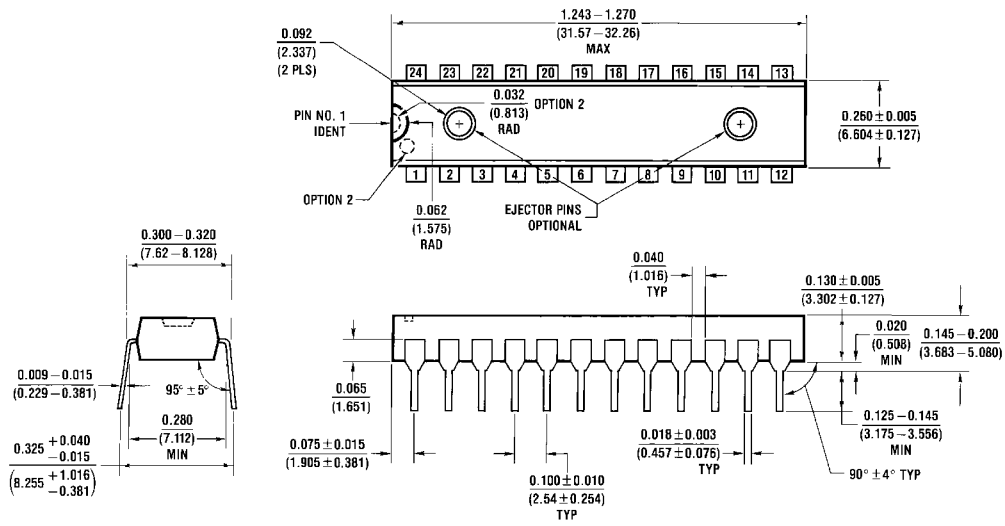
24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
Package Number J24F

J24F (REV. H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

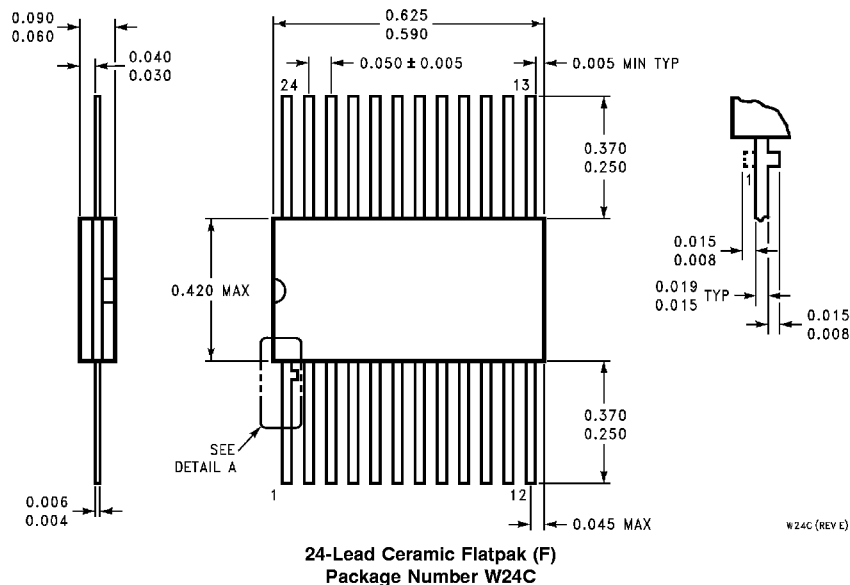


**24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M24B**



**24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
Package Number N24C**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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