ML6516444

16-Bit Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The ML6516444 is a BiCMOS, 16-bit buffer/line driver with 3-state outputs. This device was specifically designed for high speed bus applications. Its 16 channels support propagation delay of 2.5ns maximum, and fast output enable and disable times of 8.0ns or less to minimize datapath delay.

This device is designed to minimize undershoot, overshoot, and ground bounce to decrease noise delays. These transceivers implement a unique digital and analog implementation to eliminate the delays and noise inherent in traditional digital designs. The device offers a new method for quickly charging up a bus load capacitor to minimize bus settling times, or FastBus™ Charge. FastBus Charge is a transition current, (specified as $I_{DYNAMIC}$) that injects between 60 to 200mA (depending on output load) of current during the rise time and fall time. This current is used to reduce the amount of time it takes to charge up a heavily-capacitive loaded bus, effectively reducing the bus settling times, and improving data/clock margins in tight timing budgets.

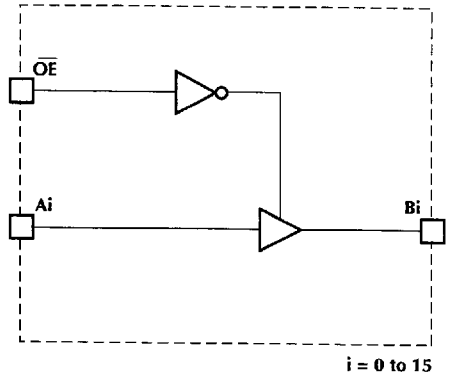
Micro Linear's solution is intended for applications for critical bus timing designs that include minimizing device propagation delay, bus settling time, and time delays due to noise. Applications include; high speed memory arrays, bus or backplane isolation, bus to bus bridging, and sub-2.5ns propagation delay schemes.

The ML6516444 follows the pinout and functionality of the industry standard 3.3V-logic families.

FEATURES

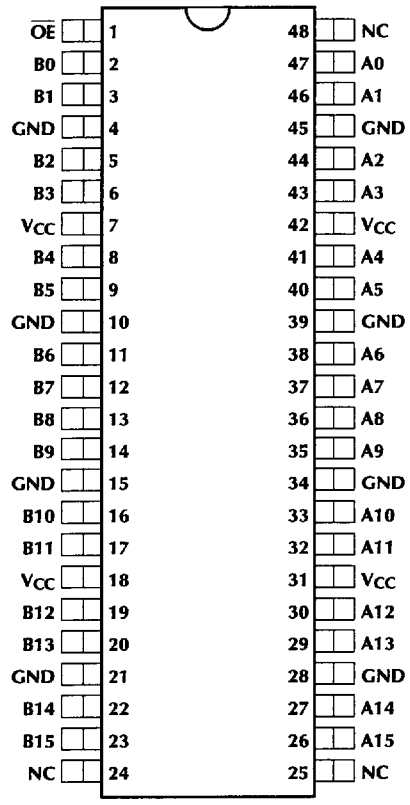
- Low propagation delays — 2.5ns maximum for 3.3V
  2.25ns maximum for 5.0V
- Fast output enable/disable times of 8.0ns maximum
- FastBus Charge current to minimize the bus settling time during active capacitive loading
- 3.0 to 3.6V and 4.5 to 5.5V V_{CC} supply operation; LV-TTL compatible input and output levels with 3-state capability
- Industry standard pinout compatible to FCT, ALV, LCX, LVT, and other low voltage logic families
- ESD protection exceeds 2000V
- Full output swing for increased noise margin
- Undershoot and overshoot protection to 400mV typically
- Low ground bounce design

BLOCK DIAGRAM



PIN CONFIGURATION

ML6516444
48-Pin SSOP (R48)
48-Pin TSSOP (T48)



TOP VIEW

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	Ai	Bi
L	H	H
L	L	L
H	X	Z

L = Logic Low, H = Logic High, X = Don't Care, Z = High Impedance
i = 0 to 15

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable
2	B0	Data Output
3	B1	Data Output
4	GND	Signal Ground
5	B2	Data Output
6	B3	Data Output
7	V_{CC}	3.3V or 5.0V Supply
8	B4	Data Output
9	B5	Data Output
10	GND	Signal Ground
11	B6	Data Output
12	B7	Data Output
13	B8	Data Output
14	B9	Data Output
15	GND	Signal Ground
16	B10	Data Output
17	B11	Data Output
18	V_{CC}	3.3V or 5.0V Supply
19	B12	Data Output
20	B13	Data Output
21	GND	Signal Ground
22	B14	Data Output
23	B15	Data Output
24	NC	No Connect
25	NC	No Connect
26	A15	Data Input
27	A14	Data Input
28	GND	Signal Ground
29	A13	Data Input
30	A12	Data Input
31	V_{CC}	3.3V or 5.0V Supply
32	A11	Data Input
33	A10	Data Input
34	GND	Signal Ground
35	A9	Data Input
36	A8	Data Input
37	A7	Data Input
38	A6	Data Input
39	GND	Signal Ground
40	A5	Data Input
41	A4	Data Input
42	V_{CC}	3.3V or 5.0V Supply
43	A3	Data Input
44	A2	Data Input
45	GND	Signal Ground
46	A1	Data Input
47	A0	Data Input
48	NC	Output Enable Active High

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 7V
DC Input Voltage ..... –0.3V to V_{CC} + 0.3V
AC Input Voltage (PW < 20ns) ..... –3.0V
DC Output Voltage ..... –0.3V to 7VDC
Output Current, Source or Sink 180mA

Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10sec) ..... 150°C
Thermal Impedance (θ_{JA}) ..... 76°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
V_{IN} Operating Range ..... 3.0V to 5.5V

ELECTRICAL CHARACTERISTICS – 3.3V OPERATION

Unless otherwise specified, V_{IN} = 3.3V, T_A = Operating Temperature Range (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF)						
t_{PHL}, t_{PLH}	Propagation Delay	Ai to Bi	1.8	2.1	2.5	ns
t_{OE}	Output Enable Time	OE to Ai			8.0	ns
t_{OD}	Output Disable Time	OE to Ai			8.0	ns
T_{OS}	Output-to-Output Skew				500	ps
C_{IN}	Input Capacitance				5	pF
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = Open)						
V_{IH}	Input High Voltage	Logic high	2.0			V
V_{IL}	Input Low Voltage	Logic low			0.8	V
I_{IH}	Input High Current	Per pin, V_{IN} = 3V			300	µA
I_{IL}	Input Low Current	Per pin, V_{IN} = 0V			300	µA
I_{HI-Z}	Three-State Output Current	V_{CC} = 3.6V, 0 < V_{IN} < V_{CC}			5	µA
V_{IC}	Input Clamp Voltage	V_{CC} = 3.6V, I_{IN} = 18mA		–0.7	–0.2	V
$I_{DYNAMIC}$	Dynamic Transition Current (FastBus Charge)	Low to high transitions		80		mA
		High to low transitions		80		mA
V_{OH}	Output High Voltage	V_{CC} = 3.6V, I_{OH} = –2mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 3.6V, I_{OL} = 2mA			0.6	V
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, f = 0Hz, inputs = V_{CC} or 0V			3	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

ELECTRICAL CHARACTERISTICS – 5V OPERATION

Unless otherwise specified, V_{IN} = 5V, T_A = Operating Temperature Range (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF)						
t_{PHL}, t_{PLH}	Propagation Delay	Ai to Bi	1.6	1.9	2.25	ns
t_{OE}	Output Enable Time	OE to Ai/Bi			8.0	ns
t_{OD}	Output Disable Time	OE to Ai			8.0	ns
T_{OS}	Output-to-Output Skew				500	ps
C_{IN}	Input Capacitance				5	pF
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = Open)						
V_{IH}	Input High Voltage	Logic high	3.6			V
V_{IL}	Input Low Voltage	Logic low			0.8	V
I_{IH}	Input High Current	Per pin, V_{IN} = 4.5V			300	µA
I_{IL}	Input Low Current	Per pin, V_{IN} = 0V			300	µA
I_{HI-Z}	Three-State Output Current	V_{CC} = 5.5V, 0 < V_{IN} < V_{CC}			5	µA
V_{IC}	Input Clamp Voltage	V_{CC} = 5.5V, I_{IN} = 18mA		–0.7	–0.2	V
$I_{DYNAMIC}$	Dynamic Transition Current (FastBus Charge)	Low to high transitions		120		mA
		High to low transitions		120		mA
V_{OH}	Input Clamp Voltage	V_{CC} = 5.5V, I_{OH} = –2mA	4.5			V
V_{OL}	Input Clamp Voltage	V_{CC} = 5.5V, I_{OL} = 2mA			1.2	V
I_{CC}	Quiescent Power Supply Current	V_{CC} = 5.5V, f = 0Hz, inputs = V_{CC} or 0V			3	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

PERFORMANCE DATA 3.3V OPERATION

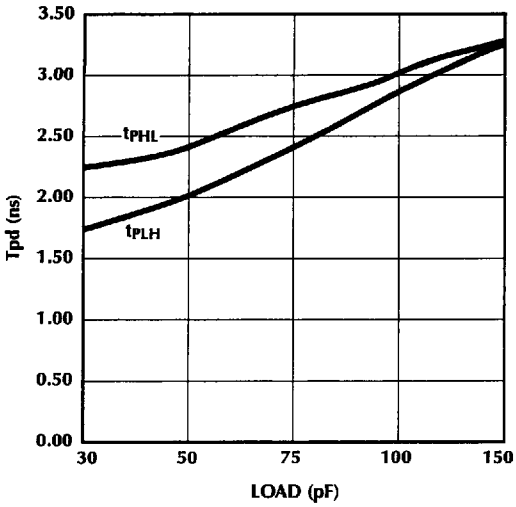


Figure 1. Propagation Delay over Load Capacitance: 30 to 150pF, $V_{CC} = V_{IN} = 3.3V$, 20MHz

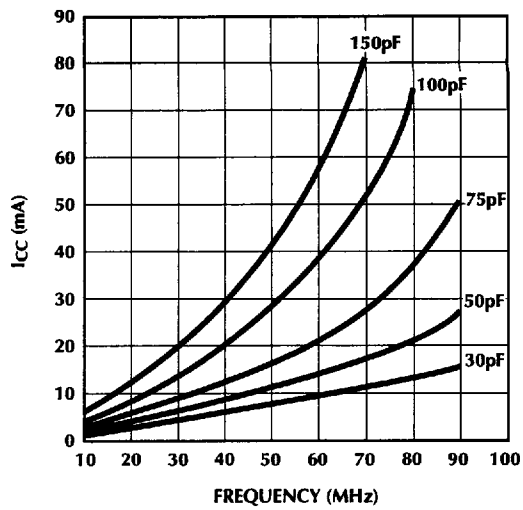


Figure 2. I_{CC} vs. Frequency (10 to 100 MHz) over Load, $V_{CC} = V_{IN} = 3.3V$

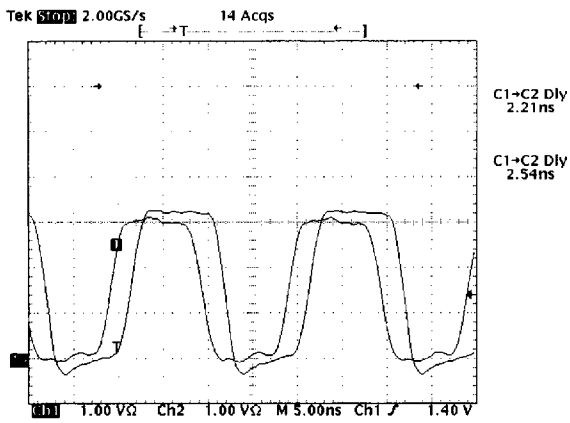


Figure 3. Ground Bounce: $V_{CC} = V_{IN} = 3.0V$ V_{IN}: $t_{RISE} = t_{FALL} = 2ns$

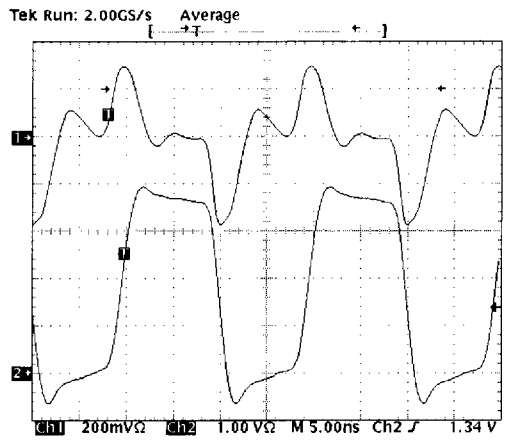


Figure 4. $I_{DYNAMIC}$ Current (FastBus Charge): $V_{CC} = V_{IN} = 3.3V$, 50pF load, 40mA/DIV, V_{IN}: $t_{RISE} = t_{FALL} = 2ns$

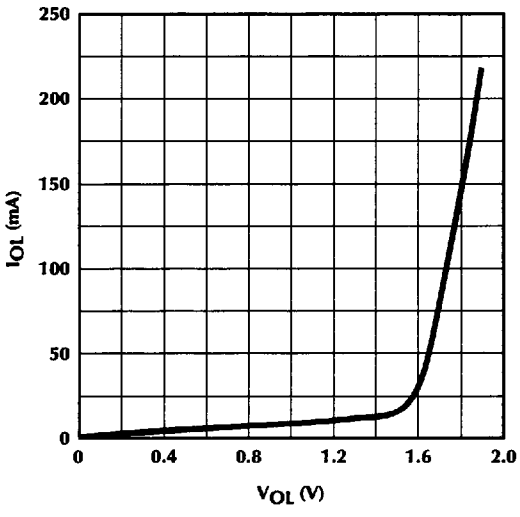


Figure 5a. Typical V_{OL} vs. I_{OL} for One Buffer Output

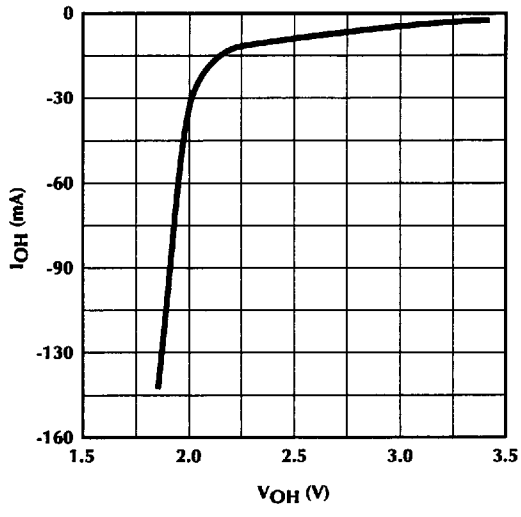


Figure 5b. Typical V_{OH} vs. I_{OH} for One Buffer Output

PERFORMANCE DATA 5.0V OPERATION

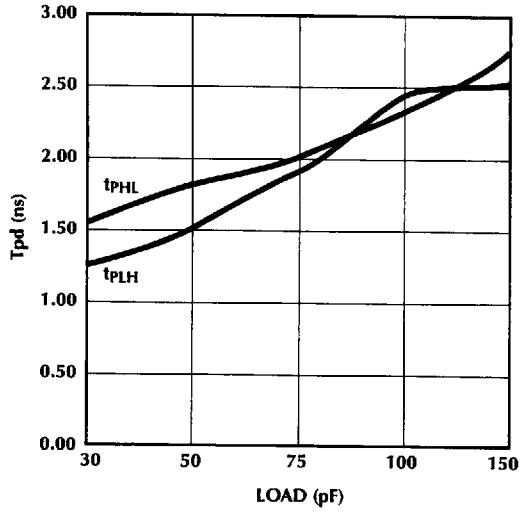


Figure 6. Propagation Delay over Load Capacitance: 30 to 150pF, $V_{CC} = V_{IN} = 5.0V$, 20MHz

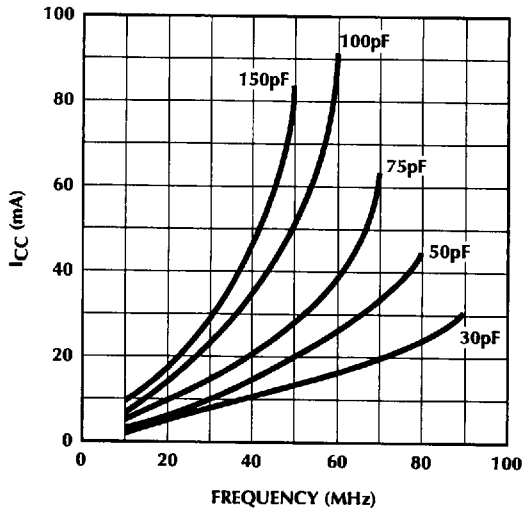


Figure 7. I_{CC} vs. Frequency (10 to 100 MHz) over Load, $V_{CC} = V_{IN} = 5.0V$

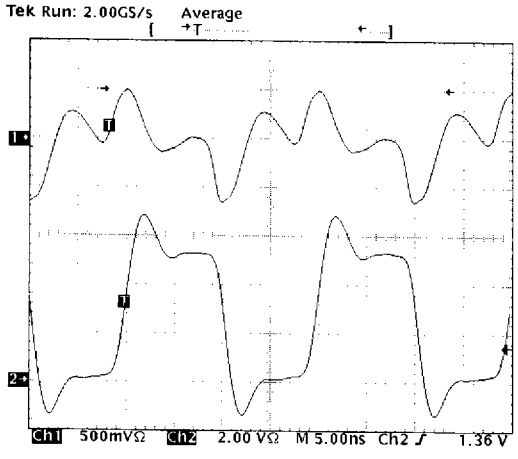


Figure 8. $I_{DYNAMIC}$ Current (FastBus Charge): $V_{CC} = V_{IN} = 5.0V$, 50pF load, 100mA/DIV, V_{IN}: $t_{RISE} = t_{FALL} = 2ns$

FUNCTIONAL DESCRIPTION

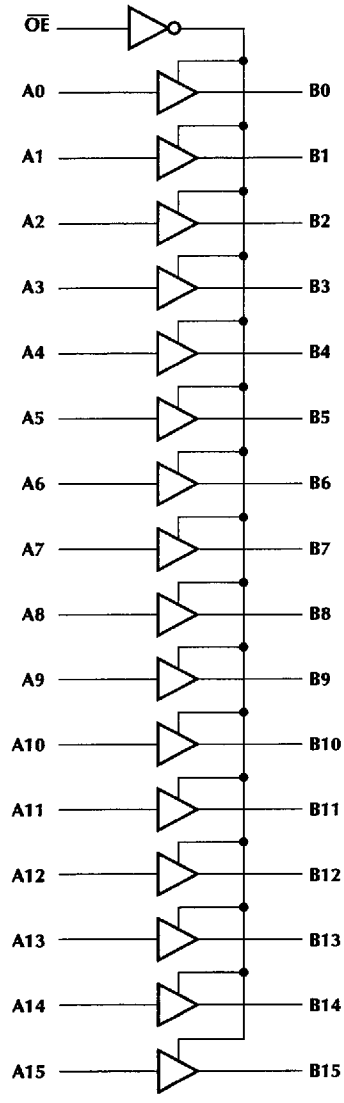


Figure 9. Logic Diagram

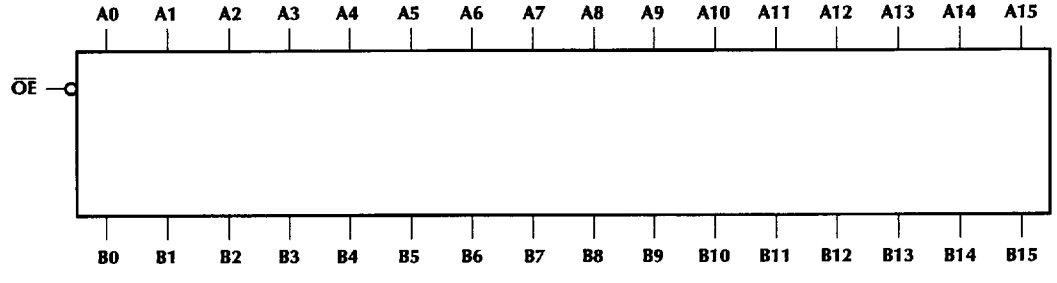


Figure 10. Logic Symbol

ARCHITECTURAL DESCRIPTION

The ML6516444 is a 16-bit buffer/line driver with 3-state outputs designed for 3.0V to 3.6V and 4.5V to 5.5V V_{CC} operation. This device is designed for 16-bit word memory interleaving operations. All the buffers are controlled via a 3-state output enable pin with output enable/disable access times of less than 8.0ns.

Until now, these transceivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these 16-bit CMOS buffers has managed to drive 50pF load capacitance with a delay of 3.6ns.

Micro Linear has produced a 16-bit buffer/line driver with a delay less than 2.5ns by using a unique circuit architecture that does not require cascade logic gates.

The basic architecture of the ML6516444 is shown in Figure 11. In this circuit, there are two paths to the output. One path sources current to the load capacitance where the signal is asserted, and the other path sinks current from the output when the signal is negated.

The assertion path is the Darlington pair consisting of transistors Q1 and Q2. The effect of transistor Q1 is to increase the current gain through the stage from input to output, to increase the input resistance and to reduce input capacitance. During an input low-to-high transition, the output transistor Q2 sources large amount of current to quickly charge up a highly capacitive load which in effect reduces the bus settling time. This current is specified as $I_{DYNAMIC}$.

The negation path is also the Darlington pair consisting of transistor Q3 and transistor Q4. With M1 connecting to the input of the Darlington pair, Transistor Q4 then sinks a large amount of current during the input transition from high-to-low.

Inverter X2 is a helpful buffer that not only drives the output toward the upper rail but also pulls the output to the lower rail.

There are a number of MOSFETs not shown in Figure 3. These MOSFETs are used to 3-state the buffers. For instance, R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines of which they are connected.

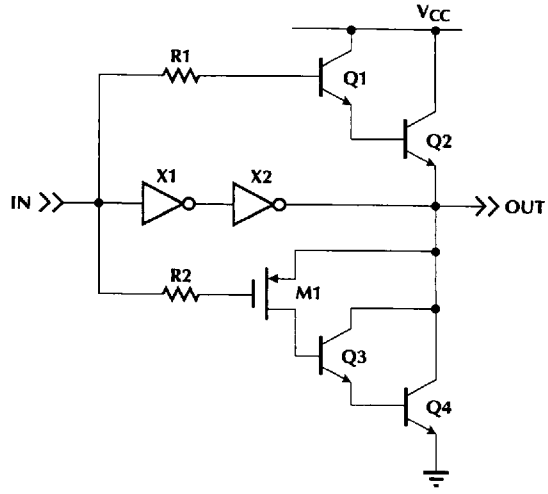


Figure 11. One Buffer Cell of the ML6516444

CIRCUITS AND WAVE FORMS

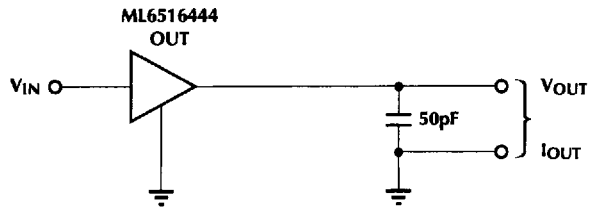


Figure 12. Test circuits for All Outputs

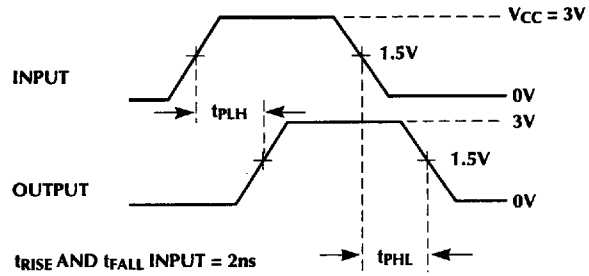


Figure 13. Propagation Delay

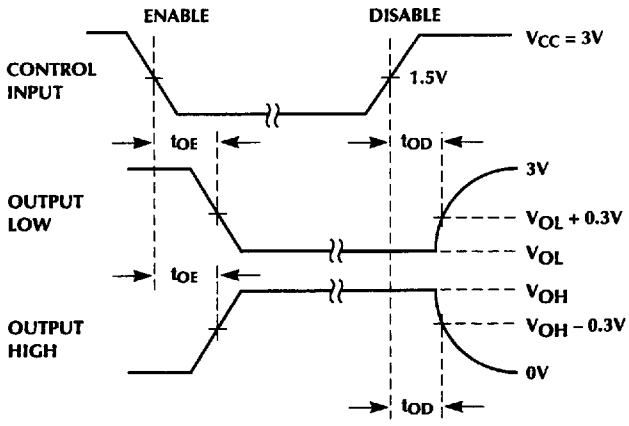


Figure 14. Enable and Disable Times

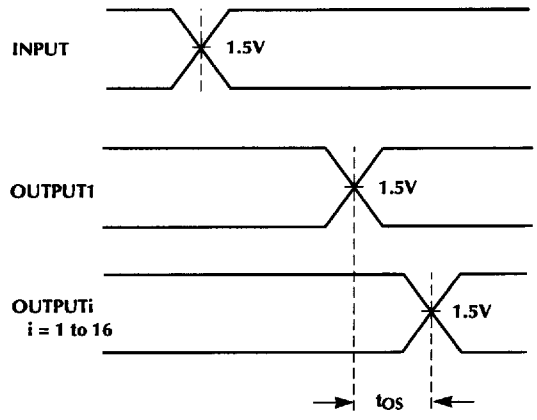
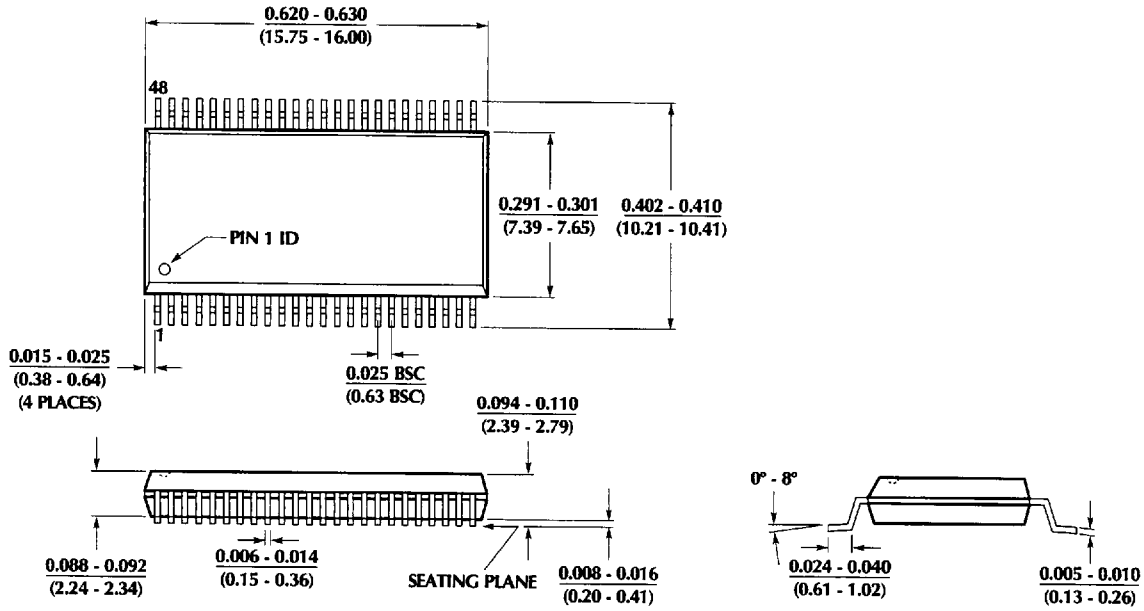


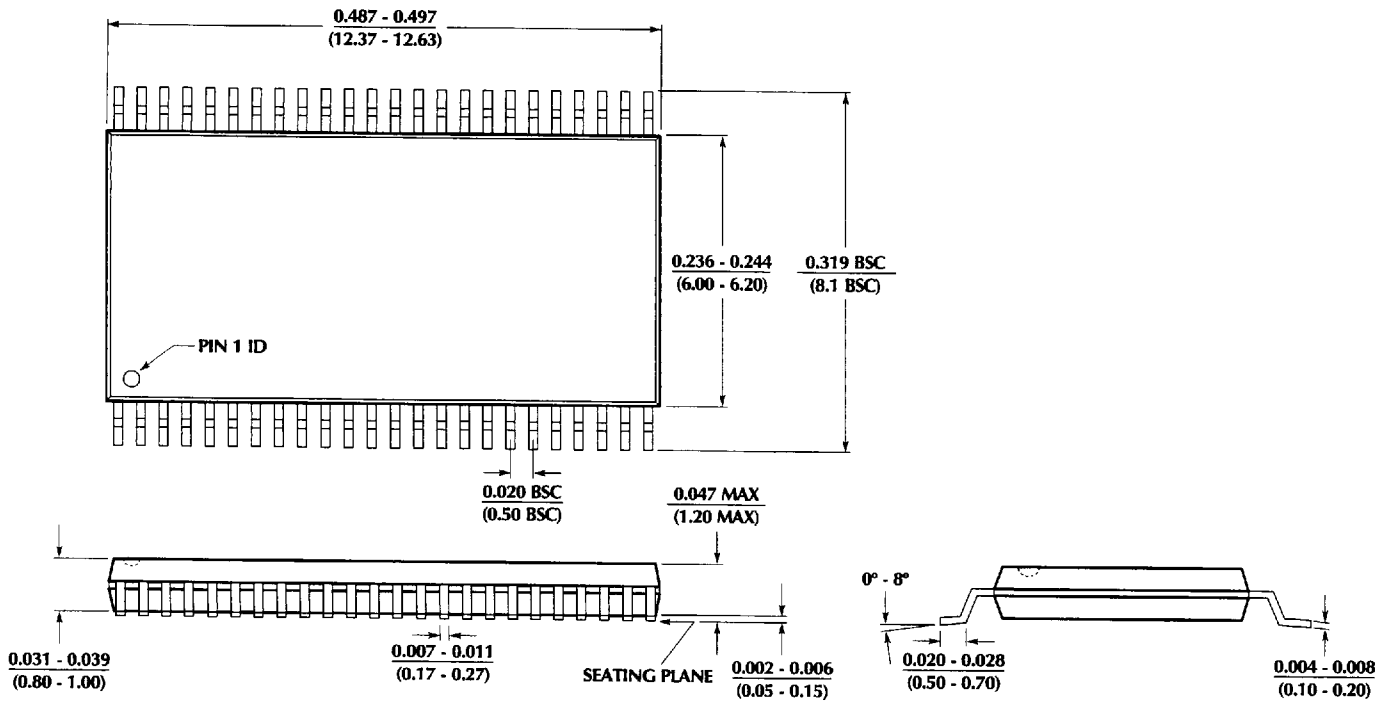
Figure 15. Output Skew

PHYSICAL DIMENSIONS inches (millimeters)

Package: R48
48-Pin SSOP



Package: T48
48-Pin TSSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6516444CR	0°C to 70°C	48-Pin SSOP (R48)
ML6516444CT	0°C to 70°C	48-Pin TSSOP (T48)

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