■ Mask ROMs

Process	Capacity	Configuration (words x bits)	* Pinout	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MIN.	Supply current (mA) MAX.	Supply voltage (V)	Package
CMOS	256k	32k x 8	J	**LH53259D/N/T**	LH5359XX	150	25	5 ± 10%	28DIP/28SOP/28TSOP(I) Forward bend
	512k	64k x 8	J	**LH53517D/N/T/TR**	LH5317XX	150	30	5 ± 10%	28DIP/28SOP/28TSOP(I)
	1M	128k x 8	J	**LH531V00D/N/T/U**	LH531VXX	100	75	5 ± 10%	32DIP/32SOP/32TSOP(I) Forward bend/32QFJ
			J	**LH53V1R00N/T**	LH5V1RXX	120	30	2.7 to 3.6	32SOP/32TSOP(I) Forward bend
			J	**LH530800AD/AN/AU**	LH531HXX	150	35	5 ± 10%	32DIP/32SOP/32QFJ
			J	**LH530800AD/AN-Y**	LH531YXX	500*3 150*2	12*5	2.6 to 5.5	32DIP/32SOP
			M	**LH531000BD/BN**	LH531GXX	150	35	5 ± 10%	28DIP/28SOP
			M	**LH531000BN-S**	LH531MXX	500	18	2.6 to 3.6	28SOP
		64k x 16	J	**LH531024D/N/U**	LH531CXX	100	75	5 ± 10%	40DIP/40SOP/44QFJ
	2M	256k x 8	J	**LH532100BD/BN/BT/BS/BSR/BU-1**	LH532KXX	120	50	5 ± 10%	32DIP/32SOP/32TSOP(I) Foward bend/32TSOP(II)/32QFJ
			J	**LH532100BD/BN/BT/BS/BSR/BU**	LH532KXX	150	50	5 ± 10%	32DIP/32SOP/32TSOP(I) Foward bend/32TSOP(II)/32QFJ
		128k x 16	J	**LH532048D/N/U**	LH532CXX	100	75	5 ± 10%	40DIP/40SOP/44QFJ
		256k x 8 128k x 16	M	**LH532600D/N/T/TR**	LH5326XX	100	75	5 ± 10%	40DIP/40SOP/48TSOP(I)
			M	**LH53V2P00N/T**	LH5V2PXX	120	35	2.7 to 3.6	40SOP/48TSOP(I) Foward bend
			M	**LH532000BD/BN/BT/BTR-1**	LH532GXX	120	50	5 ± 10%	40DIP/40SOP/48TSOP(I)
			M	**LH532000BD/BN/BT/BTR**	LH532GXX	150	50	5 ± 10%	40DIP/40SOP/48TSOP(I)
			M	**LH532000BD/BN/BT/BTR-S**	LH532SXX	500*3 150*2	15*5	2.6 to 5.5	40DIP/40SOP/48TSOP(I)
	4M	512k x 8	J	**LH53H4100D/N**	LH5H41XX	80	90	5 ± 10%	32DIP/32SOP
			J	**LH534700D/N**	LH5S47XX	100	75	5 ± 10%	32DIP/32SOP
			J	**LH534R00AD/AN/AS/ASR**	LH5347XX	120	65	5 ± 10%	32DIP/32SOP/32TSOP(II)
			F	**LH534A00T**	LH5S4AXX	120	65	5 ± 10%	32TSOP(I) Foward bend
			F	**LH534B00T**	LH5S4BXX	120	60	5 ± 10%	40TSOP(I) Foward bend
		256k x 16	J	**LH534Y00D/U**	LH534YXX	120	65	5 ± 10%	40DIP/44QFJ
		512k x 8 256k x 16	M	**LH53H4000D/N**	LH5H40XX	80	90	5 ± 10%	40DIP/40SOP
			M	**LH534600BD/BN/BT/BTR**	LH534VXX	100	75	5 ± 10%	40DIP/40SOP/48TSOP(I)
			M	**LH534P00AD/AN/AT/ATR**	LH5348XX	120	65	5 ± 10%	40DIP/40SOP/48TSOP(I)
			M	**LH53B4P00D/N*1**	LH5B4PXX	120[50]	100	5 ± 10%	40DIP/40SOP
			M	**★LH53V4P00N/T**	LH5V4PXX	120	35	2.7 to 3.6	40SOP/48TSOP(I) Forward bend
			M	**LH534000BD/BN/BT-S**	LH534SXX	500*3 200*2	15*5	2.6 to 5.5	40DIP/40SOP/48TSOP(I) Foward bend
	8M	1M x 8	J	**★LH538700AD/AN/AS**	LH538VXX	100	100	5 ± 10%	32DIP/32SOP/32TSOP(II) Foward bend
			J	**LH538R00BD/BN/BS/BSR**	LH5387XX	120	60	5 ± 10%	32DIP/32SOP/32TSOP(II)
			J	**LH538300CD/CN/CS/CSR**	LH538NXX	150	50	5 ± 10%	32DIP/32SOP/32TSOP(II)

★ Under development

Process	Capacity	Configuration (words x bits)	※ Pinout	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MIN.	Supply current (mA) MAX.	Supply voltage (V)	Package
CMOS	8M	1M x 8 512k x 16	M	**LH53B8P00AD/AN**[*1]	LH5B8GXX	120[50]	100	5 ± 10%	42DIP/44SOP
			M	**LH538600AD/AN/AT**	LH538UXX	100	100	5 ± 10%	42DIP/44SOP/48TSOP(I) Forward bend
			M	**LH538P00BD/BN/BT/BTR**	LH5388XX	120	60	5 ± 10%	42DIP/44SOP/48TSOP(I)
			M	**LH538500CD/CN/CT/CTR**	LH538BXX	150	50	5 ± 10%	42DIP/44SOP/48TSOP(I)
			M	**LH53V8000D/N/T/TR**	LH5V80XX	200[*4] 100[*2]	35[*6]	3.0 to 5.5	42DIP/44SOP/48TSOP(I)
	16M	2M x 8 1M x 16	M	★**LH53B16P00D/N**[*1]	LH5B7PXX	120[50]	100	5 ± 10%	42DIP/44SOP
			M	**LH53C16P00D/N**[*1]	LH5C7PXX	120[60]	150	5 ± 10%	42DIP/44SOP
			M	**LH53B16500D/N**[*1]	LH5B75XX	150[70]	80	5 ± 10%	42DIP/44SOP
			M	**LH5316600D/N**	LH5376XX	100	100	5 ± 10%	42DIP/44SOP
			M	**LH5316P00CD/CN**	LH5372XX	120	70	5 ± 10%	42DIP/44SOP
			M	**LH5316P00CT/CTR**	LH537DXX	120	70	5 ± 10%	48TSOP(I)
			M	**LH5316500CD/CN**	LH5370XX	150	50	5 ± 10%	42DIP/44SOP
			M	**LH53V16500N/T**	LHMV75XX	150	35	2.7 to 3.6	44SOP/48TSOP(I) Forward bend
		1M x 16 512 x 32	M	**LH53B16R00N** [*1]	LH5B7RXX	120[50]	180	5 ± 10%	70SSOP
	24M	3M x 8	M	**LH5324000D**	LH5360XX	150	70	5 ± 10%	42DIP
		1.5M x 16	M	**LH5324C00D**	LH536CXX	120	80	5 ± 10%	42DIP
			M	**LH5324A00AD**	LH536GXX	150	65	5 ± 10%	42DIP
		3M x 8 1.5M x 16	M	**LH5324P00N**	LH536PXX	120	80	5 ± 10%	44SOP
			M	★**LH5324P00T/TR**	LH536DXX	120	80	5 ± 10%	48TSOP(I)
			M	**LH5324500N**	LH5365XX	150	70	5 ± 10%	44SOP
	32M	2M x 16	M	**LH5332C00D**	LHMN5CXX	120	80	5 ± 10%	42DIP
			M	**LH5332A00D**	LH535AXX	150	65	5 ± 10%	42DIP
		4M x 8 2M x 16	M	**LH5332600N**	LHMN56XX	100	100	5 ± 10%	44SOP
			M	**LH5332600T**	LHMN5FXX	100	100	5 ± 10%	48TSOP(I) Forward bend
			M	**LH5332P00N**	LHMN5PXX	120	80	5 ± 10%	44SOP
			M	**LH5332P00T/TR**	LHMN5DXX	120	80	5 ± 10%	48TSOP(I)
			M	**LH5332500AN**	LH535FXX	150	65	5 ± 10%	44SOP
			M	**LH53V32500N**	LHMV55XX	150	35	2.7 to 3.6	44SOP
			M	**LH53V32500T/TR**	LHMV5BXX	150	35	2.7 to 3.6	48TSOP(I)
	64M	8M x 8 4M x 16	M	**LH5364000N**	LHMN00XX	150	100	5 ± 10%	44SOP

※ J : JEDEC standard EPROM pinout M : MASK ROM specific pinout F : Flash Memory compatible pinout

*1 With Page mode. Figures in brackets indicate access time during page mode.
*2 4.5 V≦Vcc≦5.5 V
*3 2.6 V≦Vcc< 4.5 V
*4 3.0 V≦Vcc< 4.5 V
*5 2.6 V≦Vcc≦3.4 V
*6 3.0 V≦Vcc≦3.6 V

T : TSOP(Type I) Forward bend TR : TSOP(Type I) Reverse bend
S : TSOP(Type II) Forward bend SR : TSOP(Type II) Reverse bend
QFJ = PLCC