

# MC74VHC1G08

## 2-Input AND Gate

The MC74VHC1G08 is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G08 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G08 to be used to interface 5V circuits to 3V circuits.

- High Speed:  $t_{PD} = 3.5ns$  (Typ) at  $V_{CC} = 5V$
- Low Power Dissipation:  $I_{CC} = 2\mu A$  (Max) at  $T_A = 25^\circ C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

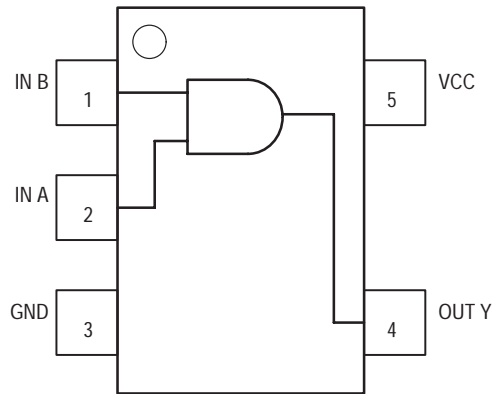
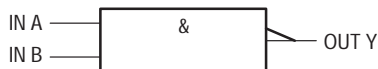


Figure 1. 5-Lead SOT-353 Pinout (Top View)

### LOGIC SYMBOL



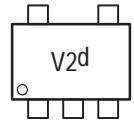
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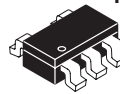
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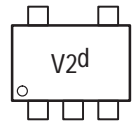
SC-88A / SOT-353/SC-70  
DF SUFFIX  
CASE 419A



Pin 1  
d = Date Code



TSOP-5/SOT-23/SC-59  
DT SUFFIX  
CASE 483A



Pin 1  
d = Date Code

### PIN ASSIGNMENT

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

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## MAXIMUM RATINGS\*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage	$V_{IN}$	-0.5 to +7.0	V
DC Output Voltage $V_{CC} = 0$ High or Low State	$V_{OUT}$	-0.5 to 7.0 -0.5 to $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$I_{OK}$	+20	mA
DC Output Current, per Pin	$I_{OUT}$	+25	mA
DC Supply Current, $V_{CC}$ and GND	$I_{CC}$	+50	mA
Power dissipation in still air, SC-88A †	$P_D$	200	mW
Lead temperature, 1 mm from case for 10 s	$T_L$	260	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — SC-88A Package: -3 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	$V_{CC}$	2.0	5.5	V
DC Input Voltage	$V_{IN}$	0.0	5.5	V
DC Output Voltage	$V_{OUT}$	0.0	$V_{CC}$	V
Operating Temperature Range	$T_A$	-55	+125	°C
Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	$t_r, t_f$	0 0	100 20	ns/V

The  $\theta_{JA}$  of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

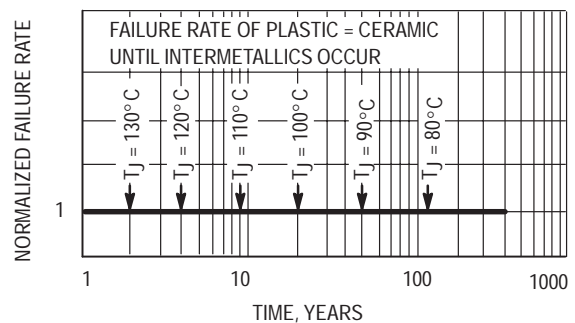


Figure 2. Failure Rate vs. Time Junction Temperature

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			5.5	3.85			3.85		3.85		
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			5.5			1.65		1.65		1.65	
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50μA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
		4.5	4.4	4.5		4.4		4.4		4.4	V
		3.0	2.58			2.48		2.34			
4.5	3.94			3.80		3.66					
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50μA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
		4.5		0.0	0.1		0.1		0.1	V	
		3.0			0.36		0.44		0.52		
4.5			0.36		0.44		0.52				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			2.0		20		40	μA

## AC ELECTRICAL CHARACTERISTICS (C<sub>load</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Y	V <sub>CC</sub> = 3.0 ± 0.3V C <sub>L</sub> = 15 pF		4.1	8.8		10.5		12.5	ns
		C <sub>L</sub> = 50 pF		5.9	12.3		14.0		16.5	
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15 pF		3.5	5.9		7.0		9.0	
		C <sub>L</sub> = 50 pF		4.2	7.9		9.0		11.0	
C <sub>IN</sub>	Maximum Input Capacitance			5.5	10		10		10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V <sub>CC</sub> = 5.0V		pF
		11		

1. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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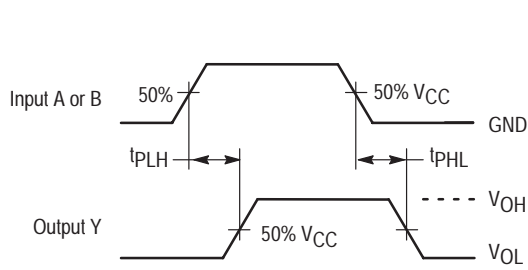
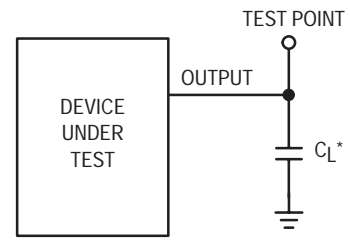


Figure 3. Switching Waveforms



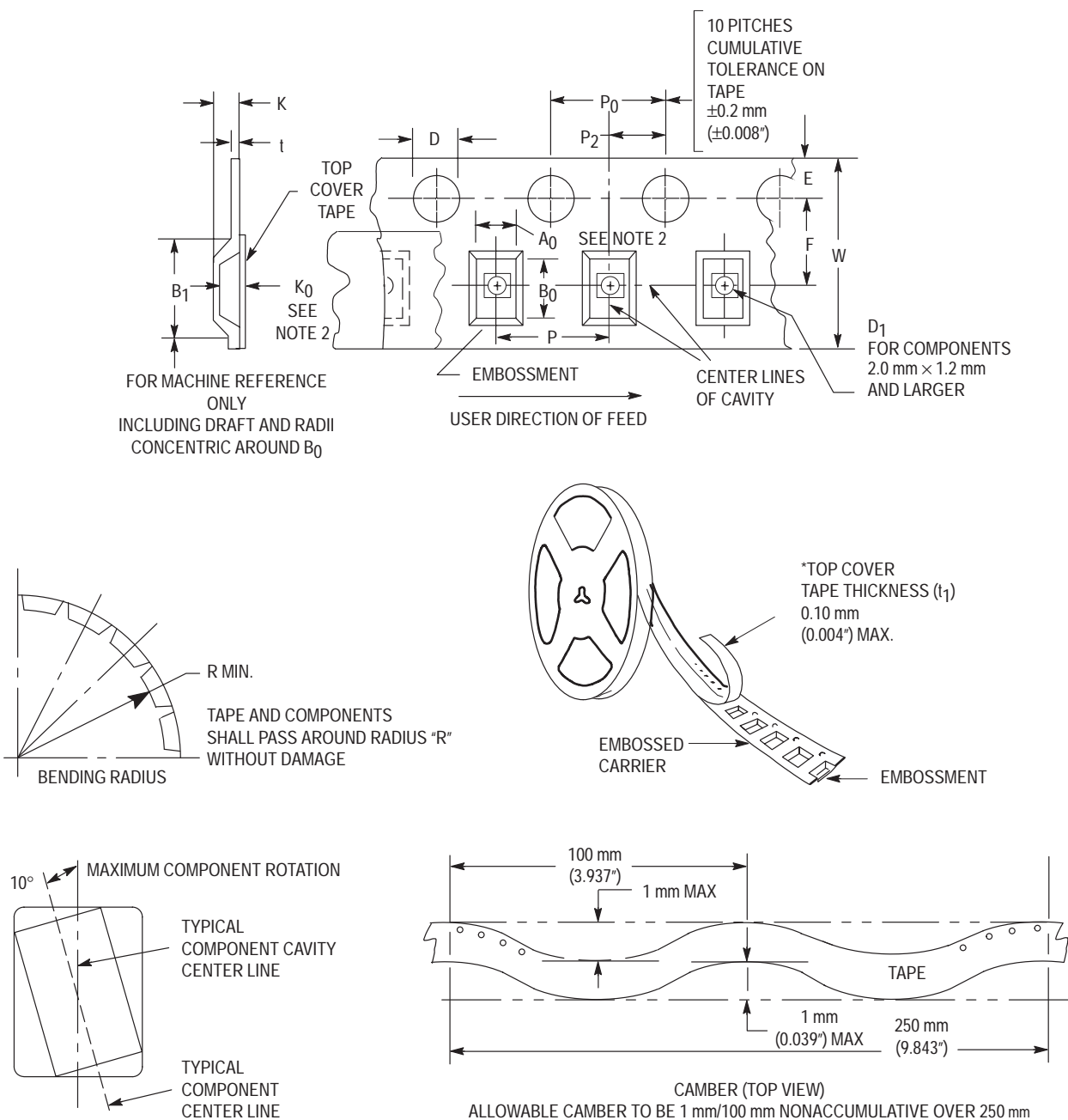
\*Includes all probe and jig capacitance

Figure 4. Test Circuit

## DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G08DFT1	MC	74	VHC1G	08	DF	T1	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1G08DFT2	MC	74	VHC1G	08	DF	T2	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1G08DFR2	MC	74	VHC1G	08	DF	R2	SC-88A / SOT-353 / SC-70	330 mm (13") 10000 Unit
MC74VHC1G08DTT2	MC	74	VHC1G	08	DT	T2	TSOPS / SOT-23 / SC-59	178 mm (7") 3000 Unit
MC74VHC1G08DTR2	MC	74	VHC1G	08	DT	R2	TSOPS / SOT-23 / SC-59	330 mm (13") 10000 Unit

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**Figure 5. Carrier Tape Specifications**

**EMBOSSED CARRIER DIMENSIONS** (See Notes 1 and 2)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/-0.0 mm (0.059 +0.004/-0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/-0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern—English are in parentheses for reference only.
2. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

# MC74VHC1G08

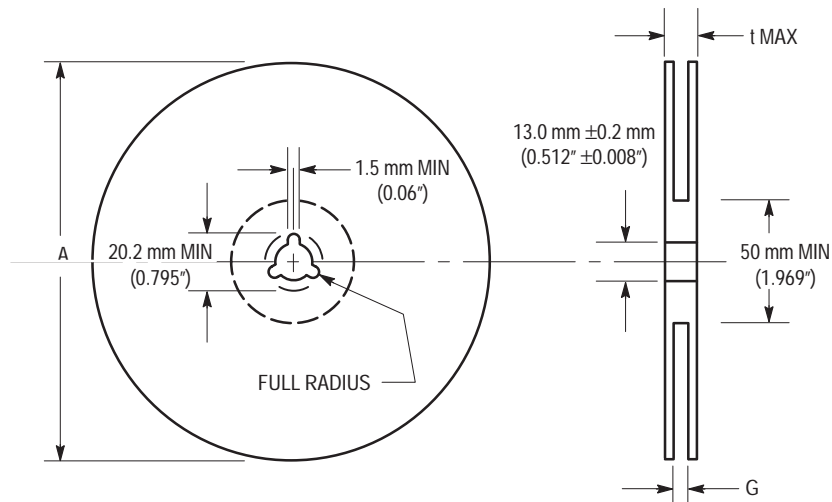


Figure 6. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
8 mm	R2	330 mm (13")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")

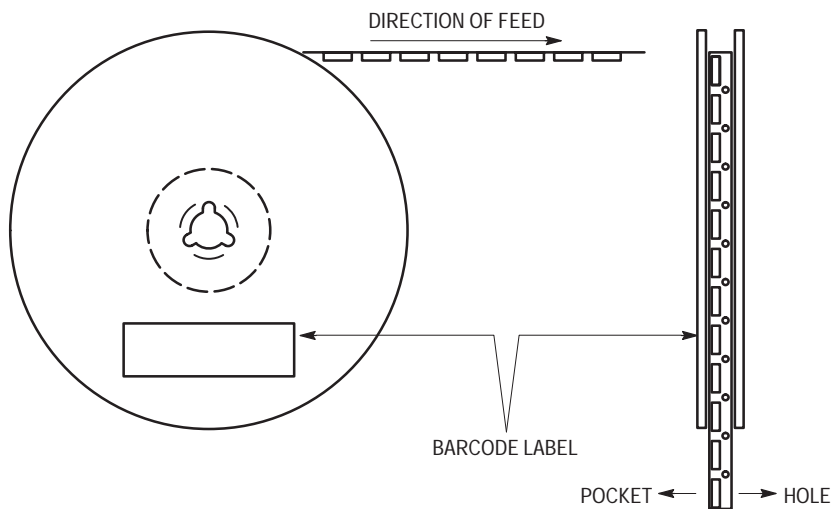
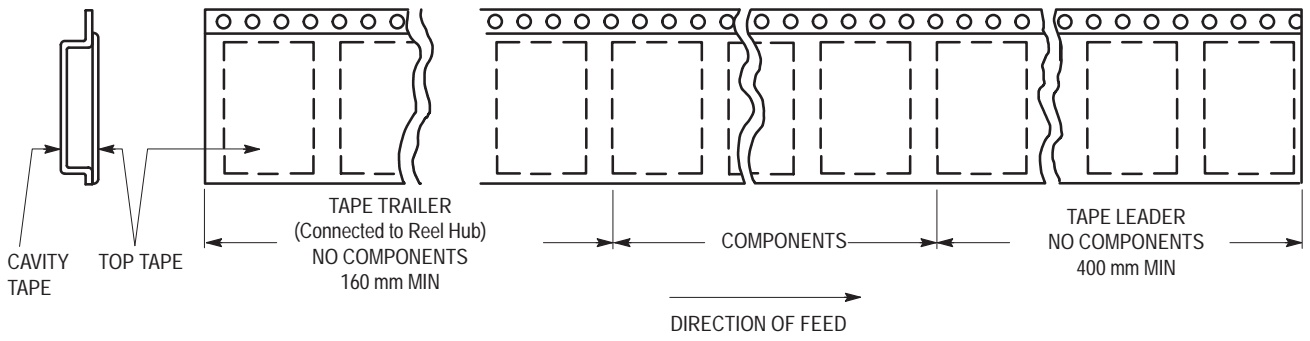
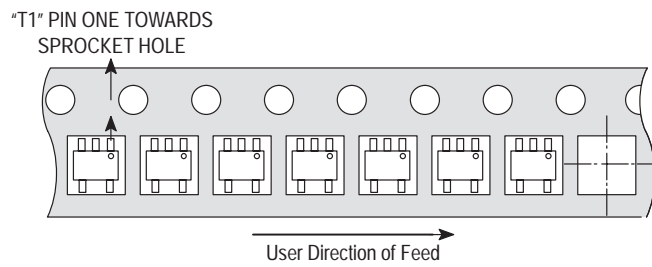


Figure 7. Reel Winding Direction

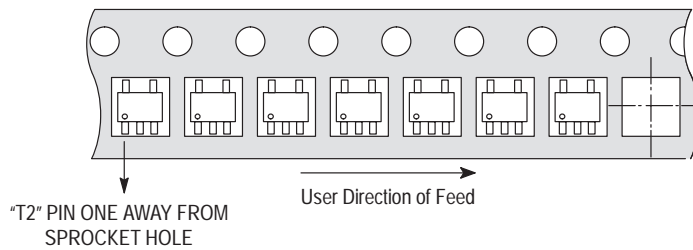
# MC74VHC1G08



**Figure 8. Tape Ends for Finished Goods**



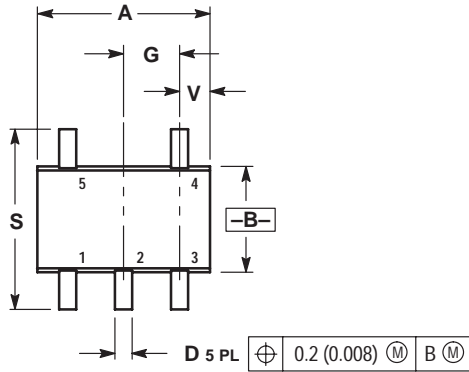
**Figure 9. T1 Reel Configuration**



**Figure 10. T2 Reel Configuration**

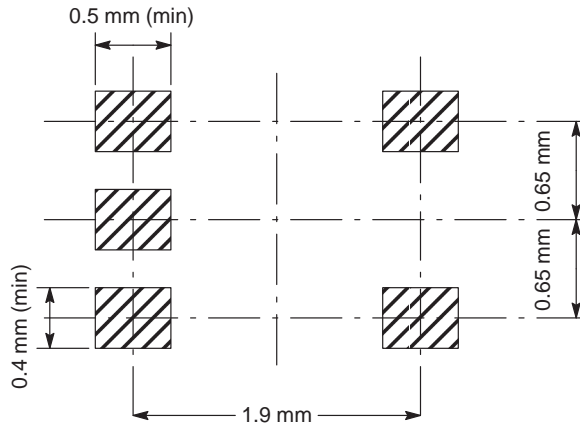
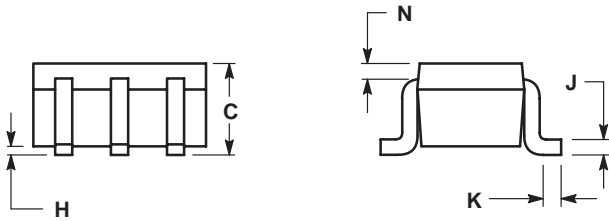
# MC74VHC1G08

SC-88A / SOT-353 / SC-70  
 DF SUFFIX  
 5-LEAD PACKAGE  
 CASE 419A-01  
 ISSUE B



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: MM.

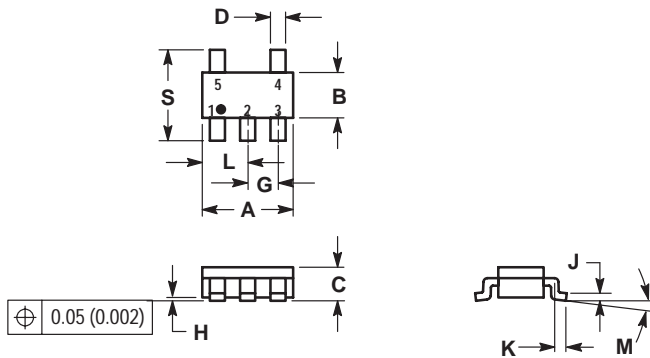
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40





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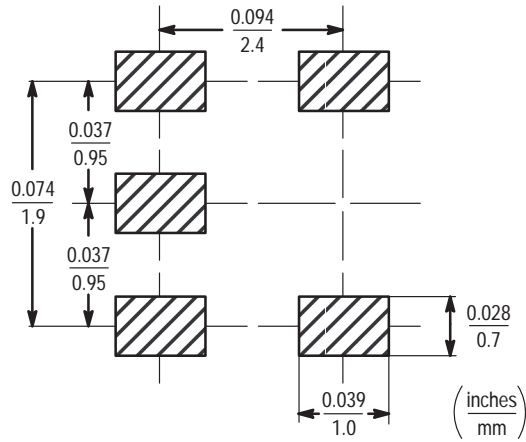
TSOP-5 / SOT-23 / SC-59  
 DT SUFFIX  
 5-LEAD PACKAGE  
 CASE 483-01  
 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181



**Notes**

**Notes**

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