Clock generator with built-in VCO, VCXO

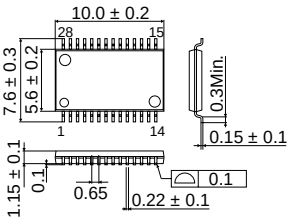
BU3081FV

BU3081FV is a clock generator. It can generate four video / audio clock signals that is used for DVD recorder (Especially for DVD recorder with DV interface of IEEE1394) from one reference frequency. Reference frequency suited for set application can be selected from built-in VCO, VCXO and external input.

●Applications
DVD Recorder

●Features
1) Clock signals are generated by connecting crystal oscillator.
2) SSOP-B28 package
3) 3.3V operating voltage
4) Built-in VCXO (Voltage-Controlled Crystal Oscillator) adjusts clock signal ±110ppm.
5) PLL reference frequency is available from built-in VCO, VCXO and external input.
6) Audio clock can be selected by switches.

●External dimensions (Unit : mm)



SSOP-B28

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Applied voltage	V_{DD}	–0.3	3.3	+7.0	V
Input voltage	V_{IN}	–0.3	–	V_{DD}+0.3	V
Strange temperature range	Tstg	–30	–	+125	°C
Power dissipation	PD	–	–	850	mW

∗ An operation is not guaranteed.
∗ In case it is used at Ta=25°C or more, 8.5mW is reduced at every 1°C.
∗ Radiation resistance design is not used.
∗ Power dissipation measured when BU3081FV is place in the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Analog V_{DD} voltage	AV_{DD},V_{DD}_V	3.15	3.3	3.45	V
Digital V_{DD} voltage	V_{DD}_EX, V_{DD}	3.0	3.3	3.6	V
Input H voltage range	VIH	0.8V_{DD}	–	V_{DD}	V
Input L voltage range	VIL	0.0	–	0.2V_{DD}	V
Operation temperature range	Iopr	–5	25	70	°C
Frequency control voltage	V_C	0.25V_{DD}	0.5V_{DD}	0.75V_{DD}	V
Output maximum load (CLK)	CL_CLK	–	–	15	pF

●Block diagrams

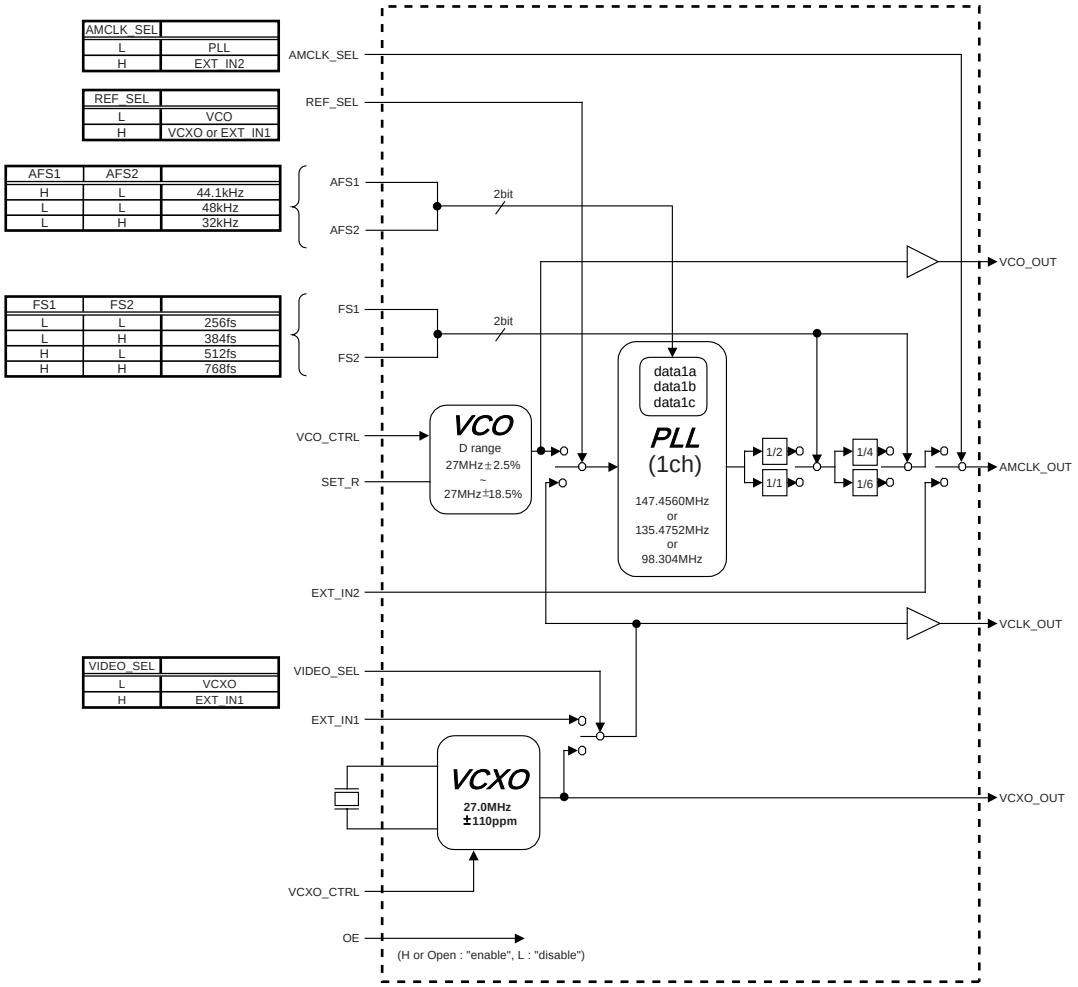


Fig.1

●**Explanation for terminal function**

Pin.No	Pin.name	Function
1	AFS1	Switch of Audio clock output (with pull-down) (∗1)
2	AFS2	Switch of Audio clock output (with pull-down) (∗1)
3	FS1	Switch of Audio clock output (with pull-down) (∗1)
4	FS2	Switch of Audio clock output (with pull-down) (∗1)
5	VCO_CTRL	Input terminal for controlling VCO
6	AV_{DD}	Analog V_{DD}
7	AV_{SS}	Analog GND
8	SET_R	Normally OPEN. Terminal for VCO output adjustment
9	XTAL_IN	Standard crystal input
10	XTAL_OUT	Standard crystal output
11	V_{DD}_V	V_{DD} for VCXO
12	VCXO_CTRL	Input terminal for controlling VCXO
13	VSS_V	GND for VCXO
14	VCXO_OUT	VCXO through output
15	TEST	Input for test mode (with pull-down), normally OPEN (or L)
16	OE	Power-down control (with pull-up), H (Open) : enable, L : disable
17	EXT_IN1	External clock input
18	VSS_EX	GND for external input
19	EXT_IN2	External clock input
20	V_{DD}_EX	V_{DD} for external input
21	VCLK_OUT	Video clock output (∗2)
22	VIDEO_SEL	Switch of video clock (with pull-down) (∗2)
23	AMCLK_OUT	Audio clock output (∗1)
24	V_{SS}	Logic GND for PLL
25	V_{DD}	Logic V_{DD} for PLL
26	REF_SEL	Switch of reference clock (with pull-down) (∗3)
27	AMCLK_SEL	Switch of audio clock (with pull-down) (∗4)
28	VCO_OUT	VCO through output

(∗1) Audio clock output select (AMCLK_SEL=L or OPEN)

AFS1	AFS2	FS1	FS2	AMCLK_OUT[MHz]
L	L	L	L	12.288
L	L	L	H	18.432
L	L	H	L	24.576
L	L	H	H	36.864
L	H	L	L	8.192
L	H	L	H	12.288
L	H	H	L	16.384
L	H	H	H	24.576
H	L	L	L	11.2896
H	L	L	H	16.9344
H	L	H	L	22.5792
H	L	H	H	33.8688

(∗2) Video clock select

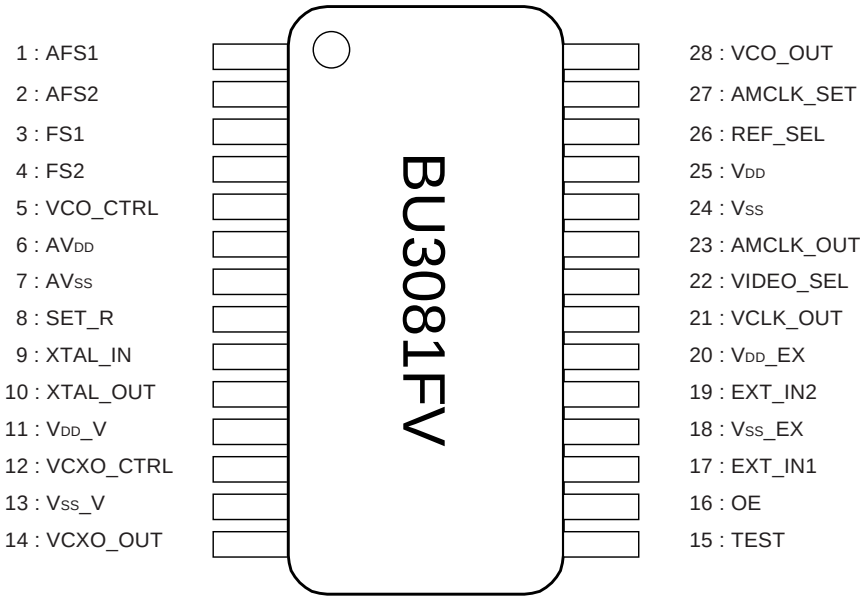
VIDEO_SEL	VCLK_OUT
L	VCXO
H	EXT_IN1

(∗3) Reference clo ck select

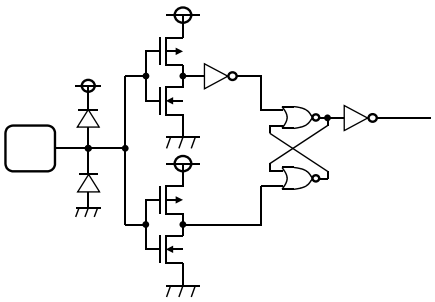
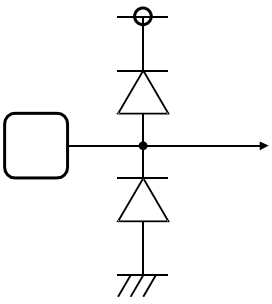
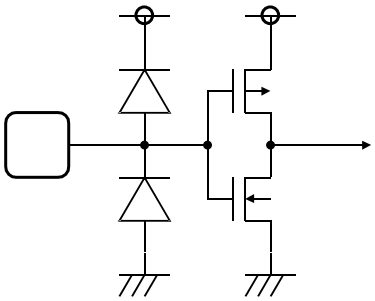
REF_SEL	Reference clock
L	VCO
H	VCXO or EXT_IN1

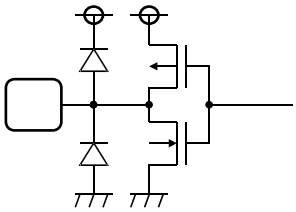
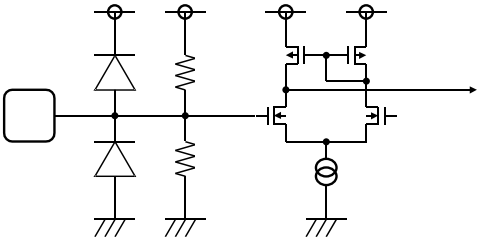
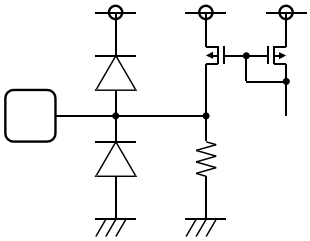
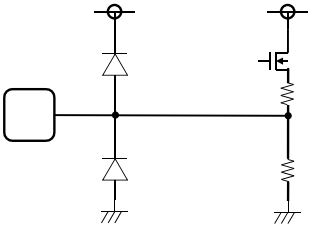
(∗4) Audio clock select

AMCLK_SEL	AMCLK_OUT
L	PLL
H	EXT_IN2



●Input /output equivalent circuit

Pin No.	Equivalent circuit
Input PIN (Schmitt trigger) 1, 2, 3, 4, 15, 22, 26, 27 (with pull-down) 16 (with pull-up)	
Direct input PIN 5, 12	
CMOS input PIN 17, 19	

Output PIN 14, 21, 23, 28	
X'tal input PIN 9	
X'tal output PIN 10	
Input terminal 8	

●**Electrical characteristics** (Unless otherwise noted, V_{CC}=3.3V, Ta=25°C, Crystal frequency=27.0000MHz, No load)

Parameter	Symbol	Rated value			Unit	Condition
		Min.	Typ.	Max.		
Output H voltage	VOH VCLK	2.4	–	–	V	IOH= –4.0mA
Output L voltage	VOL VCLK	–	–	0.4	V	IOL= 4.0mA
Power supply current	IDD	–	50	65	mA	No load
Power supply current2	IDD2	–	50	100	μA	OE=L
CLK	CLK768_44		33.8688		MHz	XTAL_IN∗(3136 / 625) /4
	CLK768_48		36.864			XTAL_IN∗(2048 / 375) /4
	CLK768_32		24.576			XTAL_IN∗(4096 / 1125) /4
	CLK512_44		22.5792			XTAL_IN∗(3136 / 625) /6
	CLK512_48		24.576			XTAL_IN∗(2048 / 375) /6
	CLK512_32		16.384			XTAL_IN∗(4096 / 1125) /6
	CLK384_44		16.9344			XTAL_IN∗(3136 / 625) /8
	CLK384_48		18.432			XTAL_IN∗(2048 / 375) /8
	CLK384_32		12.288			XTAL_IN∗(4096 / 1125) /8
	CLK256_44		11.2896			XTAL_IN∗(3136 / 625) /12
	CLK256_48		12.288			XTAL_IN∗(2048 / 375) /12
	CLK256_32		8.192			XTAL_IN∗(4096 / 1125) /12

Note) When input frequency is 27.0000MHz, output frequency is above rated value. Output frequency is decided by the formula inputted to XTALIN.

●**Deign guaranteed characteristics**

(Unless otherwise noted, V_{CC}=3.3V, Ta=25°C, Crystal frequency=27.0000MHz, No load)

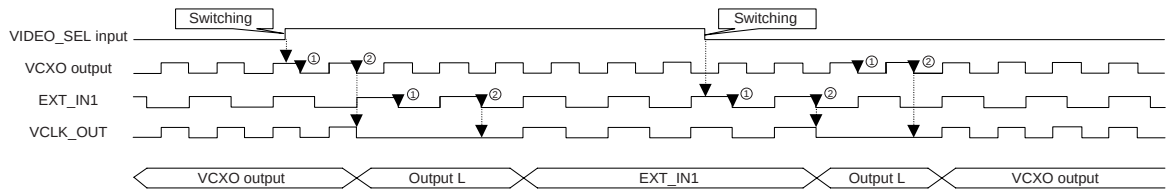
Parameter	Symbol	Rated value			Unit	Condition
		Min.	Typ.	Max.		
Duty	Duty	45	50	55	%	At 1/2 V_{DD} point
Jitter 1σ	JsSD	–	50	–	psec	Jitter 1sigma (∗1)
Jitter p-p	JsABS	–	300	–	psec	MIN-MAX (∗1)
rise time	tr	–	2.5	–	nsec	Time from 0.2V_{DD} to 0.8V_{DD}
fall time	tf	–	2.5	–	nsec	Time from 0.8V_{DD} to 0.2V_{DD}
PLL lock time	Tlock	–	–	1	msec	(∗2)
<VCXO>						
Frequency variable range (MAX)	–	+65	+110	+155	ppm	(VCXO_CTRL=0.75V_{DD})
(MIN)	–	–155	–110	–65	ppm	(VCXO_CTRL=0.25V_{DD})
<VCO>						
Frequency variable range (MAX)	–	27.675	30	32	MHz	(VCO_CTRL=0.75V_{DD})
(MIN)	–	22	24	26.325	MHz	(VCO_CTRL=0.25V_{DD})

Note 2) However, it is just the guarantee of IC and dispersion of X'tal and so on is not taken in consideration.

(∗1) JITTER means center value when using Time Interval Analyzer with 10,000 sampling.

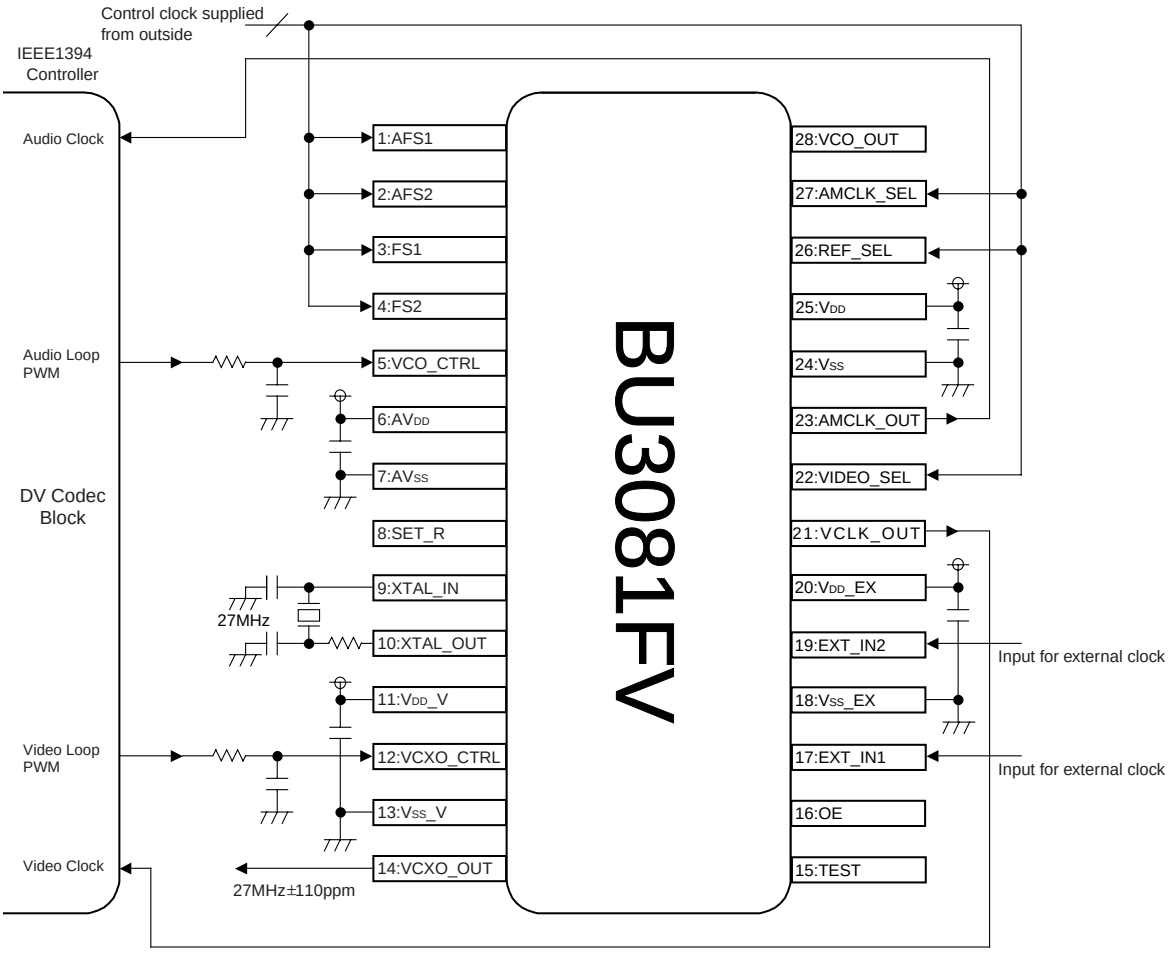
(∗2) Time between voltage supply leads to 3.0V and output clock gets stable.

(Operation of VCLK_OUT at the time of VIDEO_SEL input switching)



After VIDEO_SEL was switched, when VIDEO_SEL is switched again before VCLK_OUT is switched, less than half clock may be output in VCLK_OUT.

●Application circuit



Note 1) When OE is L, Pin14 : VCXO_OUT, Pin21 : VCLK_OUT, Pin23 : AMCLK_OUT, Pin28 : VCO_OUT become L.
Note 2) Pin8 : SET_R is set to OPEN.
Note 3) When Pin17 : EXT_IN1 is not used, set VIDEO_SEL to OPEN or L, and input the output clock of Pin28 : VCO_OUT into Pin17.
Note 4) When a crystal is not connected and VCXO is not used, set VIDEO_SEL to H and input the same external clock into Pin9 : XTAL_IN as Pin17 : EXT_IN1. Set VCXO_CTRL to L, and set VCXO_OUT and XTAL_OUT to OPEN.
Note 5) When neither VCXO nor Pin17 : EXT_IN1 is not used, set EXT_IN1, VCXO_CTRL to L, set VIDEO_SET to OPEN or L, and set VCXO_OUT, VCLK_OUT, XTAL_IN, and XTAL_OUT to OPEN.
Note 6) When Pin5 : VCO_CTRL is not used, set it to L.
Note 7) When Pin28 : VCO_OUT or Pin23 : AMCLK_OUT is not used, set them to OPEN.
Note 8) When Pin19 : EXT_IN2 is not used, set it to L.
Note 9) Pin15 : TEST is set to OPEN (or L).
Note10) The VCXO operation is checked by using the crystal (specification No. EXS00A-00460) made by NDK (Nihon Dempa Kogyo Co., LTD). Condition : normal temperature, applied voltage 3.3V
Finally, the crystal needs to be tuned to each set for adjustment f=27MHz at the time of VCXO_CTRL=1.65V and cancel of temperature characteristic. Please ask a crystal maker.
Note11) BU3081 is basically placed on the board.
Decoupling capacitance (0.1µF) need to be placed between Pin6 (AV_{DD}) and Pin7 (AV_{SS}), Pin11 (V_{DD}_V) and Pin13 (V_{SS}_V), Pin20 (V_{DD}_EX) and Pin18 (V_{SS}_EX), Pin25 (V_{DD}) and Pin24 (V_{SS}).
To obtain accurate frequency, capacitance (pF) need to be placed between Pin9 and Pin13, Pin10 and Pin13
Tantalum capacitance (10~100pF), ferrite beads may need to be placed to prevent power supply drop in certain boards case. To reduce high frequency noise, selected bypass capacitors(≤1Ω at problem high frequency) may be used for power pin as close to BU3081FV as possible.
Note12) ROHM assumes no responsibility for connection of application circuit and use of external components and component's constant described herein, conveys no license under any patent or other right, and makes no representation that the circuit are free from patent infringement.

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