



# W24M257A

## 32K × 8 HIGH SPEED CMOS STATIC RAM

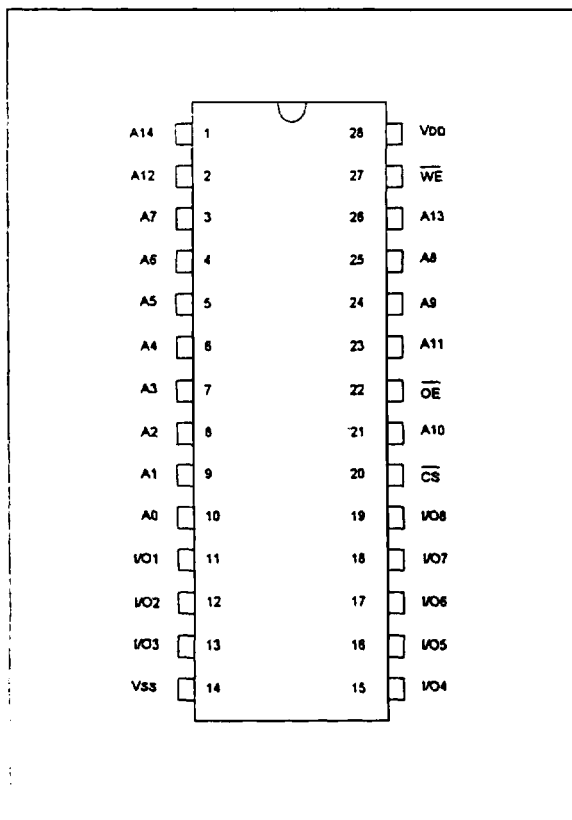
### GENERAL DESCRIPTION

The W24M257A is a high speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

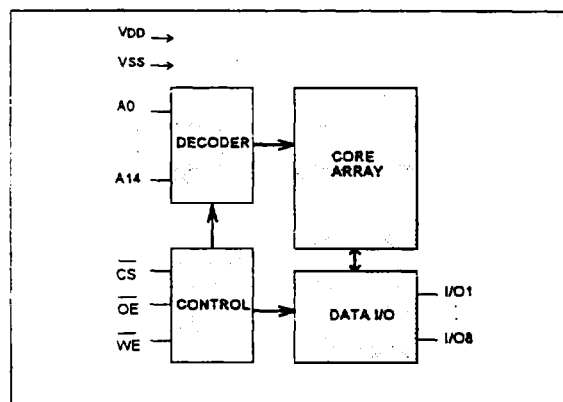
### FEATURES

- High speed access time: 12/15/20 nS (max.)
- Low power consumption:
  - Active: 400 mW (typ.)
- Single +5 V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Output level: 3.3 V
- Available packages: 28-pin 300 mil SOJ and skinny DIP

### PIN CONFIGURATION



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground



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## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to +7.0	V
Input/Output to Vss Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

## OPERATING CHARACTERISTICS

(VDD = 5 V  $\pm$  5%, Vss = 0 V, Ta = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	VIL	-	-0.5	-	+0.8	V
Input High Voltage	VIH	-	+2.2	-	VDD +0.5	V
Input Leakage Current	II	VIN = Vss to VDD	-10	-	+10	$\mu$ A
Output Leakage Current	ILO	VIO = Vss to VDD, $\overline{CS}$ = VIH or $\overline{OE}$ = VIH or $\overline{WE}$ = VIL	-10	-	+10	$\mu$ A
Output Low Voltage	VOL	IOL = +8 mA	-	-	0.4	V
Output High Voltage	VOH	IOH = -4 mA	2.4	-	3.4	V
Operating Power	IDD	$\overline{CS}$ = VIL, I/O = 0 mA	12	-	-	mA
Supply Current		Cycle = MIN, Duty = 100%	15	-	-	mA
			20	-	-	mA
Standby Power	ISB	$\overline{CS}$ = VIH, Cycle = MIN Duty = 100%	-	-	30	mA
Supply Current	ISB1	$\overline{CS}$ $\geq$ VDD -0.2 V	-	-	10	mA

Note: Typical characteristics are at VDD = 5 V, Ta = 25° C.



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## CAPACITANCE

(V<sub>DD</sub> = 5 V, T<sub>a</sub> = 25° C, f = 1 MHz)

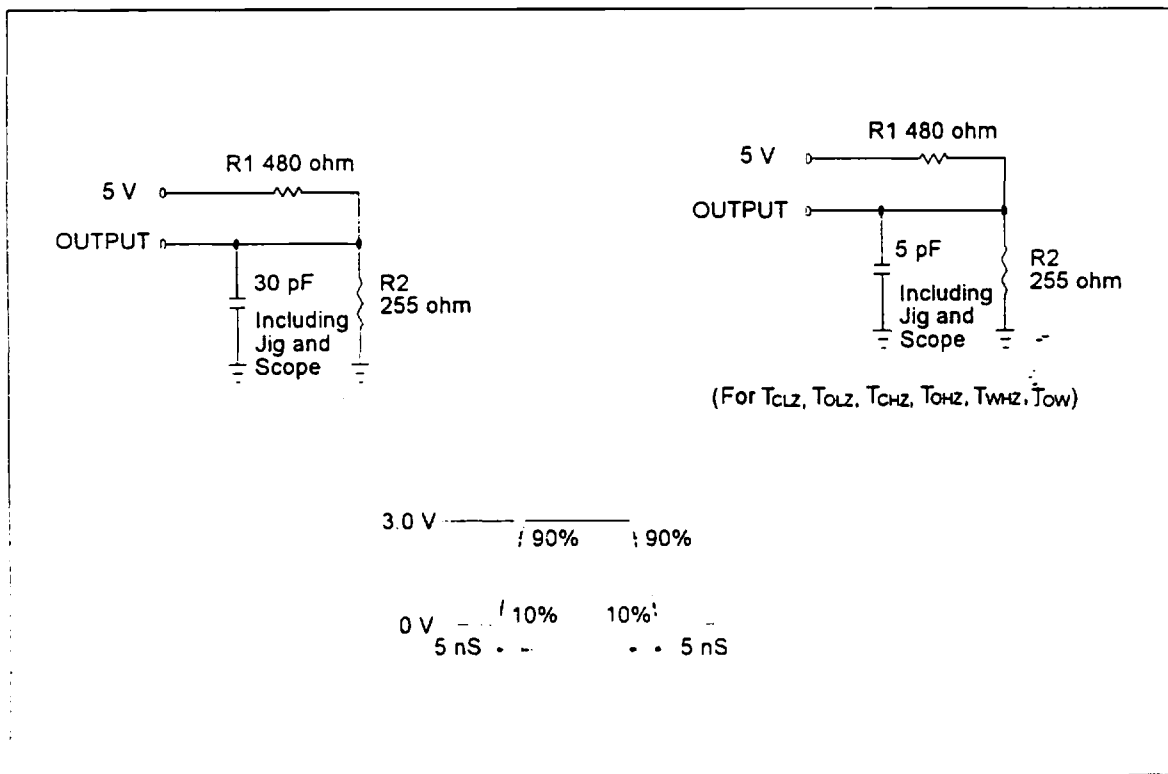
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0 V	10	pF

Note: These parameters are sampled but not 100% tested.

## AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0 V to 3 V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5 V
Output Load	C <sub>L</sub> = 30 pF, I <sub>OH</sub> /I <sub>OL</sub> = -4 mA/8 mA

## AC TEST LOADS AND WAVEFORM





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## AC CHARACTERISTICS

(V<sub>DD</sub>= 5 V ± 5%, V<sub>SS</sub>= 0 V, T<sub>a</sub>= 0 to 70° C)

### (1) Read Cycle

PARAMETER	SYM.	W24M257A-12		W24M257A-15		W24M257A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	12	-	15	-	20	-	nS
Address Access Time	TAA	-	12	-	15	-	20	nS
Chip Select Access Time	TACS	-	12	-	15	-	20	nS
Output Enable to Output Valid	TAOE	-	6	-	7	-	10	nS
Chip Selection to Output in Low Z	TCLZ*	3	-	3	-	3	-	nS
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	0	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	6	-	7	-	10	nS
Output Disable to Output in High Z	TOHZ*	-	6	-	7	-	10	nS
Output Hold from Address Change	TOH	3	-	3	-	3	-	nS

\*These parameters are sampled but not 100% tested

### (2) Write Cycle

PARAMETER		SYM.	W24M257A-12		W24M257A-15		W24M257A-20		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	12	-	15	-	20	-	nS
Chip Selection to End of Write		TCW	10	-	13	-	17	-	nS
Address Valid to End of Write		TAW	10	-	13	-	17	-	nS
Address Setup Time		TAS	0	-	0	-	0	-	
Write Pulse Width		TWP	10	-	10	-	12	-	nS
Write Recovery Time	$\overline{\text{CS}}, \overline{\text{WE}}$	TWR	0	-	0	-	0	-	nS
Data Valid to End of Write		TDW	7	-	9	-	10	-	nS
Data Hold from End of Write		TDH	0	-	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	7	-	8	-	10	nS
Output Disable to Output in High Z		TOHZ*	-	7	-	8	-	10	nS
Output Active from End of Write		TOW	0	-	0	-	0	-	nS

\*These parameters are sampled but not 100% tested

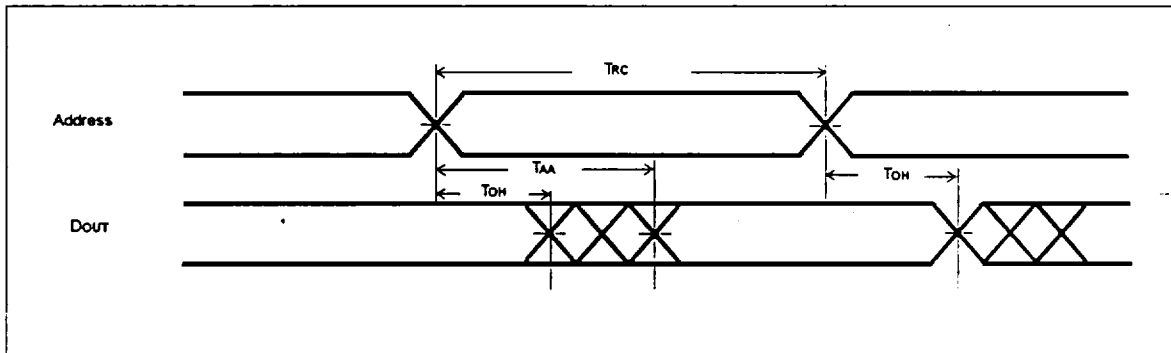


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## TIMING WAVEFORMS

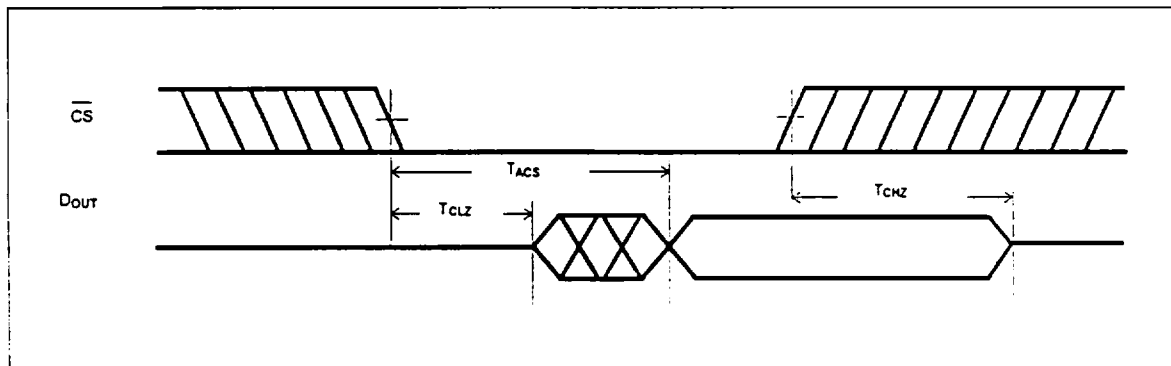
### Read Cycle 1

(Address Controlled)



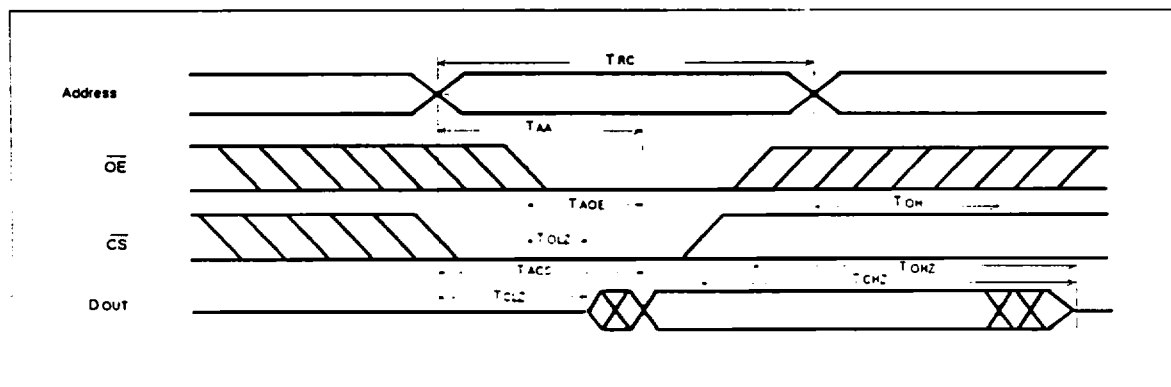
### Read Cycle 2

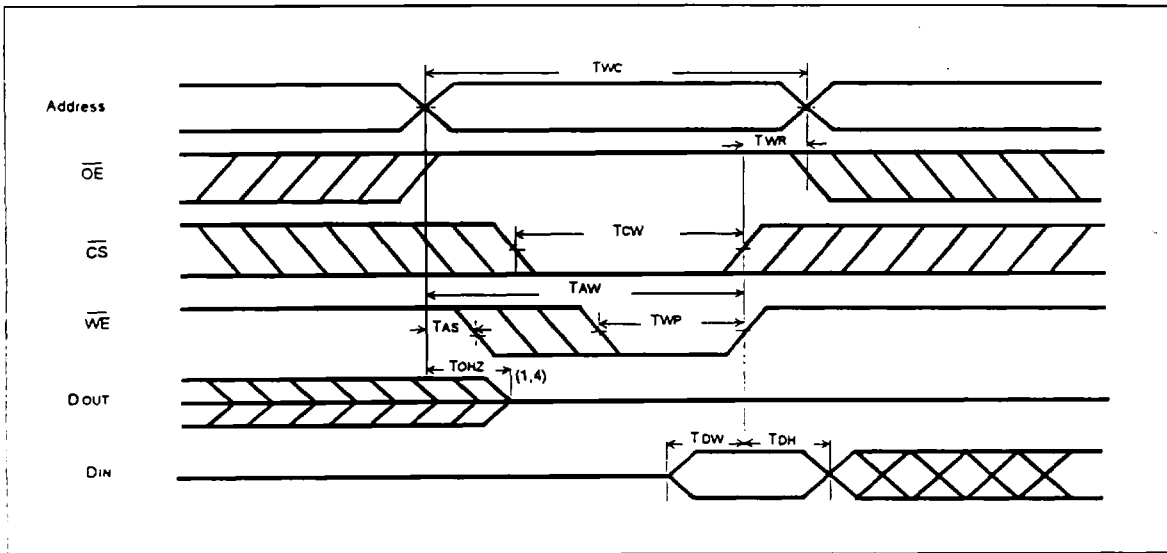
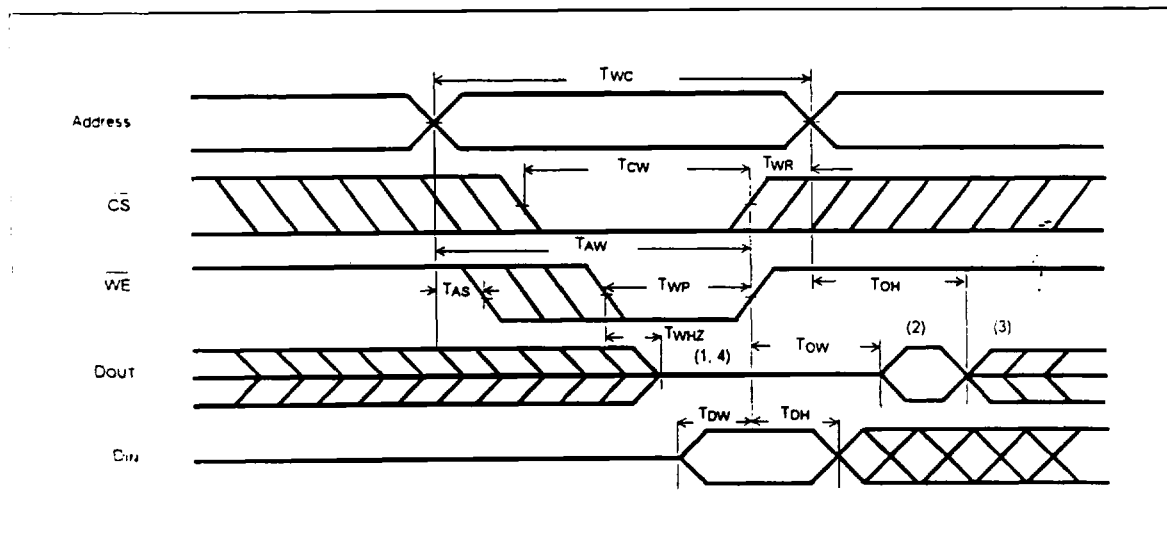
(Chip Select Controlled)



### Read Cycle 3

(Output Enable Controlled)



**Write Cycle 1**
**( $\overline{OE}$  Clock)**

**Write Cycle 2**
**( $\overline{OE}$  = VIL Fixed)**

**Notes**

- 1 During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
- 2 The data output from DOUT are the same as the data written to DIN during the write cycle.
- 3 DOUT provides the read data for the next address.
- 4 Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.



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### ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24M257AK-12	12	180	10	300mil Skinny
W24M257AK-15	15	180	10	300mil Skinny
W24M257AK-20	20	150	10	300mil Skinny
W24M257AJ-12	12	180	10	300mil SOJ
W24M257AJ-15	15	180	10	300mil SOJ
W24M257AJ-20	20	150	10	300mil SOJ

Notes:

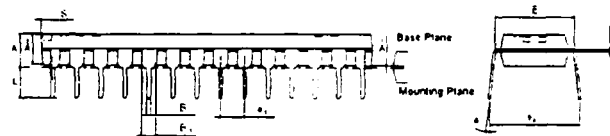
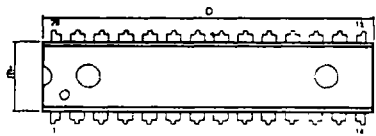
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.



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## PACKAGE DIMENSIONS

### 28-Lead P-DIP Skinny

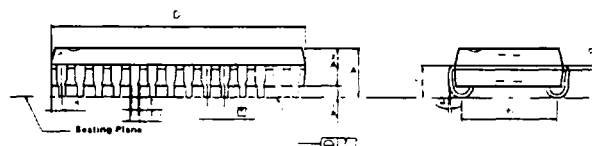
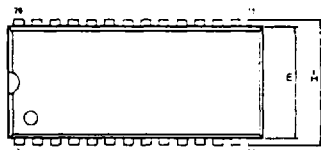


Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.172	—	—	4.45
A <sub>1</sub>	0.010	—	—	0.25	—	—
A <sub>2</sub>	0.125	0.130	0.135	3.18	3.30	3.43
B	0.018	0.018	0.222	0.45	0.45	5.65
B <sub>1</sub>	0.004	0.000	0.254	0.10	0.00	6.41
C	0.008	0.010	0.018	0.20	0.25	0.45
D	—	1.300	1.450	—	33.00	36.80
E	0.300	0.310	0.320	7.62	7.87	8.13
E <sub>1</sub>	0.293	0.298	0.303	7.44	7.57	7.69
e <sub>1</sub>	0.008	0.100	0.110	0.20	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
s	0	—	0.10	0	—	2.54
θ <sub>A</sub>	0.330	0.380	0.470	8.38	9.65	11.93
S	—	—	0.020	—	—	0.51

#### Notes:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E<sub>1</sub> does not include interlead flash.
3. Dimension D & E<sub>1</sub> include mold mismatch and are determined at the mold parting line.
4. Dimension B<sub>1</sub> does not include dambar protrusion/intrusion.
5. Controlling dimension: inches.
6. General appearance spec. should be based on final visual inspection spec.

### 28-Lead Small Outline J Band



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.140	—	—	3.55
A <sub>1</sub>	0.027	—	—	0.69	—	—
A <sub>2</sub>	0.095	0.100	0.105	2.41	2.54	2.67
b <sub>1</sub>	0.024	0.028	0.032	0.61	0.71	0.81
b	0.018	0.018	0.022	0.45	0.45	0.56
C	0.008	0.010	0.014	0.20	0.25	0.35
D	—	0.710	0.750	—	18.03	19.05
E	0.225	0.300	0.325	5.71	7.62	8.28
H	0.044	0.050	0.055	1.12	1.27	1.42
θ <sub>A</sub>	0.245	0.255	0.265	6.22	6.47	6.73
H <sub>2</sub>	0.027	0.037	0.047	0.69	0.94	1.20
L	0.073	0.087	0.097	1.85	2.21	2.46
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
0	0°	—	10°	0°	—	10°

#### Notes:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: inches.
5. General appearance spec. should be based on final visual inspection spec.





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