

**PRELIMINARY**

Note: This is not a final specification.  
Some parameter limits are subject to change.

# MITSUBISHI LSI's M5M4V18167CTP-5,-6,-7, -5S,-6S,-7S

**PIPELINE BURST MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

## DESCRIPTION

The M5M4V18167CTP is pipeline burst dynamic RAM organized 1048574-words by 16-bits. This is fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

## FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18167CTP-5,-5S	50	10	25	10	90	540
M5M4V18167CTP-6,-6S	60	11.6	30	12	110	450
M5M4V18167CTP-7,-7S	70	15	35	15	130	390

- Standard 50 pin TSOP
- Single 3.3V +0.3V, -0.15V supply (3.15V~3.6V)
- Low stand-by power dissipation  
1.8mW (Max) .....CMOS input level
- Low operating power dissipation  
M5M4V18167CTP- 5,-5S .....650.0mW (Max)  
M5M4V18167CTP- 6,-6S .....540.0mW (Max)  
M5M4V18167CTP- 7,-7S .....470.0mW (Max)
- Pipeline Burst mode , RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance  
All inputs, output LVTTTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A0~A9)
  - ∴ Applicable to self refresh version (M5M4V18167CTP-5S,-6S,-7S: option) only

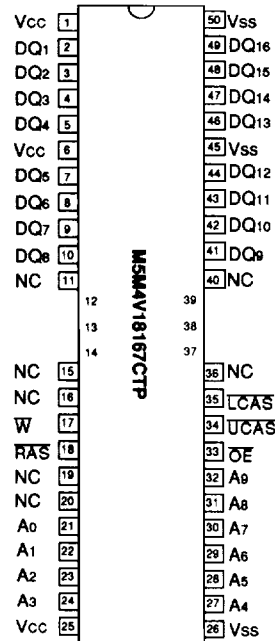
## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

## PIN DESCRIPTION

Pin name	Function
A0~A9	Address inputs
DQ1~DQ16	Data inputs / outputs
RAS	Row address strobe input
UCAS	Upper byte control column address strobe input
LCAS	Lower byte control column address strobe input
W	Write control input
OE	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

## PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC:NO CONNECTION

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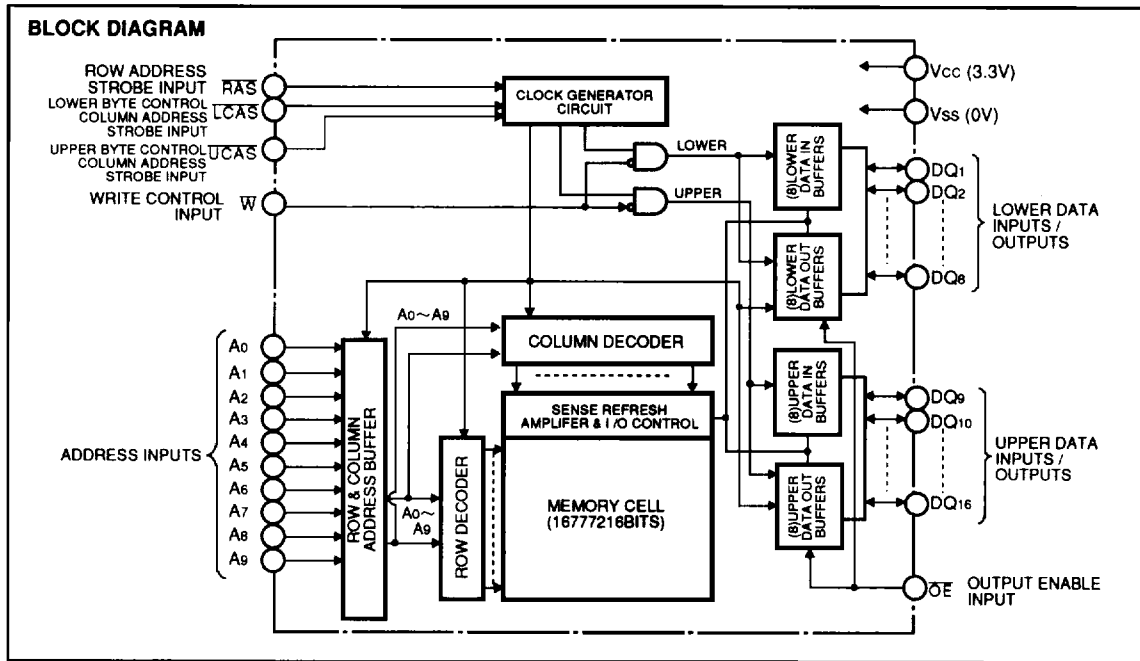
FUNCTION

The M5M4V18167CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., pipeline burst mode, RAS only refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	RAS	LCAS	UCAS	W	OE	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
RAS-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
CAS before RAS refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

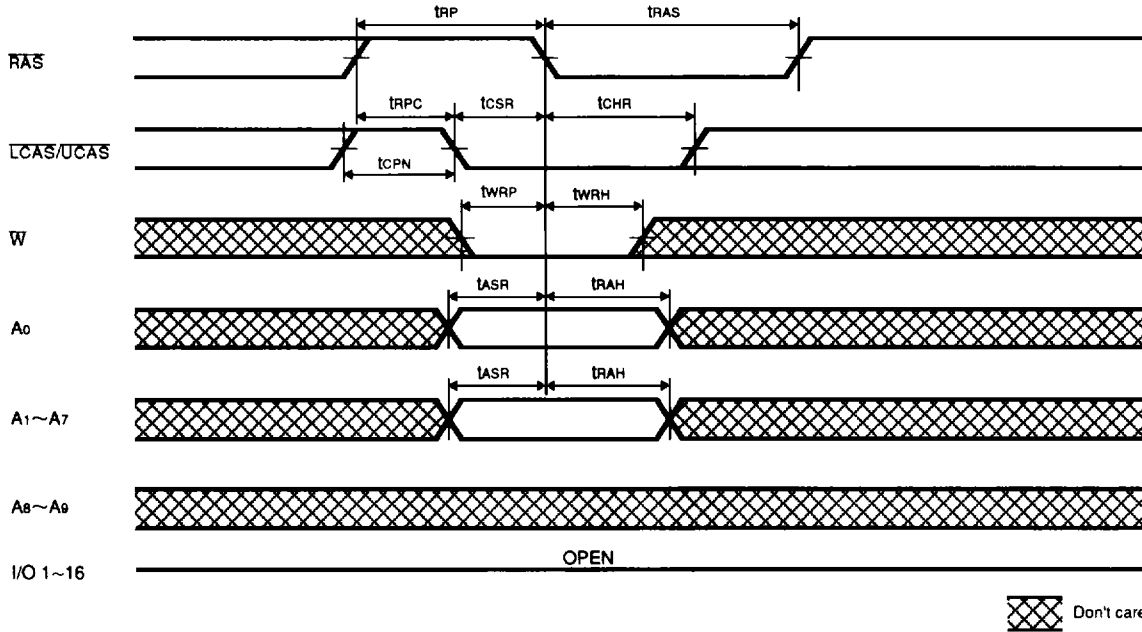


PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Burst Address Sequence Table

	INTERLEAVE				LINEAR			
	1st	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01	X..X10
2nd	X..X01	X..X00	X..X11	X..X10	X..X01	X..X10	X..X11	X..X00
3rd	X..X10	X..X11	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01
4th	X..X11	X..X10	X..X01	X..X00	X..X11	X..X00	X..X01	X..X10

Burst Address Sequence Set Cycle



Note 1: Address Table for Burst address sequence setting cycle.

	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Linear	X	X	L	L	H	L	L	L	L	L
Interleave	X	X	L	L	H	L	L	L	L	H

- 2: The burst sequence will remain set until the device power is interrupted or another Burst address sequence setting cycle.
- 3: A RAS only or CBR refresh cycle must follow the Burst address setting cycle to exit the programming mode.

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**PIPELINE BURST MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~4.6	V
Vi	Input voltage		-0.5~4.6	V
Vo	Output voltage		-0.5~4.6	V
Io	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

**RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 4)**

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.15	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
Vih	High-level input voltage, all inputs	2.0		Vcc+0.3	V
Vil	Low-level input voltage, all inputs	-0.3		0.8	V

Note 4: All voltage values are with respect to Vss.

**ELECTRICAL CHARACTERISTICS (Ta=0~70 °C, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted) (Note 5)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Voh	High-level output voltage	I <sub>OH</sub> =-2.0mA	2.4		Vcc	V
Vol	Low-level output voltage	I <sub>OL</sub> =2.0mA	0		0.4	V
Ioz	Off-state output current	Q floating 0V ≤ V <sub>out</sub> ≤ 3.3V	-10		10	μA
Ii	Input current	0V ≤ V <sub>IN</sub> ≤ 3.6V, Other inputs pins=0V	-10		10	μA
Icc1 (AV)	Average supply current from Vcc, operating (Note 6,7,8)	M5M4V18167C-5,-5S	RAS, CAS cycling trc=twc=min. output open		180	mA
		M5M4V18167C-6,-6S			150	
		M5M4V18167C-7,-7S			130	
Icc2	Supply current from Vcc, stand-by (Note 8)	RAS = CAS = V <sub>ih</sub> , output open			2	mA
		RAS = CAS ≥ Vcc - 0.2 V			0.5	
Icc2*	Supply current from Vcc, stand-by (Note 9)	RAS = CAS ≥ Vcc - 0.2 V			150	μA
Icc3 (AV)	Average supply current from Vcc, refreshing (Note 6,8)	M5M4V18167C-5,-5S	RAS cycling, CAS = V <sub>ih</sub> trc=min. output open		180	mA
		M5M4V18167C-6,-6S			150	
		M5M4V18167C-7,-7S			130	
Icc4(AV)	Average supply current from Vcc Pipeline-Burst-Mode (Note 6,7)	M5M4V18167C-5,-5S	RAS = V <sub>il</sub> , CAS cycling trc=min. output open		150	mA
		M5M4V18167C-6,-6S			140	
		M5M4V18167C-7,-7S			120	
Icc4(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 6)	M5M4V18167C-5,-5S	CAS before RAS refresh cycling trc=min. output open		180	mA
		M5M4V18167C-6,-6S			150	
		M5M4V18167C-7,-7S			130	
Icc4(AV) *	Average supply current from Vcc Extended-Refresh-Mode (Note 9)	RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling (W, OE, A0~A9 ≤ 0.2V or ≥ Vcc - 0.2V) DQ=open, tRC=125 μs, tRAS=tRAS min. ~1 μs			300	μA
Icc4(AV) *	Average supply current from Vcc Self-Refresh-Mode (Note 9)	RAS = CAS ≤ 0.2V, output open			200	μA

Note 5: Current flowing into an IC is positive, out is negative.

6: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

7: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

8: Column Address can be changed once or less while RAS = V<sub>il</sub> and CAS/OCAS = V<sub>ih</sub>.

9: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 16.4 ms) of RAS inactivity before proper device operation is achieved.

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**CAPACITANCE** (Ta=0~70 °C, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI(A)	Input capacitance, address inputs	Vi=Vss f=1MHZ Vi=25mVrms			5	pF
CI(OE)	Input capacitance, OE Input				7	pF
CI(W)	Input capacitance, write control input				7	pF
CI(RAS)	Input capacitance, RAS input				7	pF
CI(CAS)	Input capacitance, CAS input				7	pF
CI/O	Input/Output capacitance, data ports				7	pF

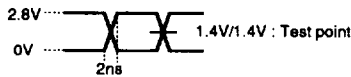
**SWITCHING CHARACTERISTICS** (Ta=0~70°C, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted, see notes 10,11)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 12)		10		11.6		15	ns
tRAC	Access time from RAS (Note 13)		50		60		70	ns
tAA	Column address access time (Note 14)		25		30		35	ns
tCPA	Access time from CAS precharge (Note 15)		30		35		40	ns
tOEA	Access time from OE		10		12		15	ns
tDOH	Data hold time from CAS Low	3		3		3		ns
tOLZ	Output low impedance time from OE low	3		3		3		ns
tCLZ	Output low impedance time from CAS low	3		3		3		ns
tOEZ	Output disable time after OE high (Note 16)	4	10	4	10	4	15	ns
tWEZ	Output disable time after WE low (Note 16)	4	10	4	10	4	15	ns
tOFF	Output disable time after CAS high (Note 16,17)	4	10	4	10	4	15	ns
tREZ	Output disable time after RAS high (Note 16,17)	4	10	4	10	4	15	ns

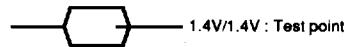
Note 10: AC Measurements  $t_T=2ns$ .

11: AC Characteristics test condition

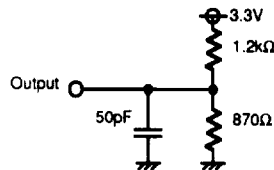
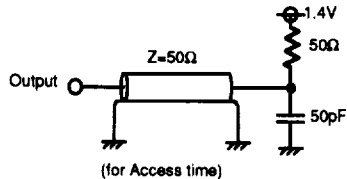
(1) Input timing Specification



(2) Output timing Specification



(3) Output Load



Note 12: Assumes that  $t_{RCD} \geq t_{RCD(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$  and  $t_{CP} \geq t_{CP(max)}$ .

13: Assumes that  $t_{RCD} \leq t_{RCD(max)}$  and  $t_{RAD} \leq t_{RAD(max)}$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by amount that  $t_{RCD}$  exceeds the value shown.

14: Assumes that  $t_{RAD} \geq t_{RAD(max)}$  and  $t_{ASC} \leq t_{ASC(max)}$ .

15: Assumes that  $t_{CP} \leq t_{CP(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$ .

16:  $t_{OEZ(max)}$ ,  $t_{WEZ(max)}$ ,  $t_{OFF(max)}$  and  $t_{REZ(max)}$  defines the time at which the output achieves the high impedance state ( $I_{OUT} \leq |\pm 10 \mu A|$ ) and is not reference to  $V_{OH(min)}$  or  $V_{OL(max)}$ .

17: Output is disabled after both RAS and CAS go to high.

PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

**TIMING REQUIREMENTS (for Read, Write, and Refresh Cycles)**

(Ta=0~70°C, Vcc = 3.15V~3.6V, Vss=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note18)	18	25	20	31.8	20	40	ns
tCRP	Delay time, CAS high to RAS low	10		10		10		ns
tRPC	Delay time, RAS high to CAS low	5		5		5		ns
tCPN	CAS high pulse width	10		10		10		ns
tRAD	Column address delay time from RAS low (Note19)	15	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	1.5		1.5		1.5		ns
tASC	Column address setup time before CAS low (Note20)	1.5		1.5		1.5		ns
tRAH	Row address hold time after RAS low	8.5		8.5		8.5		ns
tCAH	Column address hold time after CAS low	8.5		8.5		8.5		ns
tdZC	Delay time, data to CAS low (Note21)	0		0		0		ns
tdZO	Delay time, data to OE low (Note21)	0		0		0		ns
tRDD	Delay time, RAS high to data (Note22)	13		15		20		ns
tCDD	Delay time, CAS high to data (Note22)	13		15		20		ns
tODD	Delay time, OE high to data (Note22)	13		15		20		ns
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	5	10000	5	10000	5	10000	ns
tRCS	Read Setup time before CAS low	3		3		3		ns
tRCH	Read hold time after CAS high (Note 23)	5		5		5		ns
tRRH	Read hold time after RAS high (Note 23)	10		10		10		ns
tORH	RAS hold time after OE low	13		15		20		ns
tOCH	CAS hold time after OE low	13		15		20		ns
twCS	Write setup time before CAS low	3		3		3		ns
twCH	Write hold time after CAS low	5		5		5		ns
twEP	Write pulse width	7		7		7		ns
tCRW	CAS Low to RAS High (Required only for Write Cycle)	15		15		15		ns
tDS	Data setup time before CAS low or W low	3		3		3		ns
tDH	Data hold time after CAS low or W low	5		5		5		ns
tT	Transition time	1.5	50	1.5	50	1.5	50	ns
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tREF*	Refresh cycle time		128		128		128	ms

Note 18: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

19: tRAD(max) is specified as a reference point only. If tRAD  $\geq$  tRAD(max) and tASC  $\leq$  tASC(max), access time is controlled exclusively by tAA.

20: tASC(max) is specified as a reference point only. If tRCD  $\geq$  tRCD(max) and tASC  $\geq$  tASC(max), access time is controlled exclusively by tCAC.

21: Either tdZC or tdZO must be satisfied.

22: Either tRDD or tCDD or tODD must be satisfied.

23: Either tRCH or tRRH must be satisfied for a read cycle.

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**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Pipeline Burst Mode Cycle (Read,Read terminated Read,Write,Write terminated Write,Read-Write,Write-Read) (Note 24)**

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Pipeline Burst EDO Cycle	15		16.6		20		ns
tDOH	Output hold time from $\overline{\text{CAS}}$ low	3		3		3		ns
tRAS	$\overline{\text{RAS}}$ low pulse width for read write cycle (Note25)	50	125000	60	125000	70	125000	ns
tCP	$\overline{\text{CAS}}$ high pulse width (Note26)	5		5		5		ns
tCHOL	Hold time to maintain the data Hi -Z until $\overline{\text{CAS}}$ access	7		7		7		ns
tOEP	$\overline{\text{OE}}$ Pulse Width	7		7		7		ns
tWEP	$\overline{\text{WE}}$ Pulse Width	7		7		7		ns
tWET	$\overline{\text{WE}}$ Pulse Width (for Write comand termination)	7		7		7		ns
twLC	$\overline{\text{W}}$ Lock out from $\overline{\text{CAS}}$ High	3		3		3		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

25: tRAS(min) is specified as two cycles of  $\overline{\text{CAS}}$  input are performed.

26: tCP(max) is specified as a reference point only.

**$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh, and WCBR Cycle (Note 27)**

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{\text{CAS}}$ setup time before $\overline{\text{RAS}}$ low	10		10		10		ns
tCHR	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	15		15		15		ns
tWRP	$\overline{\text{WE}}$ setup time before $\overline{\text{RAS}}$ low	10		10		10		ns
tWRH	$\overline{\text{WE}}$ hold time after $\overline{\text{RAS}}$ low	10		10		10		ns

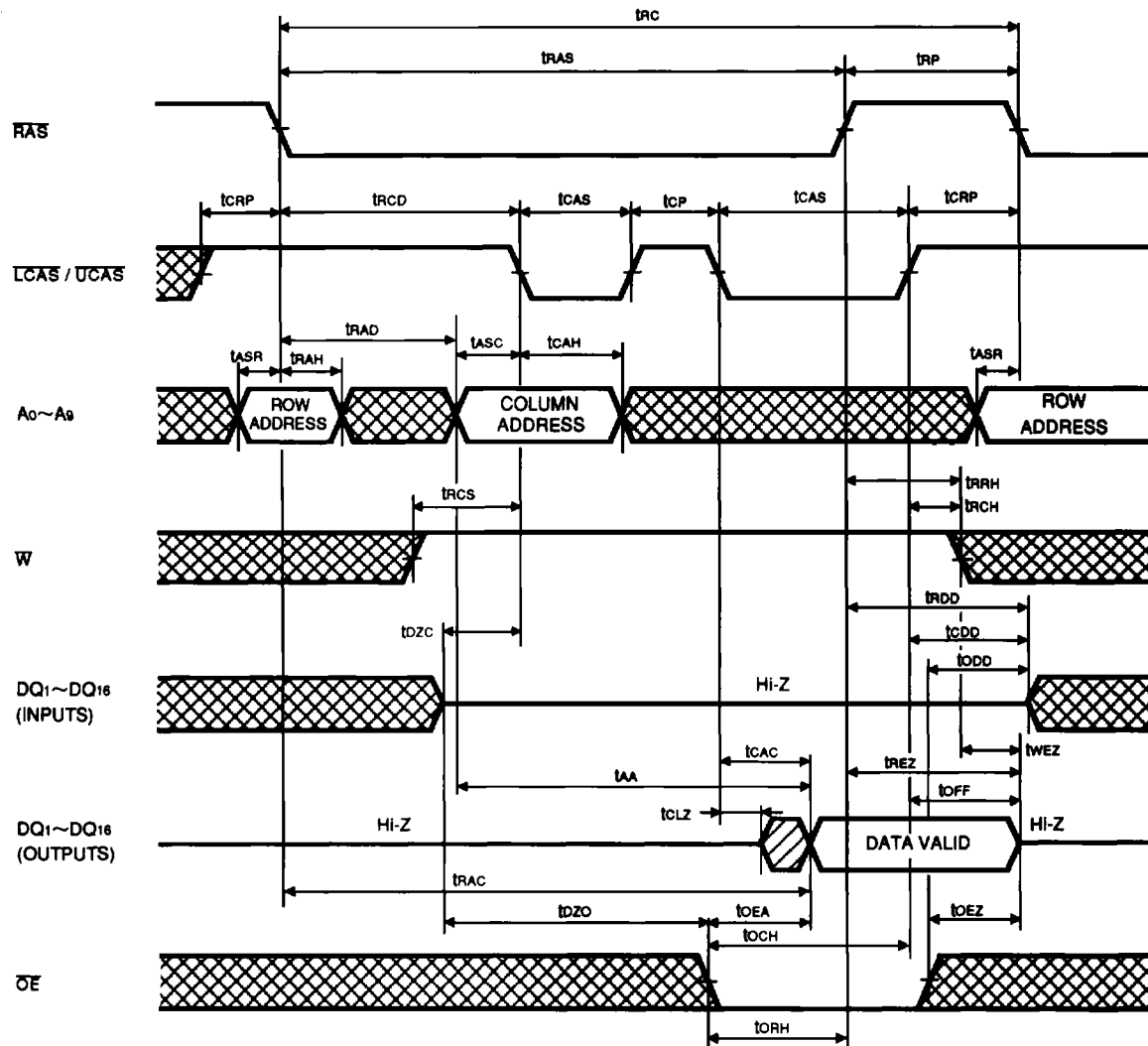
Note 27: Eight or more  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles instead of eight  $\overline{\text{RAS}}$  cycles are necessary for proper operation of  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh mode.

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**Timing Diagrams (Note 28)  
Read Cycle**



Note 28

	Indicates the don't care input.
	Indicates the invalid output.

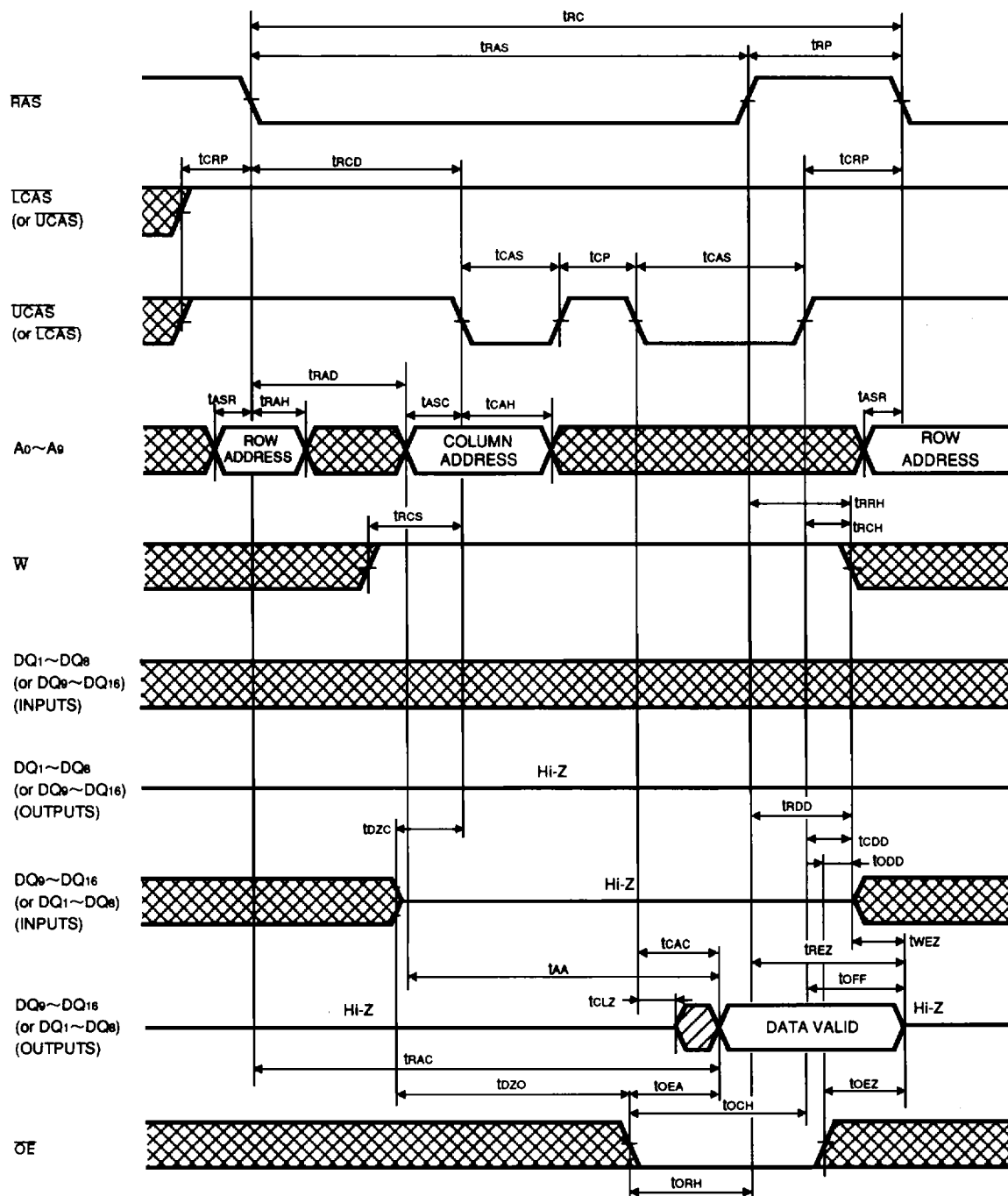


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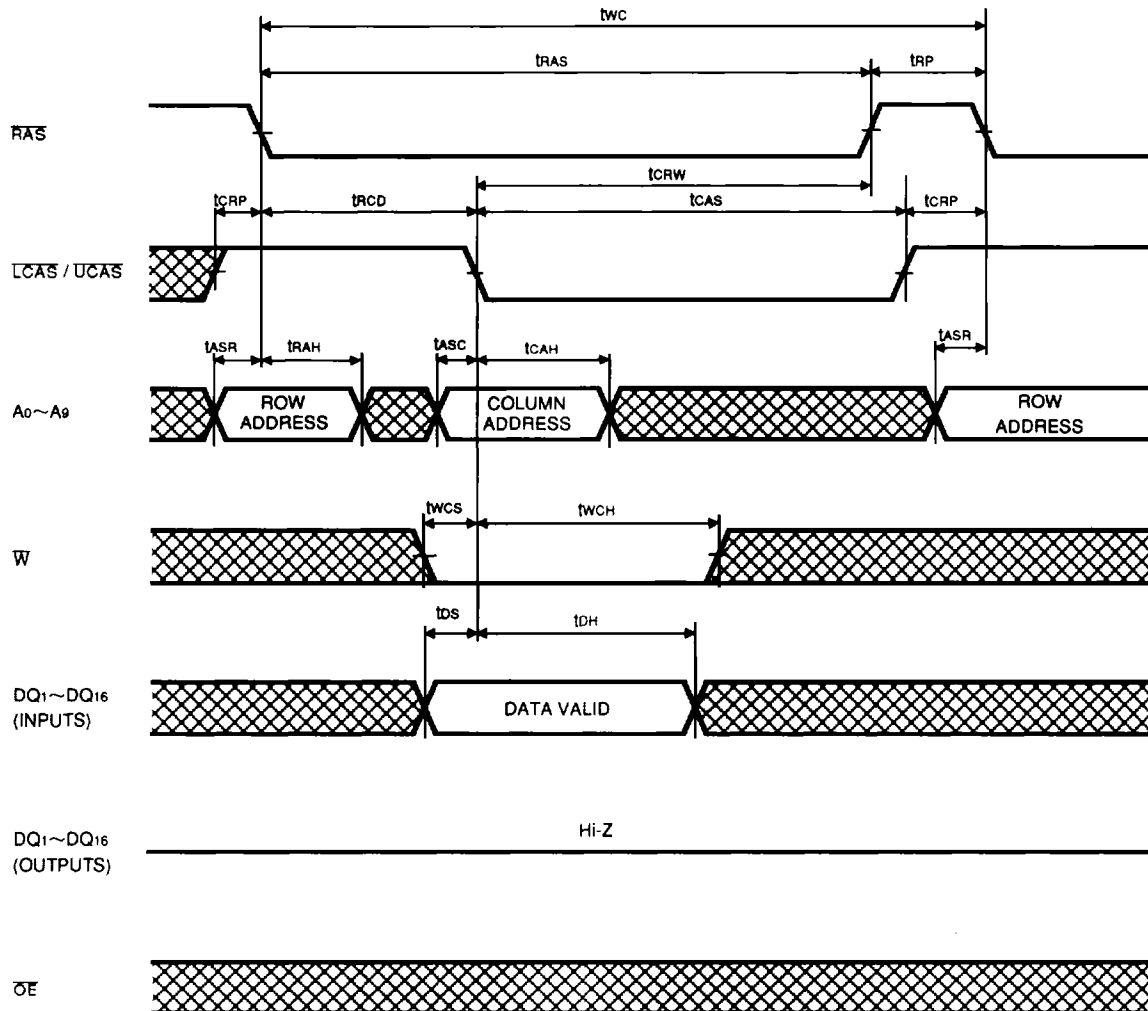
PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Byte Read Cycle



PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Write Cycle

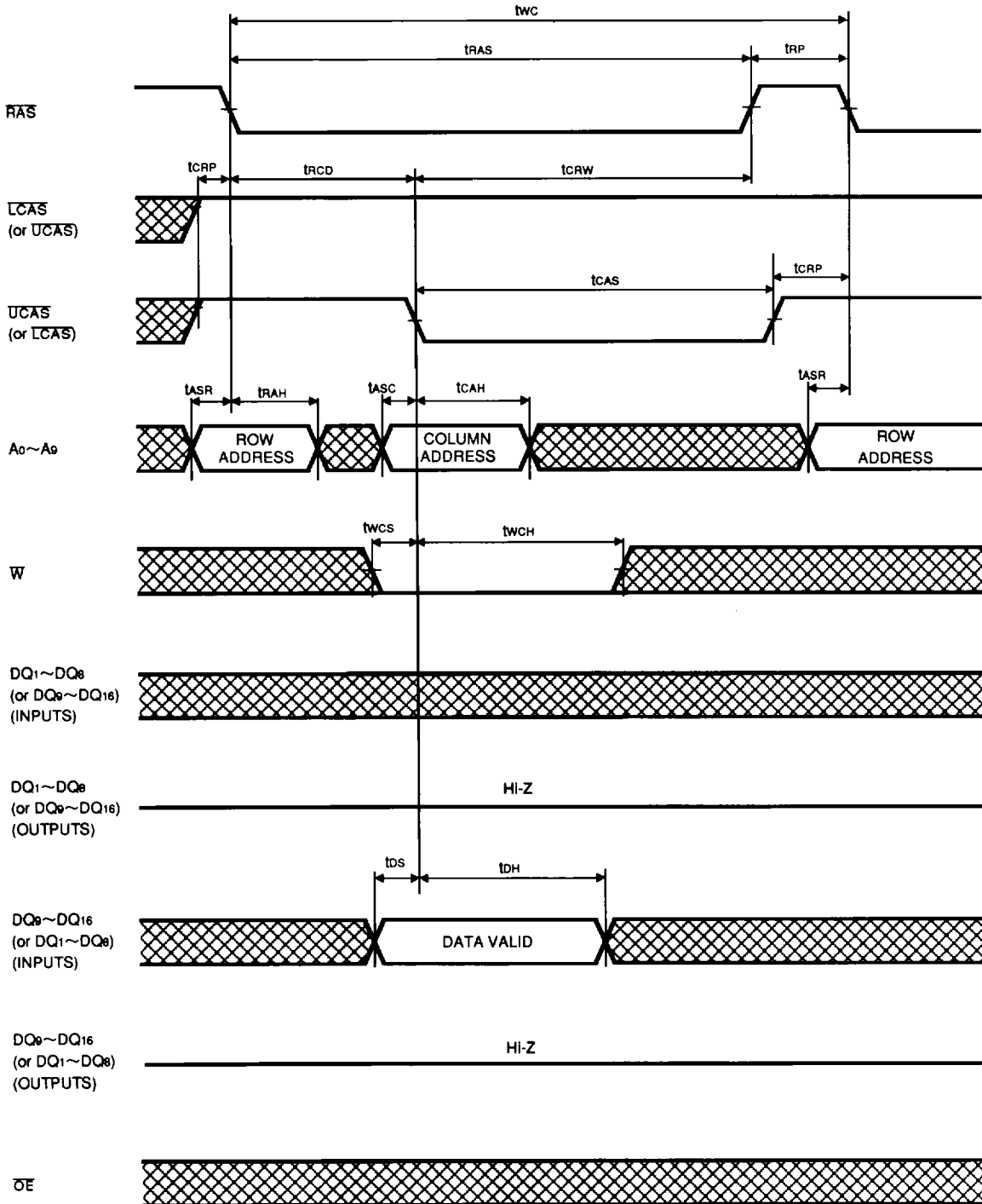


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PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

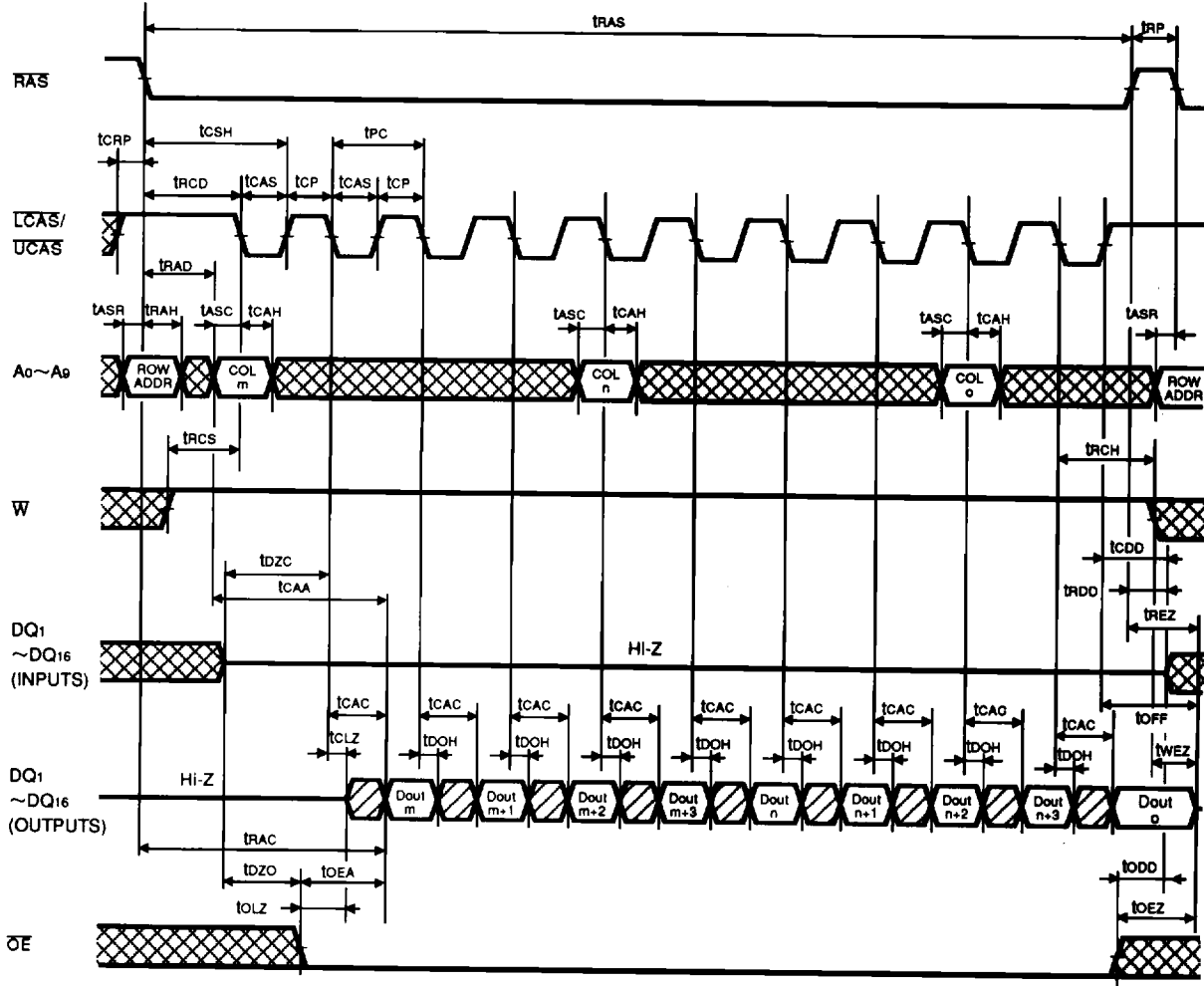
Byte Write Cycle



Notes: 1. Data is in a test condition.  
2. Some parameters' values are subject to change.

PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Pipeline Burst Mode Read Cycle (1)

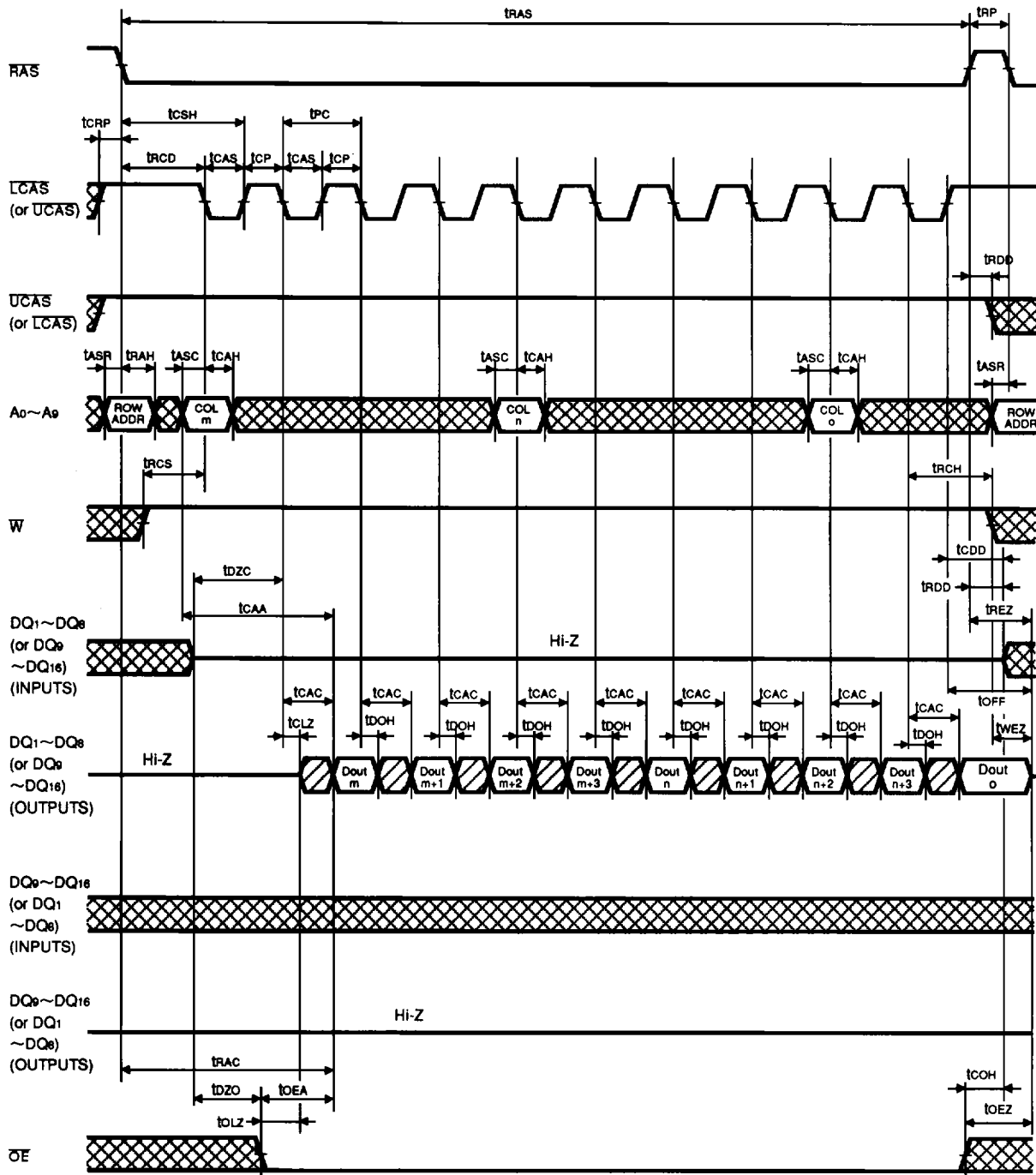


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**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

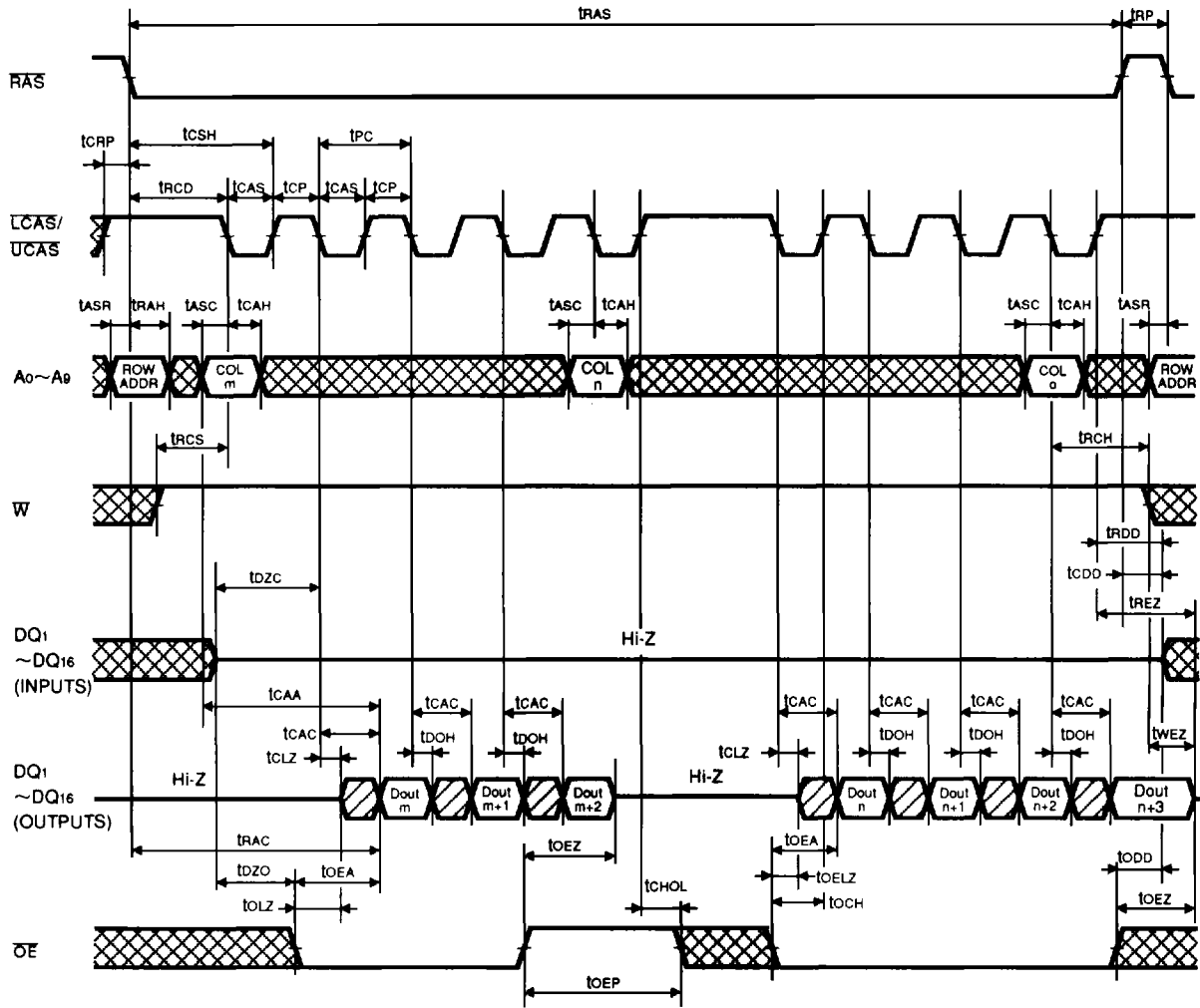
Pipeline Burst Mode Byte Read Cycle (1)



PRELIMINARY

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Pipeline Burst Mode Read Cycle (2)**

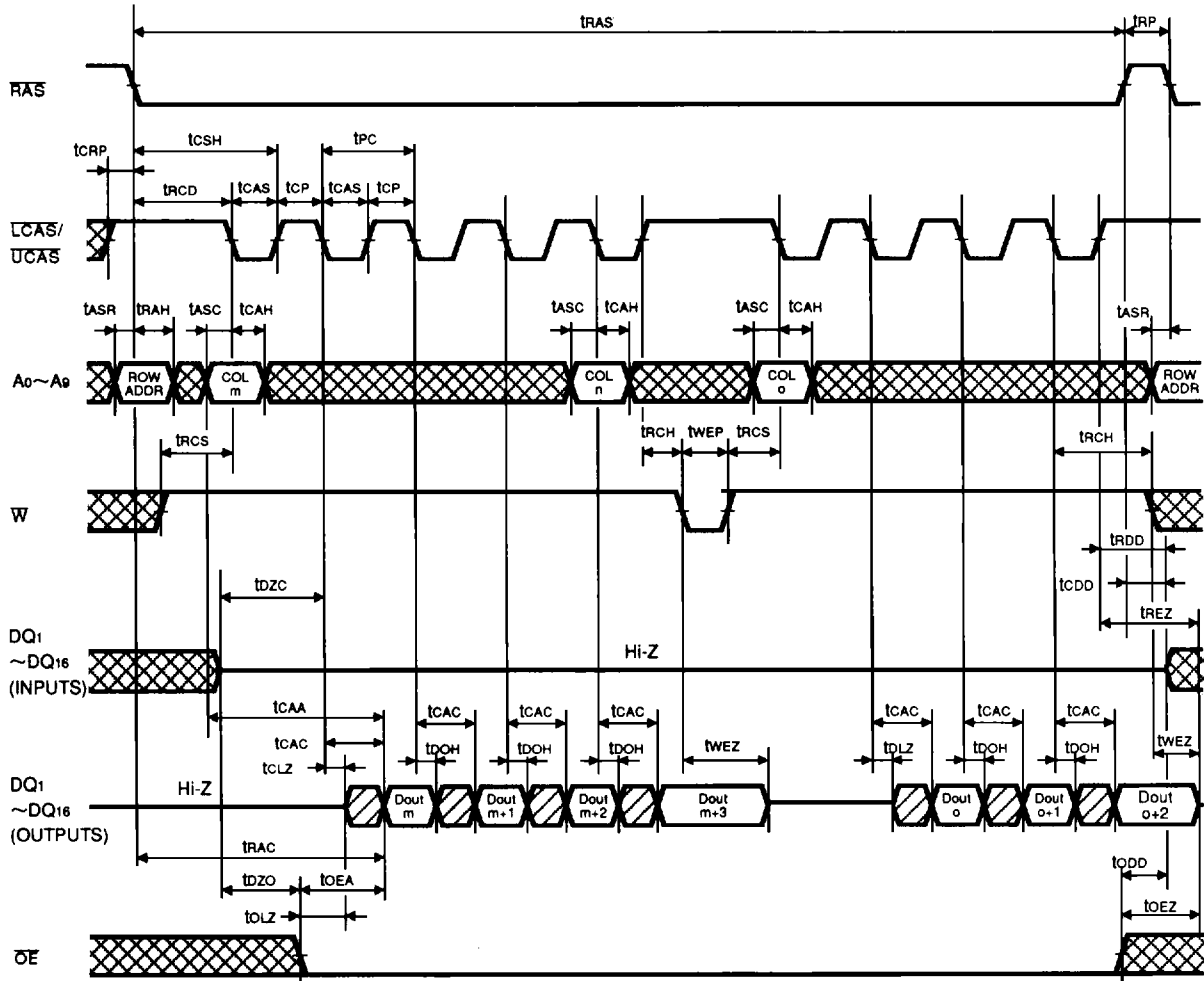


# M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

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## PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

### Pipeline Burst Mode Read Cycle (Read Terminated Read)



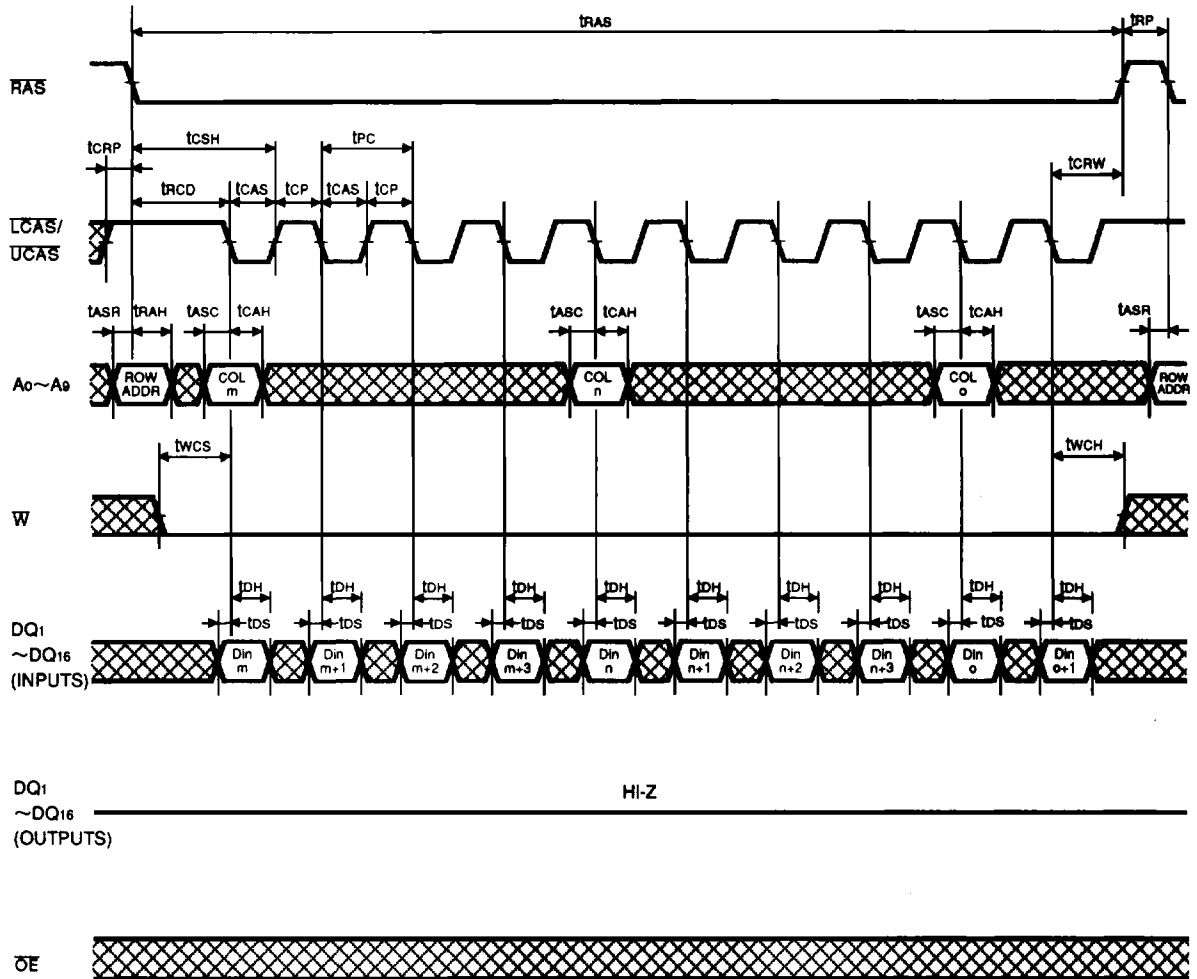
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# MITSUBISHI LSI<sup>®</sup> M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

## PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

### Pipeline Burst Mode Write Cycle

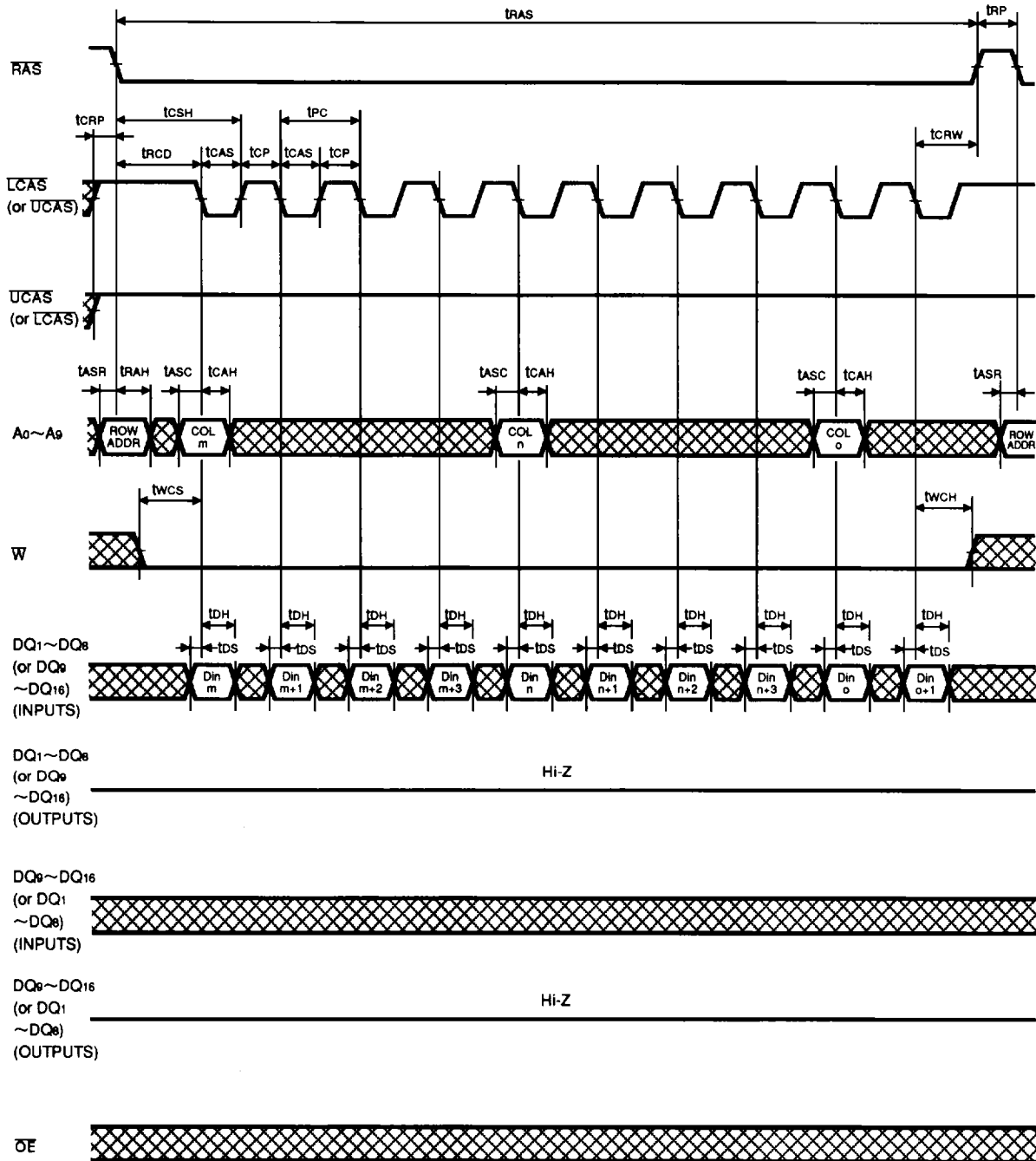




PRELIMINARY

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Pipeline Burst Mode Byte Write Cycle**



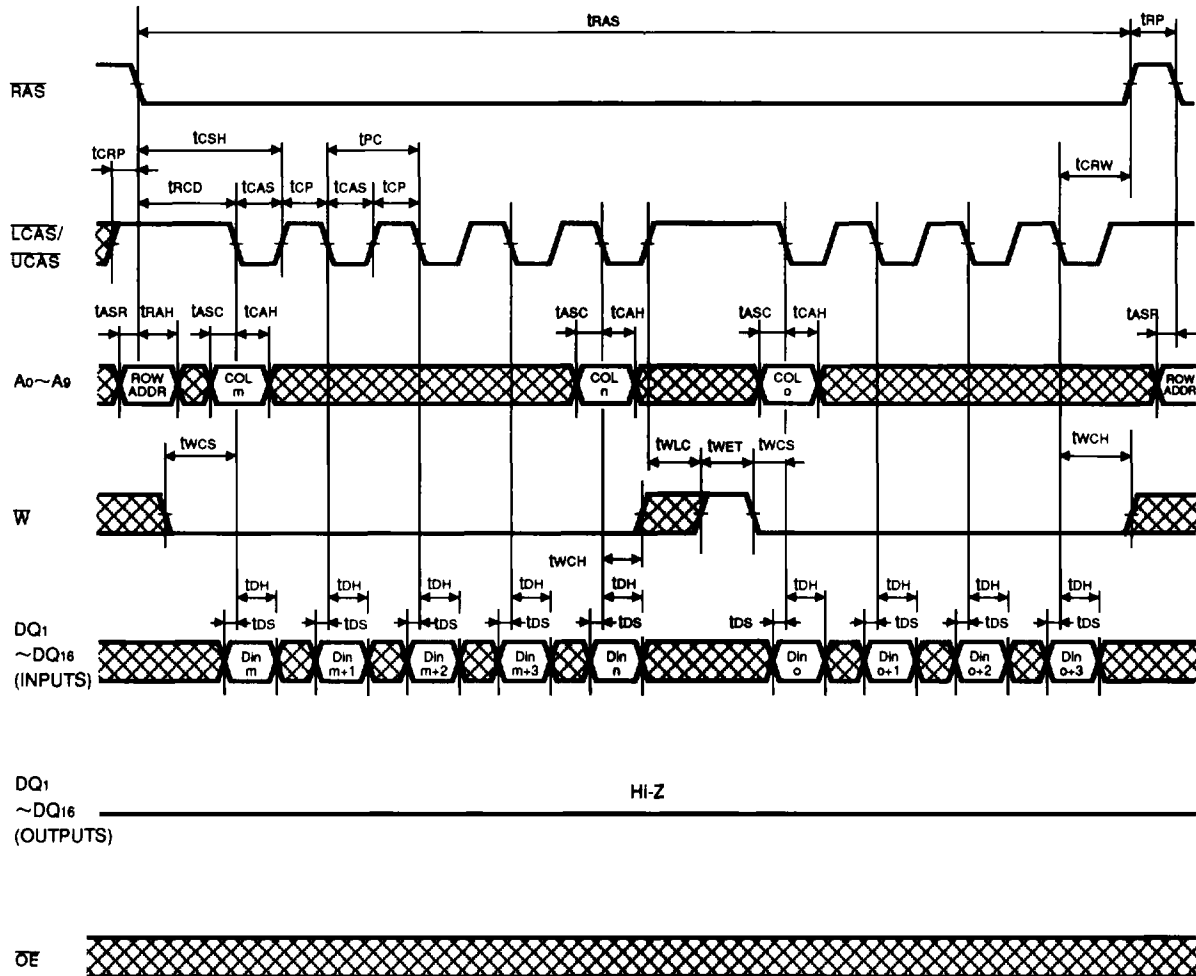
PRELIMINARY

MITSUBISHI LSI's

M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Pipeline Burst Mode Write Cycle (Write terminated Write)

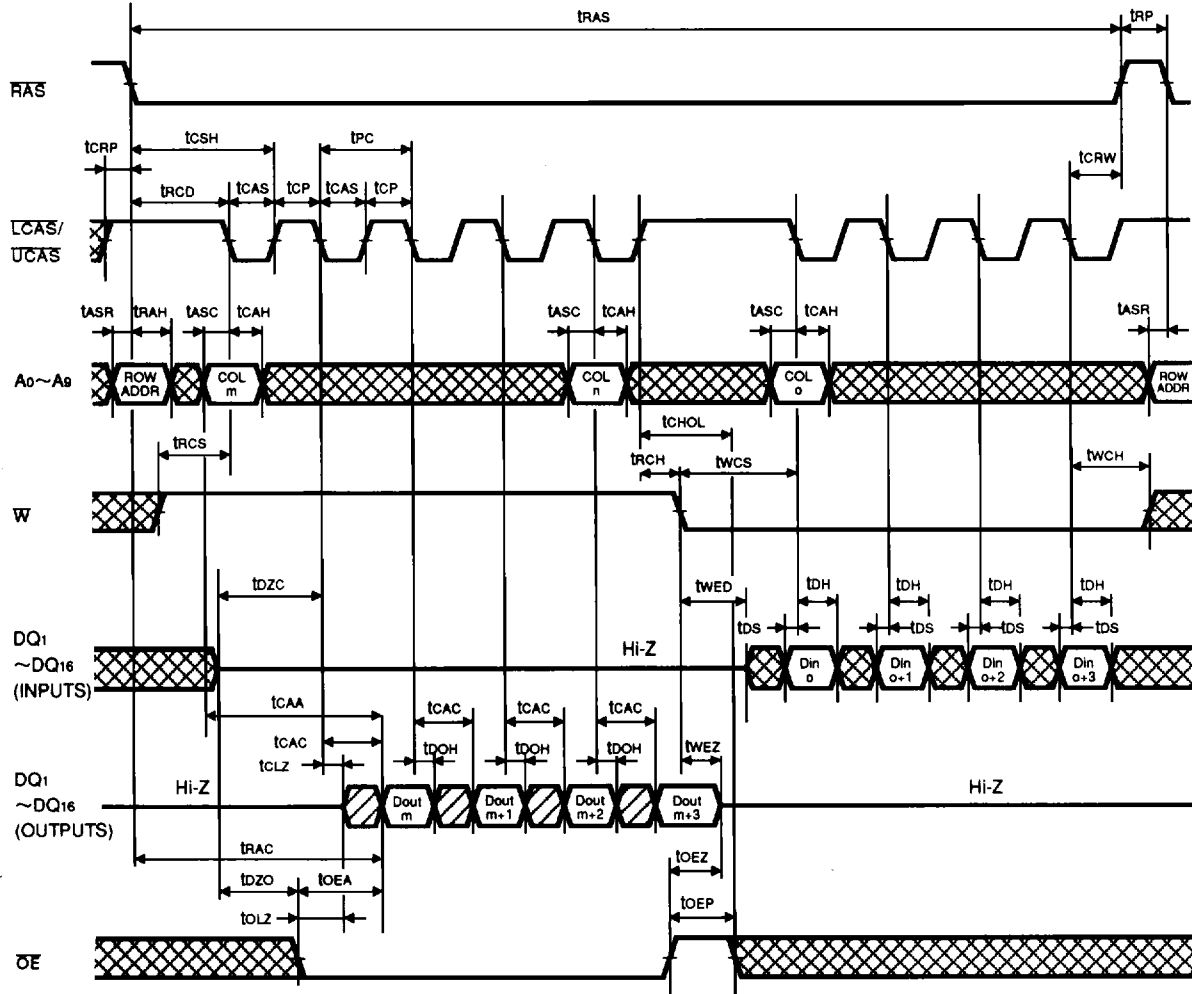


PRELIMINARY

MITSUBISHI LSIs  
**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Pipeline Burst Mode Read-Write Cycle**



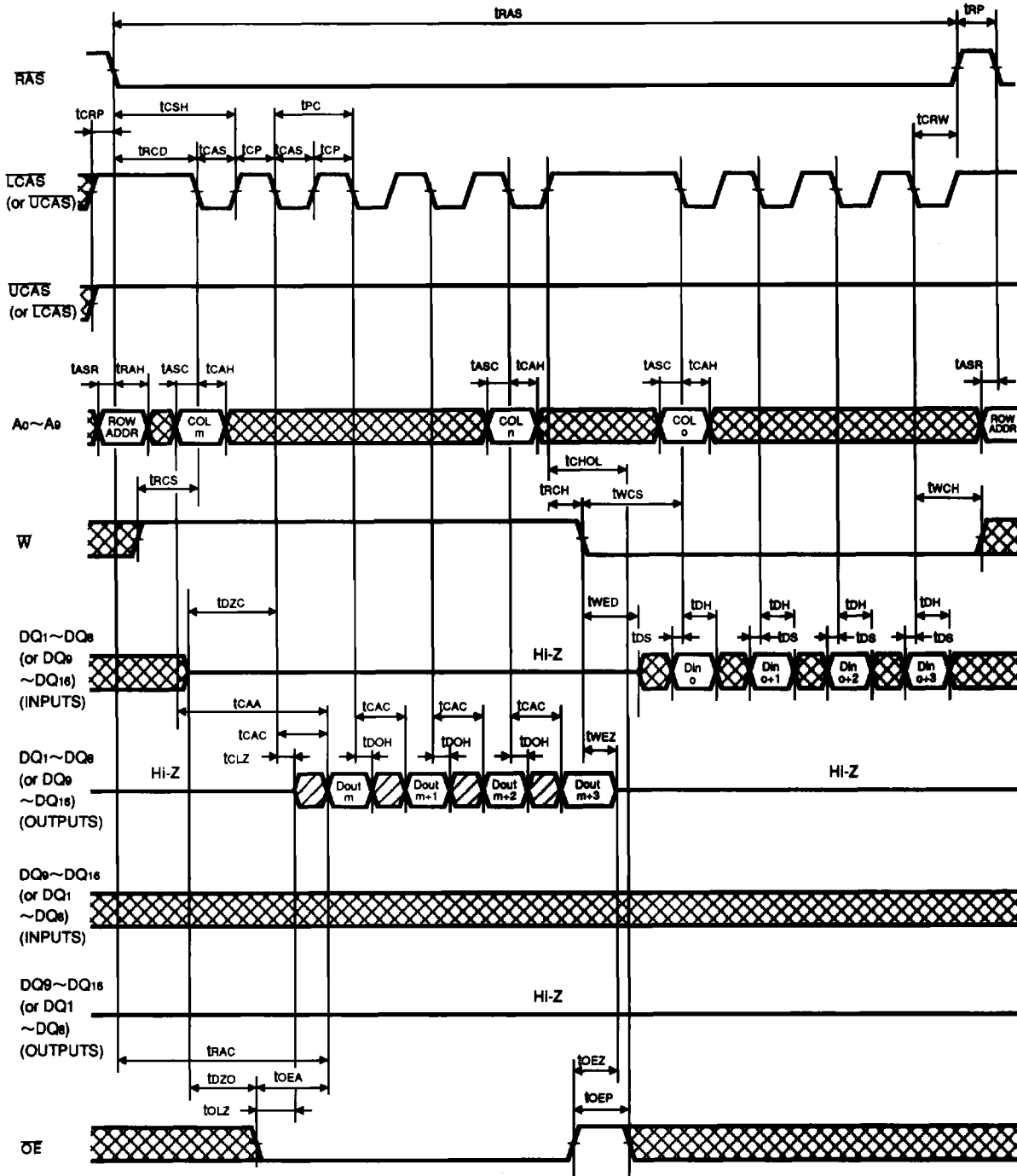
**PRELIMINARY**

*Notice: This is a preliminary drawing. Some parameters may be subject to change.*

# M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

## PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Pipeline Burst Mode Byte Read-Write Cycle



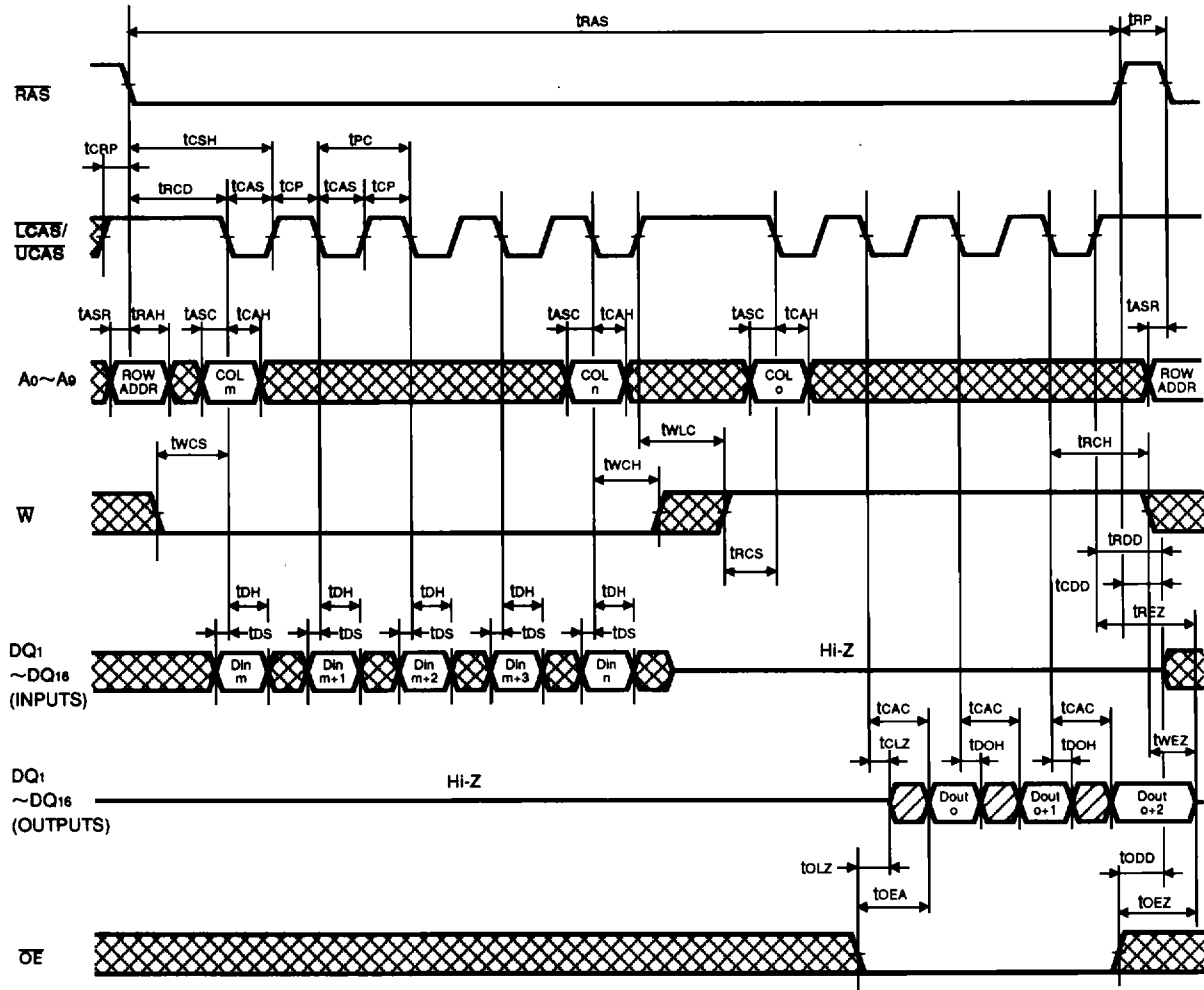
**PRELIMINARY**

Notice: This is not a final specification.  
Some parameters might be subject to change.

**MITSUBISHI LSIs**  
**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

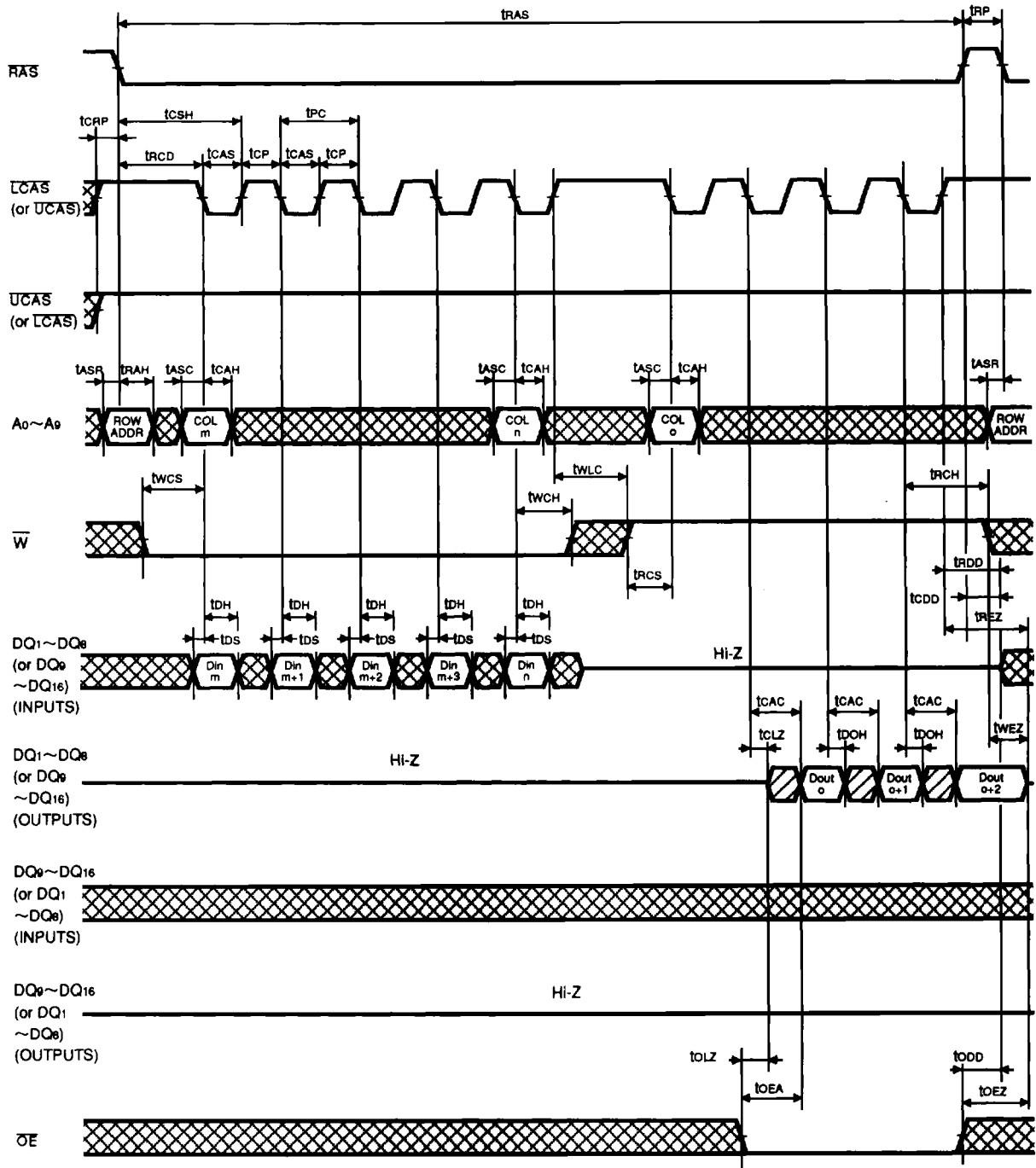
**Pipeline Burst Mode Write-Read Cycle**



PRELIMINARY

PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Pipeline Burst Mode Byte Write-Read Cycle



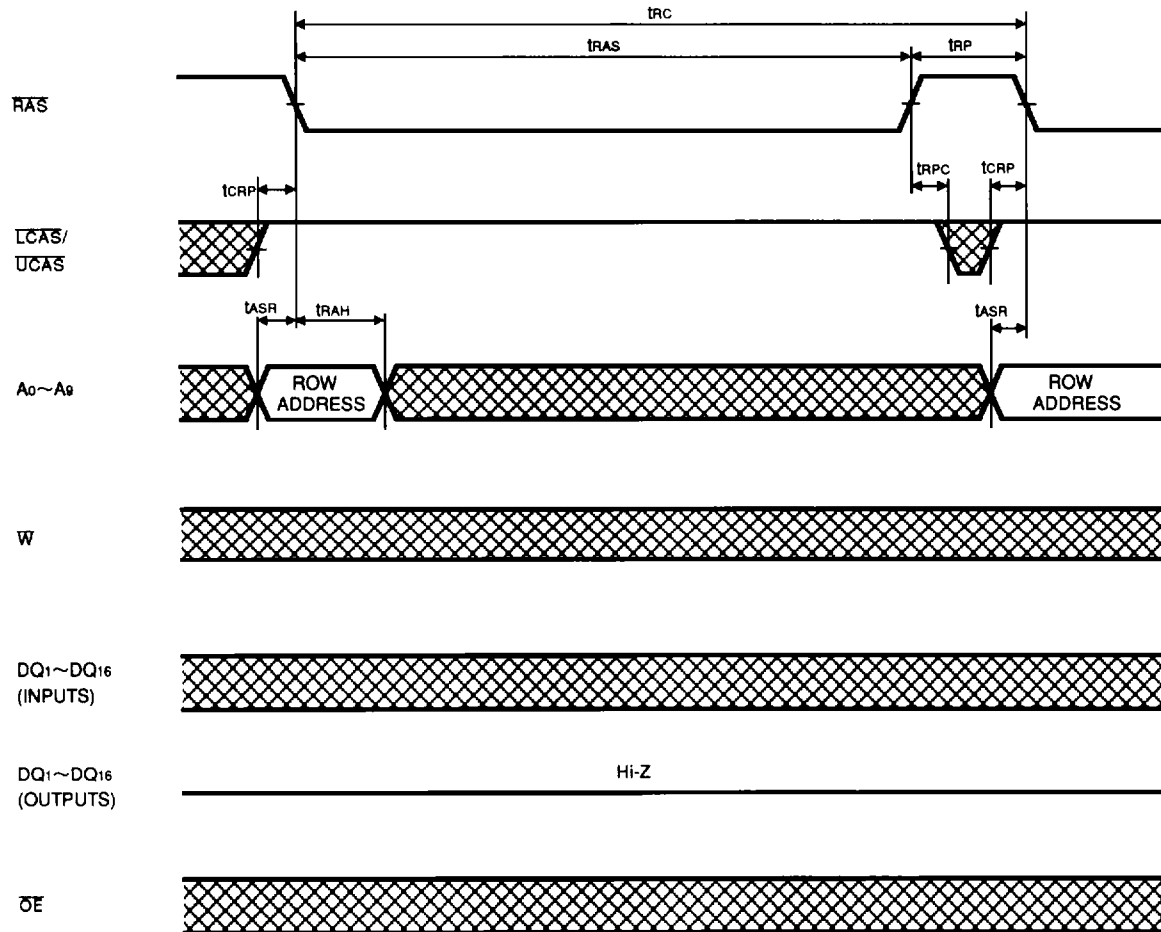
PRELIMINARY

MITSUBISHI LSIs

# M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## RAS-only Refresh Cycle



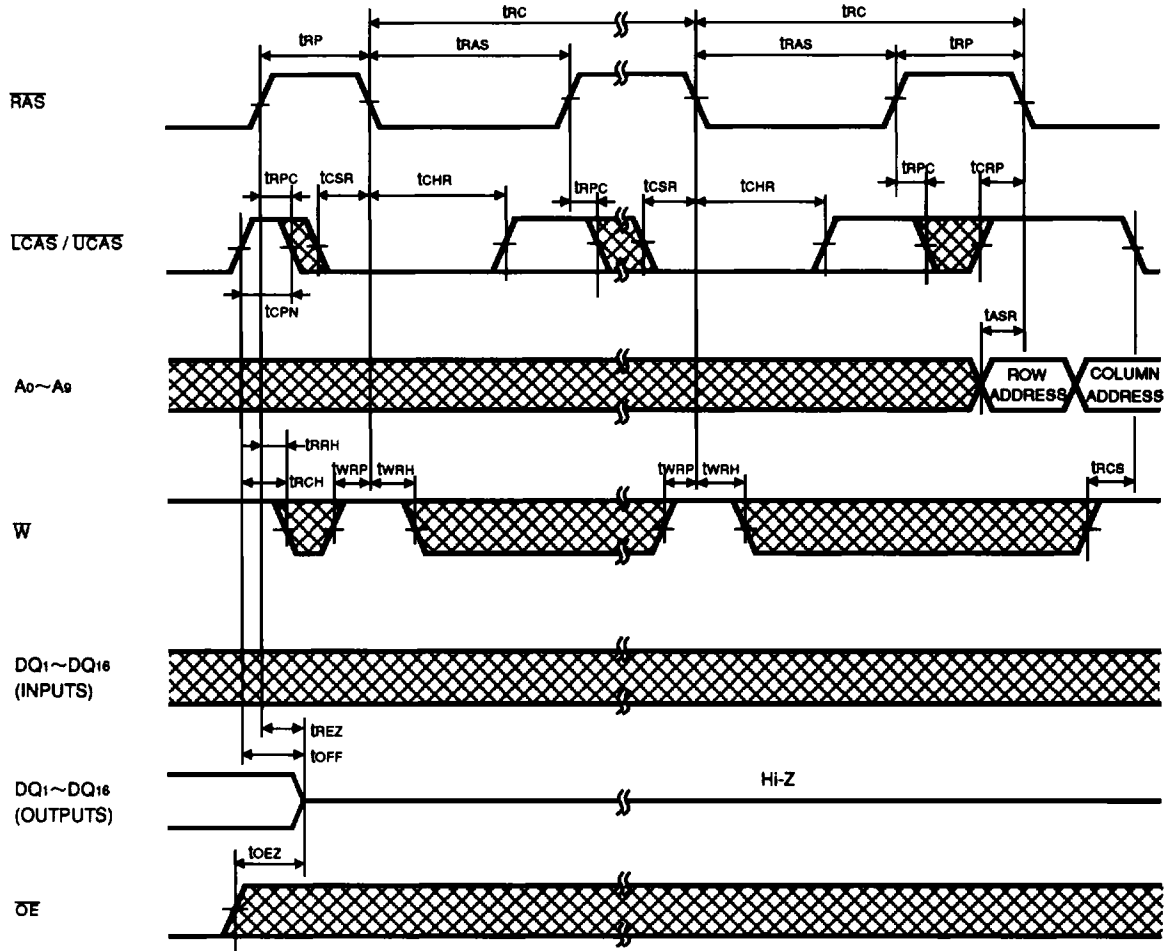
**PRELIMINARY**

Note: This is not a final specification.  
Some parameters might be subject to change.

**MITSUBISHI LSI**  
**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**CAS before RAS Refresh Cycle, Extended Refresh Cycle \***





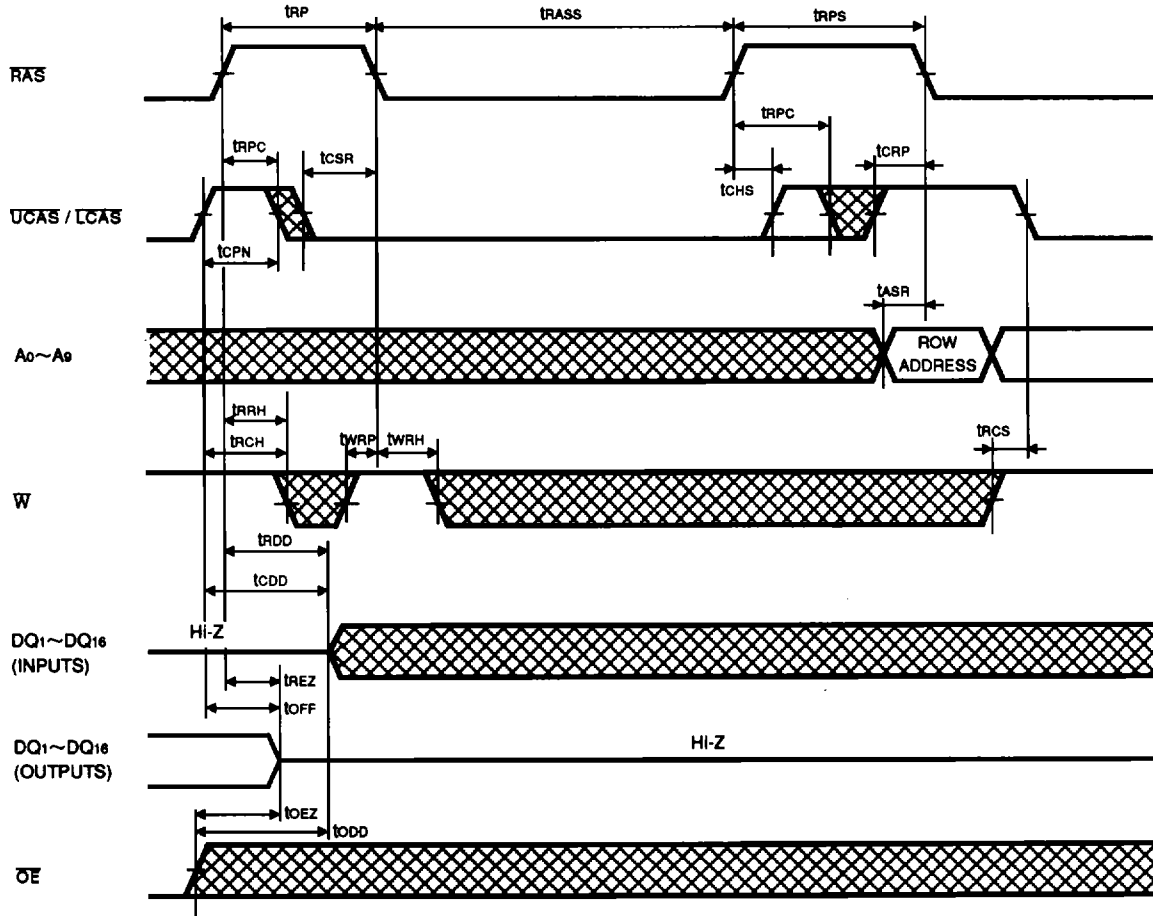
**PRELIMINARY**

Notice: This is not a final specification.  
Some parameter limits may be subject to change.

**MITSUBISHI LSI's**  
**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Self Refresh Cycle\***



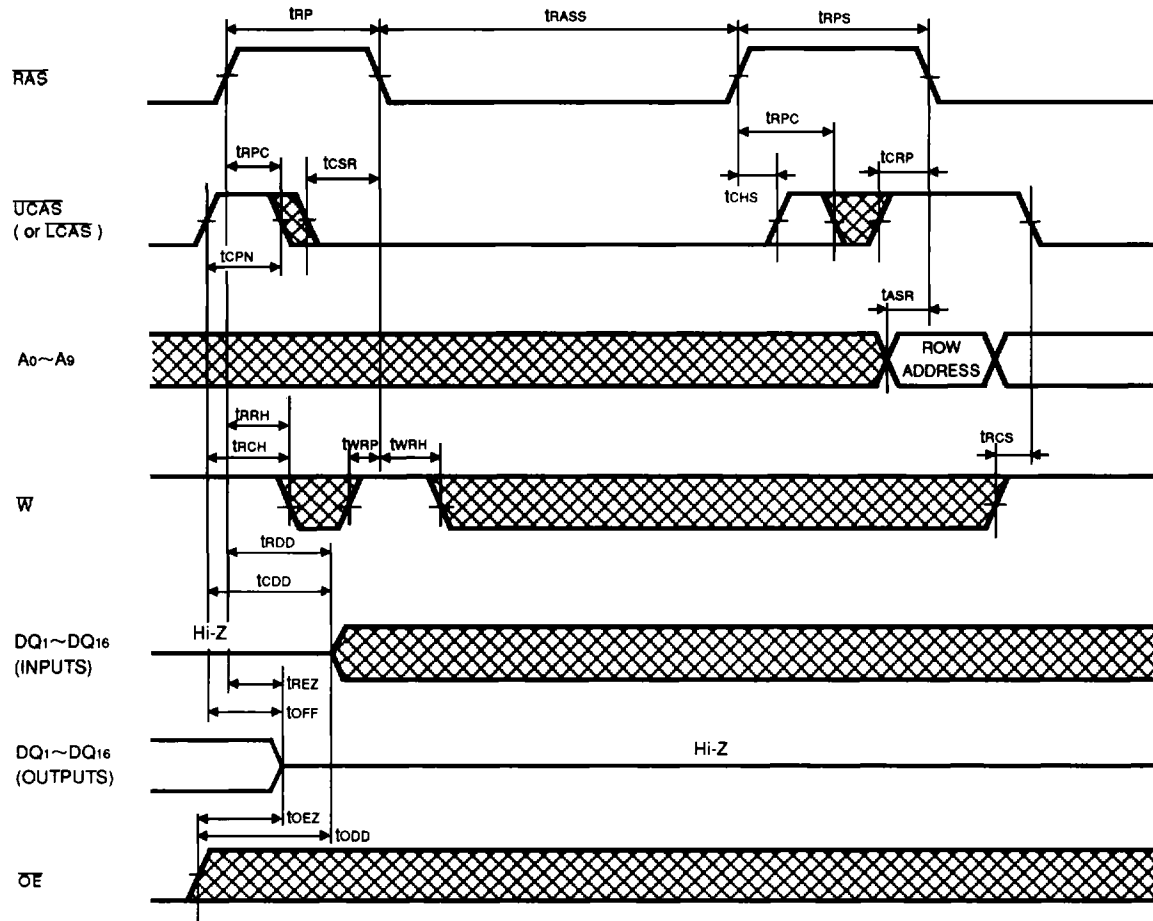
**PRELIMINARY**

本図は、最終的な仕様と異なる場合があります。  
Some parameters and waveforms are preliminary.

**MITSUBISHI LSI**  
**M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S**

**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Upper/(Lower) Self Refresh Cycle\***



**PIPELINE BURST MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**SELF REFRESH SPECIFICATIONS \***

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

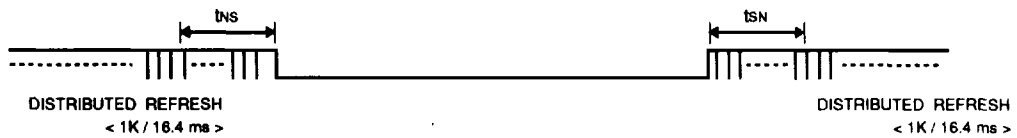
**TIMING REQUIREMENTS** ( $T_a=0\sim 70^{\circ}\text{C}$ ,  $V_{cc}=3.15\text{V}\sim 3.6\text{V}$ ,  $V_{ss}=0\text{V}$ , unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5S		M5M4V18167C-6S		M5M4V18167C-7S		
		Min	Max	Min	Max	Min	Max	
t <sub>RAS</sub>	Self Refresh RAS low pulse width	100		100		100		μs
t <sub>RPS</sub>	Self Refresh RAS high precharge time	90		110		130		ns
t <sub>CHS</sub>	Self Refresh RAS hold time	-50		-50		-50		ns

**SELF REFRESH ENTRY & EXIT CONDITIONS**

**(1) In case of distributed refresh**

The last / first full refresh cycles (1K) must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh, on the condition of t<sub>NS</sub> ≤ 16.4 ms and t<sub>SN</sub> ≤ 16.4 ms.



**(2) In case of burst refresh**

The last / first full refresh cycles (1K) must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh, on the condition of t<sub>NS</sub> + t<sub>SN</sub> ≤ 16.4 ms.

