64Mbit Single Operating Voltage Serial Flash Memory With 133 MHz Dual- or Quad-Output SPI Bus Interface

PRELIMINARY
NOVEMBER 2012

FEATURES

• Single Power Supply Operation
- Low voltage range: 2.3 V – 3.6 V

• Memory Organization
- IS25LQ064: 8192K x 8 (64 Mbit)

• Cost Effective Sector/Block Architecture
- 64Mb : Uniform 4KByte sectors / one hundred twenty eight uniform 32K/64KByte blocks

• Serial Peripheral Interface (SPI) Compatible
- Supports single-, dual- or quad-output
- Supports SPI Modes 0 and 3
- Maximum 50 MHz clock rate for normal read
- Maximum 133 MHz clock rate for fast read
- Maximum 532MHz clock rate equivalent Quad SPI
- Supports DTR Mode , Maximum 66MHz.

• Byte Program Operation
- Typical 8 us/Byte

• Page Program (up to 256 Bytes) Operation
- Typical 0.6 ms per page program

• Sector, Block or Chip Erase Operation
- Sector Erase (4KB)→25ms
- Block Erase (32KB)→0.25s
  (64KB)→ 0.5s
- Chip Erase →30 s (Max)

• Deep power-down mode

• Special Security function
- Safe guard function (Appendix 1)

• Support Serial Flash Discoverable Parameters (SFDP)mode

• Low Power Consumption
- Max 15 mA active read current
- Max 20 mA program/erase current
- Max 30uA standby current
- Max 1uA Deep power-down current.

• Hardware Write Protection
- Protect and unprotect the device from write operation by Write Protect (WP#) Pin

• Software Write Protection
- The Block Protect (BP3, BP2, BP1, BP0) bits allow partial or entire memory to be configured as read-only

• High Product Endurance
- Guaranteed 100,000 program/erase cycles per single sector
- Minimum 20 years data retention

• Industrial Standard Pin-out and Package
- 8-pin SOIC 208-mil
- 8-pin WSON
- 16-pin SOIC 300-mil
- 8-pin VSOP 208-mil
- Lead-free (Pb-free), package

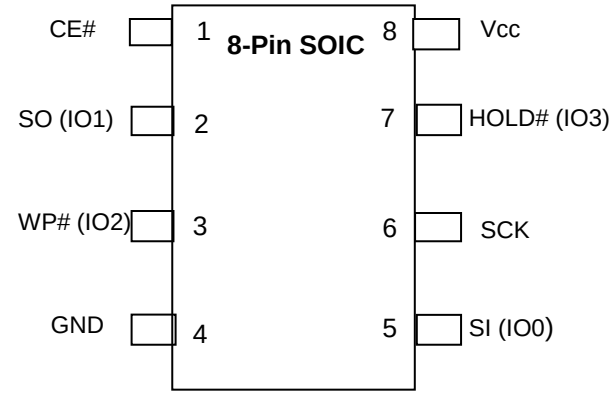
Additional 16+ 256*3 bytes Security information row one-time programmable (OTP) area (reserved 240 bytes)

GENERAL DESCRIPTION

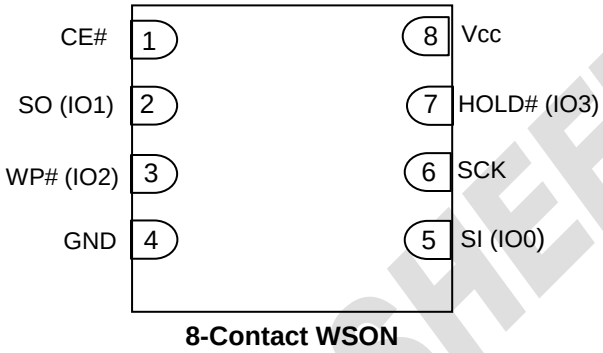
The IS25LQ064 are 64 Mbit Serial Peripheral Interface (SPI) Flash memories, providing single or quad-output. The devices are designed to support a 50 MHz clock rate in normal read mode, and 133 MHz in fast read, the fastest in the industry. The devices use a single low voltage power supply, ranging from 2.3 Volt to 3.6 Volt, to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers.

The IS25LQ064 are accessed through a 4-wire SPI Interface consisting of Serial Data Input/Output (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. The devices support page program mode, where 1 to 256 bytes data can be programmed into the memory in one program operation. These devices are divided into uniform 4 KByte sectors or 32K/64 KByte blocks.
The IS25LQ064 are manufactured on pFLASH™'s advanced non-volatile technology. The devices are offered in 8-pin SOIC 208mil and 8-contact WSON.

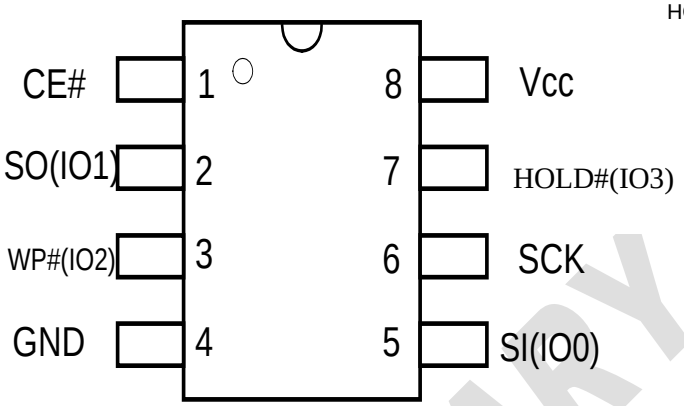
CONNECTION DIAGRAMS



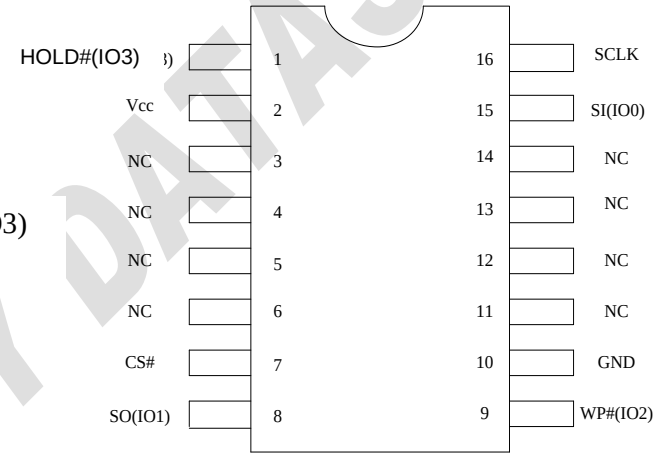
8-Pin SOIC



8-Contact WSON



8-Pin PDIP

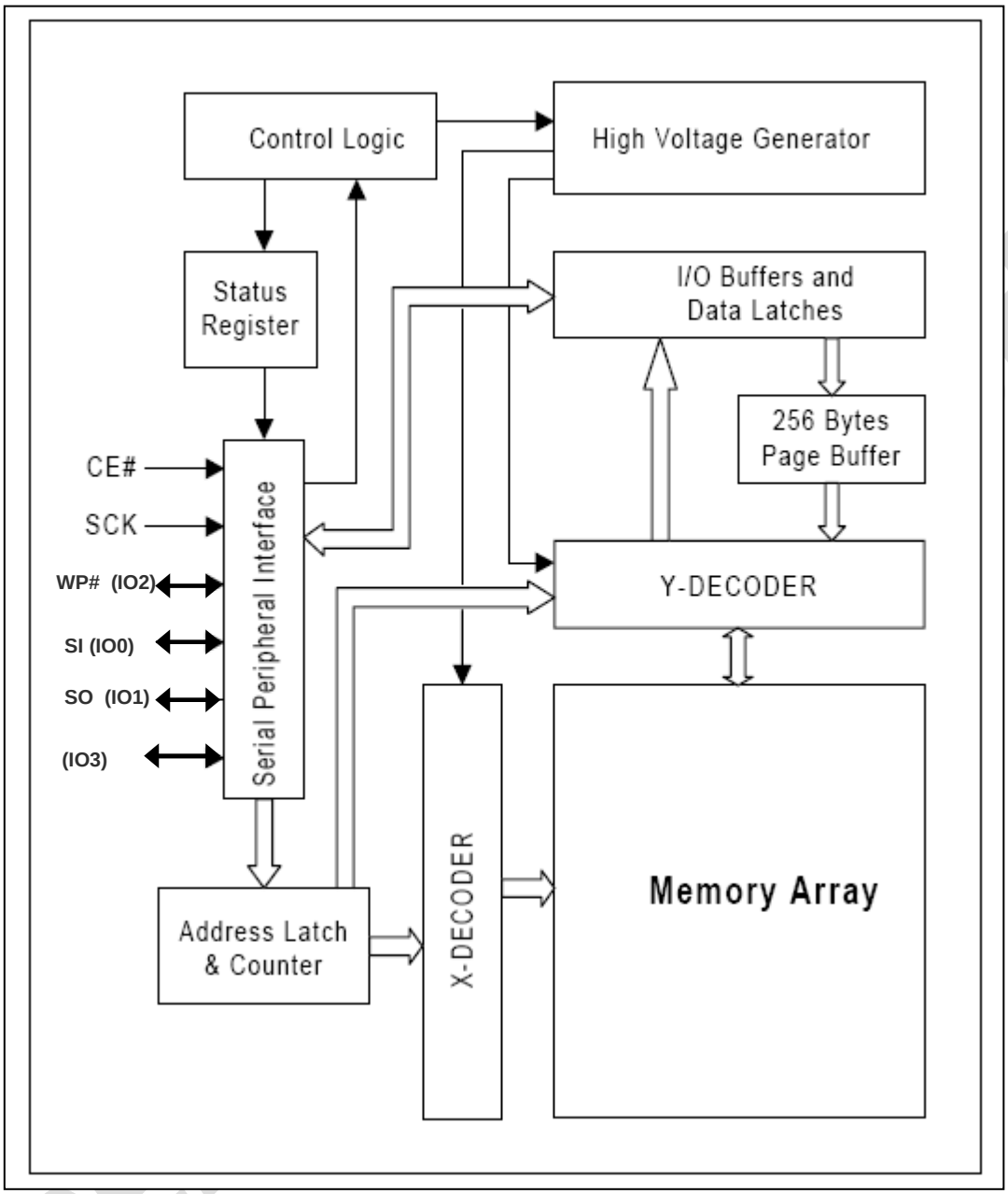


16-Pin SOIC

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# low activates the devices internal circuitries for device operation. CE# high deselects the devices and switches into standby mode to reduce the power consumption. When a device is not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI (IO0)	INPUT/OUTPUT	Serial Data Input/Output
SO (IO1)	INPUT/OUTPUT	Serial Data Input/Output
GND		Ground
Vcc		Device Power Supply
WP# (IO2)	INPUT/OUTPUT	Write Protect/Serial Data Output: A hardware program/erase protection for all or part of a memory array. When the WP# pin is low, memory array write-protection depends on the setting of BP3, BP2, BP1 and BP0 bits in the Status Register. When the WP# is high, the status register are not write-protected. When the QE bit of is set "1", the /WP pin (Hardware Write Protect) function is not available since this pin is used for IO2
Hold (IO3)	INPUT/OUTPUT	Hold: Pause serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register-2 is set for "1", the function is Serial Data Input & Output (for 4xI/O read mode)

BLOCK DIAGRAM



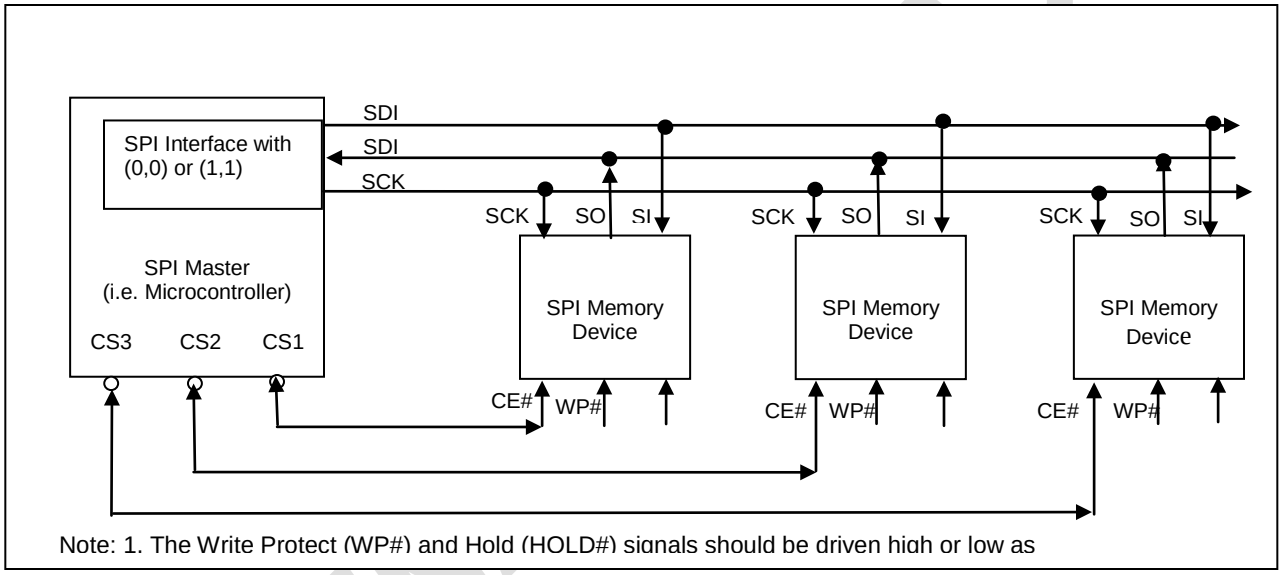
SPI MODES DESCRIPTION

Multiple IS25LQ064 devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity when the SPI master is in Stand-by mode: the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 2. For both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 1. Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Note: 1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven high or low as

Figure 2-1. SPI Modes Support

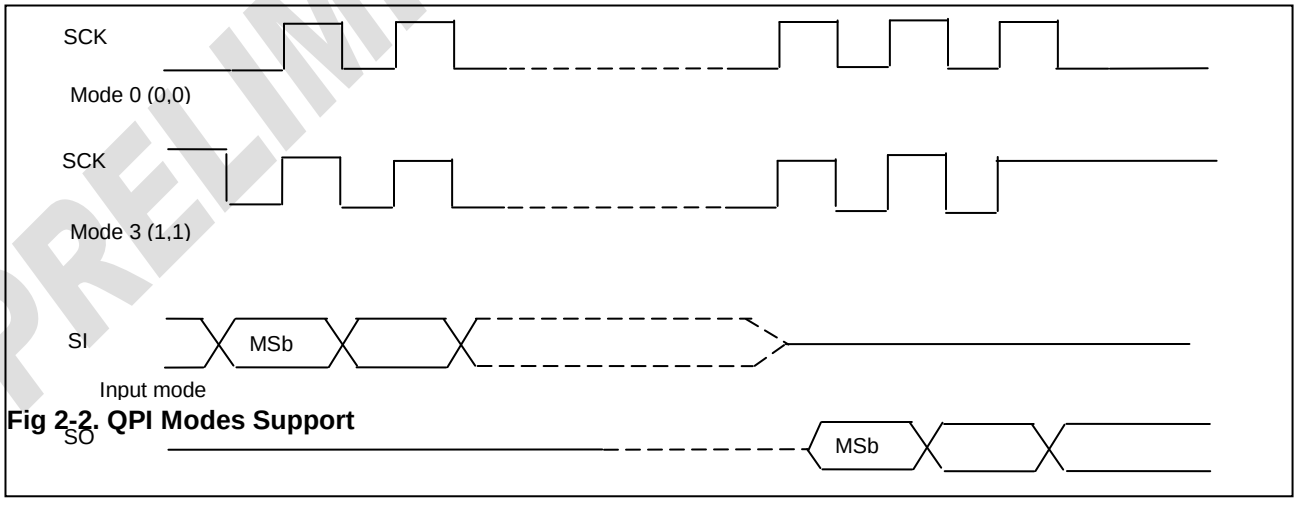
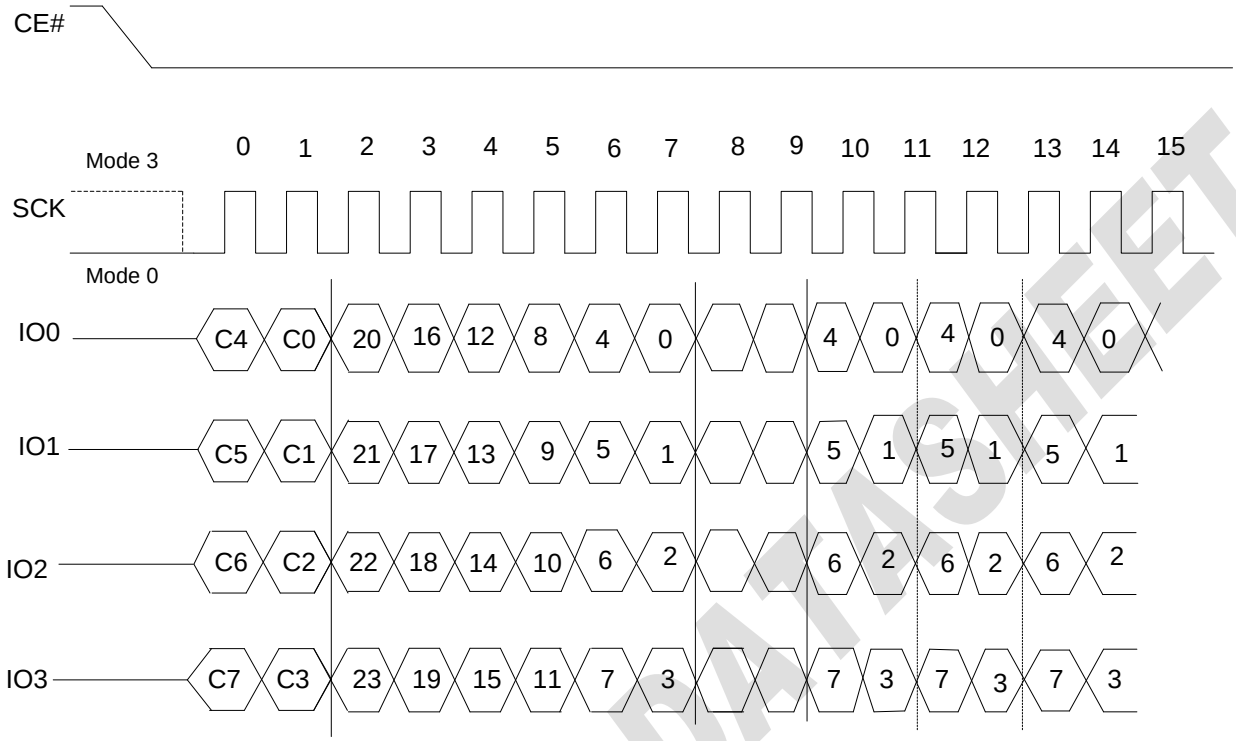


Fig 2-2. QPI Modes Support



SYSTEM CONFIGURATION

The IS25LQ064 devices are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the Motorola MC68HCxx series of microcontrollers or any SPI interface-equipped system controllers.

1. Configurable sector size: The memory array of
IS25LQ064 is divided into uniform 4 KByte sectors or uniform 32K/64 KByte blocks (a block consists of sixteen adjacent sectors).

Table 1 illustrates the memory map of the devices. The Configuration Register controls how the memory is mapped.

BLOCK/SECTOR ADDRESSES

Table 1. Block/Sector Addresses of IS25LQ064

Memory Density	Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (KBytes)	Address Range
64Mbit	Block 0	Block 0	Sector 0	4	000000h - 000FFFh
			:	:	:
		Block 1	:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Block 2	Sector 16	4	010000h - 010FFFh
			:	:	:
		Block 3	:	:	:
			Sector 31	4	01F000h - 01FFFFh
	Block 2	Block 4	Sector 32	4	020000h - 020FFFh
			:	:	:
		Block 5	:	:	:
			Sector 47	4	02F000h – 02FFFFh
	:	:	:	:	:
	Block 125	Block 250	Sector 1999	4	7D0000h – 7D0FFFh
			:	:	:
		Block 251	:	:	:
			Sector 2015	4	7DF000h – 7DFFFFh
	Block 126	Block 252	Sector 2016	4	7E0000h – 7E0FFFh
			:	:	:
		Block 253	:	:	:
			Sector 2031	4	7EF000h – 7EFFFFh
	Block 127	Block 254	Sector 2032	4	7F0000h – 7F0FFFh
			:	:	:
		Block 255	:	:	:
			Sector 2047	4	7FF000h – 7FFFFFh

REGISTERS (CONTINUED)

STATUS REGISTER

Refer to Tables 2 & 3 for Status Register Format and Status Register Bit Definitions.

The BP0, BP1, BP2, BP3 and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP2, BP1, BP0, and SRWD bits were set to "0" at factory. The Status Register can be read by the Read Status Register (RDSR). Refer to Table 10 for Instruction Set.

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is "0", the device is ready for a write status register, program or erase operation. When the WIP bit is "1", the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is "0", the write enable latch is disabled, and all write operations, including write status register, write configuration register, page program, sector erase, block and chip erase operations are inhibited. When the WEL bit is "1", write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically be the reset after the completion of a write instruction.

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Tables 7, 8 and 9 for the Block Write Protection bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.Note: a Chip Erase (CHIP_ER) instruction is executed only if all the Block Protection Bits are set as "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the status register that allows Quad operation. When the QE bit is set to "0",the pin WP# and HOLD# are enable. When the QE bit is set to "1", the pin IO2 and IO3 are enable.

WARNING: The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground.
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Table 2. Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default (flash bit)	0	0	0	0	0	0	0	0

***** The default value of the BP3, BP2, BP1, BP0, and SRWD bits were set to “0” at factory.

Table 3. Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates a write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No
Bit 2	BP0	Block Protection Bit: (See Tables 7, 8 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Yes
Bit 7	SRWD	Status Register Write Disable: (See Table 10 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Yes

REGISTERS (CONTINUED)

Function REGISTER
The function of Function Register bits are described as follows:

Top/Bottom Secection : Select BP 0~3 area starting from Top or Bottom. See Tables 7 and 8 for details

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is '1' after the host issues a suspend command during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to '0.'

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS is '1' after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the PSUS bit is reset to '0.'

IR lock bit 0 ~ 3: The information row lock bit is OTP type. If the bit set to "1", the information can not be programmed.

Table 4. Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0 (Reserved)	ESUS	PSUS	TBS	Reserved
Default	0	0	0	0	0	0	0	0

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	Reserved	Reserved	Reserved	Reserved
Bit 1	Top/Bottom Selection	Top/Bottom Selection. (See Tables 7 and 8 for details) "0" indicates Top area. "1" indicates Bottom area.	R/W	Yes(OTP)
Bit 2	PSUS	Program suspend bit: "0" indicates program is not suspend "1" indicates program is suspend	R	No
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	No
Bit 4	IR Lock 0 (Reserved)	Lock the information row 0: "0" indicates the information row can be program "1" indicates the information row can not be program	R/W	Yes(OTP)
Bit 5	IR Lock 1	Lock the information row 1: "0" indicates the information row can be program "1" indicates the information row can not be program	R/W	Yes(OTP)
Bit 6	IR Lock 2	Lock the information row 2: "0" indicates the information row can be program "1" indicates the information row can not be program	R/W	Yes(OTP)
Bit 7	IR Lock3	Lock the information row 3: "0" indicates the information row can be program "1" indicates the information row can not be program	R/W	Yes(OTP)

REGISTERS (CONTINUED)

Table 5. Top/Bottom Selection

T/B Selection = 0 , TOP area.

Status Register Bits				Protected Memory Area
BP3	**BP2**	**BP1**	**BP0**	**64 Mbit**
0	0	0	0	0(None)
0	0	0	1	1(1 block : 127th):
0	0	1	0	2(2 block : 126th and 127th)
0	0	1	1	3(4 blocks :124th to 127th)
0	1	0	0	4(8 blocks : 120th to 127th)
0	1	0	1	5(16 blocks :112th to 127th)
0	1	1	0	6(32 blocks :96th to 127th)
0	1	1	1	7(64 blocks :64th to 127th)
1	1	1	1	8(128 blocks :0th to 127th)
1	0	0	0	9(128 blocks :0th to 127th) All blocks
1	0	0	1	10(128 blocks :0th to 127th) All blocks
1	0	1	0	11(128 blocks :0th to 127th) All blocks
1	0	1	1	12(128 blocks :0th to 127th) All blocks
1	1	0	0	13(128 blocks :0th to 127th) All blocks
1	1	0	1	14(128 blocks :0th to 127th) All blocks
1	1	1	0	15(128 blocks :0th to 127th) All blocks

T/B Selection = 1 , Bottom area.

Status Register Bits				Protected Memory Area
BP3	**BP2**	**BP1**	**BP0**	**64 Mbit**
0	0	0	0	0(None)
0	0	0	1	1(1 block : 0th):
0	0	1	0	2(2 block : 0th and 1th)
0	0	1	1	3(4 blocks :0th and 3rd)
0	1	0	0	4(8 blocks : 0th to 7th)
0	1	0	1	5(16 blocks :0th to 15th)
0	1	1	0	6(32 blocks :0th to 31th)
0	1	1	1	7(64 blocks :0th to 63th)
1	1	1	1	8(128 blocks :0th to 127th)
1	0	0	0	9(128 blocks :0th to 127th) All blocks
1	0	0	1	10(128 blocks :0th to 127th) All blocks
1	0	1	0	11(128 blocks :0th to 127th) All blocks
1	0	1	1	12(128 blocks :0th to 127th) All blocks
1	1	0	0	13(128 blocks :0th to 127th) All blocks
1	1	0	1	14(128 blocks :0th to 127th) All blocks
1	1	1	0	15(128 blocks :0th to 127th) All blocks

REGISTERS (CONTINUED)

PROTECTION MODE

The IS25LQ064 have two types of write-protection mechanisms: hardware and software. These are used to prevent irrelevant operation in a possibly noisy environment and protect the data integrity.

HARDWARE WRITE-PROTECTION

The devices provide two hardware write-protection features:

a. When inputting a program, erase or write status register instruction, the number of clock pulse is checked to determine whether it is a multiple of eight before the executing. Any incomplete instruction command sequence will be ignored.

b. Write inhibit is 1.9 V, all write sequence will be ignored when Vcc drop to 1.9V and lower.

c. The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0 and SRWD in the Status Register. Refer to the STATUS REGISTER description.

SOFTWARE WRITE PROTECTION

The IS25LQ064 also provides two software write protection features:

a. Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.

b. The Block Protection (BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

Table 6. Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

DEVICE OPERATION

The IS25LQ064 utilize an 8-bit instruction register. Refer to Table 11 Instruction Set for details of the Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in.

The timing for each instruction is illustrated in the following operational descriptions.

REGISTERS (CONTINUED)

Read Parameters

Table 7. Read Parameter Table

	P7	P6	P5	P4	P3	P2	P1	P0
	Reserved	Reserved	Dummy Cycles	Dummy Cycles	Wrap Enable	Reserved	Wrap Length	Wrap Length
Default (flash bit)	0	0	0	0	0	0	0	0

Table 8. Burst Length data

	P1	**P0**
8 bytes	0	0
16 bytes	0	1
32 bytes	1	0
64 bytes	1	1

Table 9. Wrap Function

	P3
Enable	0
Disable	1

Table 10. Read Dummy Cycles.

Read Modes	**P5,P4 = 00**	**P5,P4 = 01**	**P5,P4 = 10**	**Max Freq**
Normal Read 03h	0	0	0	50MHz
Fast read 0Bh	8	8	8	133MHz
Dual IO Read BBh	4	4	8	4cc : 104MHz 8cc : 133MHz
Quad IO Read EBh	6	4	8	4cc : 84MHz 6cc : 103MHz 8cc : 133MHz

Table 11. Instruction Set

Instruction Name	Hex Code	Operation	Mode	Maximum Frequency
RD	03h	Read Data Bytes from Memory at Normal Read Mode	SPI	50 MHz
FR	0Bh	Read Data Bytes from Memory at Fast Read Mode	SPI , QPI	133 MHz
FRDIO	BBh	Fast Read Dual I/O	SPI	133MHz
FRQIO	EBh	Fast Read Quad I/O	SPI , QPI	133MHz
~~FRQIO4~~	~~E7h~~	~~Fast Read Quad I/O with 4 dummy cycles~~	~~SPI~~	~~133MHz~~
PP	02h	Page Program Data Bytes Into Memory	SPI , QPI	133 MHz
PPQ	38h	Page Program Data Bytes Into Memory with Quad interface	SPI	133 MHz
SER	D7h	Sector Erase	SPI , QPI	133 MHz
BER32 (32Kbyte)	52h	Block Erase 32K	SPI , QPI	133 MHz
BER64 (64Kbyte)	D8h	Block Erase 64K	SPI , QPI	133 MHz
CER	C7h/ 60h	Chip Erase	SPI , QPI	133 MHz
WREN	06h	Write Enable	SPI , QPI	133 MHz
WRDI	04h	Write Disable	SPI , QPI	133 MHz
RDSR	05h	Read Status Register	SPI , QPI	133 MHz
WRSR	01h	Write Status Register	SPI , QPI	133 MHz
RDFR	48h	Read function register	SPI	133MHz
WRFR	42h	Write function register	SPI	133MHz
QIOEN	35h	Enter Quad IO mode (QPI)	SPI	133MHz
QIODI	F5h	Exit Quad IO mode(QPI)	QPI	133MHz
PERSUS	B0h	Suspend during the program/erase	SPI , QPI	133MHz
PERRSM	30h	Resume program/erase	SPI , QPI	133MHz
PD	B9h	Deep power down mode	SPI , QPI	133 MHz
RDID	ABh	Read Manufacturer and Product ID/release Deep power down	SPI , QPI	133 MHz
SRP	C0h	Set Read Parameters	SPI , QPI	133MHz

RDJDID	9Fh	Read Manufacturer and Product ID by JEDEC ID Command	SPI , QPI	133 MHz
RDMDID	90h	Read Manufacturer and Device ID	SPI , QPI	133 MHz
RDIDQ	AFh	Read ID in QPI mode	QPI	133 MHz
RDSFDP	5Ah	SFDP Read	SPI , QPI	133 MHz
NOP	00h	No operation! Cancel the reset enable.	SPI , QPI	133MHz
RSTEN	66h	Soft ware reset enable	SPI , QPI	133MHz
RST	99h	Reset	SPI , QPI	133MHz
RSTM	FFh	Mode Reset	SPI , QPI	133MHz
IRER	64h	Erase Information Row	SPI	133MHz
IRP	62h	Program Information Row	SPI	133MHz
IRRD	68h	Read Information Row	SPI	133MHz
FRDTR	0Dh	Fast Read DTR Mode	SPI , QPI	133 MHz
FRDDTR	BDh	Fast Read Dual I/O DTR Mode	SPI	133MHz
FRQDTR	EDh	Fast Read Quad I/O DTR Mode	SPI , QPI	133MHz

SFDP (Serial Flash Discoverable Parameter) Definition Table

Address (Byte)	Data	Description	Comment
00h	53h	SFDP Signature	Fixed : 50444653h
01h	46h		
02h	44h		
03h	50h		
04h	00h	SFDP Minor Revision Number	Rev 1.0
05h	01h	SFDP Major Revision Number	
06h	00h	Number of Parameter Numbers	1 Parameter Number
07h	FFh	Resvered	
08h	00h	ID Number	JEDEC specified=00h
09h	00h	Parameter Table Minor Revision Number	Rev 1.0
0Ah	01h	Parameter Table Major Revision Number	
0Bh	09h	Parameter Table Length	9 DWORDs
0Ch	80h	JEDEC Parameter Table Pointer (PTP)	Point = 000030h
0Dh	00h		
0Eh	00h		
0Fh	FFh	Reserved	
10h	7Fh	Manufacturer ID	
11h	00h	Reserved	
12h	01h	Reserved	
13h	09h	Reserved	
14h	60h	pFLASH Parameter Table Pointer (PTP)	Point = 000060h
15h	00h		
16h	00h		
17h	FFh	Reserved	
30h	FFh	Bit[01:00]: Block/Sector Erase 00=Reserved 01= 4KB erase 10=Reserved	

		11=not support 4K erase Bit[2] : Write Granularity 0:1Byte ,1:64Byte or larer Bit[7:3] : Reserved	
31h	20h	Sector Erase OP Code (4KB)	
32h	B8h	Bit[0] : Reserved Bit[1] : (1-1-4) Fast Read 0=not support 1=support Bit[2] : (1-4-4) Fast Read 0=not support 1=support Bit[3] : (1-2-2) Fast Read 0=not support 1=support Bit[4] : Double Transfer Rate (DTR) 0=not support 1=support Bit[6:5] : Address Bytes Number Type 00:3Bytes 01:3 or 4 Bytes 10:4 Bytes 11:Reserved Bit[1] : (1-1-2) Fast Read 0=not support 1=support	
33h	FFh	Reserved	
34h	FFh	Flash Size 064Mb = 07FFFFFFh	
35h	FFh		
36h	FFh		
37h	07h		
38h	44h	Bit[4:0] : (1-4-4)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (1-4-4)Fast Read Number of Mode Bits 000b : Mode Bits not support	
39h	EBh	(1-4-4) Fast Read Opcode	
3Ah	00h	Bit[4:0] : (1-1-4)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (1-1-4)Fast Read Number of Mode Bits 000b : Mode Bits not support	

3Bh	FFh	(1-1-4) Fast Read Opcode	
3Ch	00h	Bit[4:0] : (1-1-2)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (1-1-2)Fast Read Number of Mode Bits 000b : Mode Bits not support	
3Dh	FFh	(1-1-2) Fast Read Opcode	
3Eh	04h	Bit[4:0] : (1-2-2)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (1-2-2)Fast Read Number of Mode Bits 000b : Mode Bits not support	
3Fh	BBh	(1-2-2) Fast Read Opcode	
40h	EEh	Bit[0] : (2-2-2) Fast Read 0=not support 1=support Bit[3:1] : Reserved Bit[4] : (4-4-4) Fast Read 0=not support 1=support Bit[7:5] : Reserved	
41h	FFh	Reserved	
42h	FFh	Reserved	
43h	FFh	Reserved	
44h	FFh	Reserved	
45h	FFh	Reserved	
46h	00h	Bit[4:0] : (2-2-2)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (2-2-2)Fast Read Number of Mode Bits 000b : Mode Bits not support	
47h	FFh	(2-2-2) Fast Read Opcode	
48h	FFh	Reserved	
49h	FFh	Reserved	
4Ah	00h	Bit[4:0] : (4-4-4)Fast Read Number of Dummy Cycles 0 0000b : Dummy cycles not support Bit[7:5] : (4-4-4)Fast Read Number of Mode Bits 000b : Mode Bits not support	
4Bh	FFh	(4-4-4) Fast Read Opcode	
4Ch	0Ch	Sector Type 1 Size (4KB)	
4Dh	20h	Sector Type 1 Opcode	

4Eh	0Fh	Sector Type 1 Size (32KB)	
4Fh	52h	Sector Type 1 Opcode	
50h	10h	Sector Type 1 Size (64KB)	
51h	D8h	Sector Type 1 Opcode	
52h	00h	Sector Type 1 Size (256KB) – Not support	
53h	FFh	Sector Type 1 Opcode	
60h 61h	00h 36h	Vcc Supply Maximum Voltage 2000h = 2.00V 2700h = 2.70V 3600h = 3.60V	
62h 63h	00h 23h	Vcc Supply Minimum Voltage 1650h = 1.65V 2300h = 2.30V 2700h = 2.70V	
64h 65h	9Dh F9h	Bit[0] : HW Reset# Pin 0=not support 1=support Bit[1] : HW Hold# Pin 0=not support 1=support Bit[2] : Deep Power Down Mode 0=not support 1=support Bit[3] : SW Reset 0=not support 1=support Bit[11:04] : SW Reset Opcode :99h Bit[12] : Power Suspend / Resume 0=not support 1=support Bit[13] : Erase Suspend / Resume 0=not support 1=support Bit[14] : Reserved Bit[15] : Wrap-Around Read Mode 0=not support 1=support	
66h	C0h	Wrap-Around Read Mode Opcode	
67h	64h	Wrap-Around Read data length 08h=support 8B Wrap-Around Read	

		16h=support 8B & 16B 32h=support 8B &16B & 32B 64h=support 8B & 16B & 32B & 64B	
68h 69h	D9h C8h	Bit[0] : Individual Block Lock 0=not support 1=support Bit[1] : Individual Block Lock bit 0=Volatile 1=Nonvolatile Bit[09:02] : Individual Block Lock Opcode : 36h Bit[10] : Individual Block Lock bit default status 0=protect 1=unprotect Bit[11] : Secured OTP 0=not support 1=support Bit[12] : Read Lock 0=not support 1=support Bit[13] : Permanent Lock 0=not support 1=support Bit[15:14] : Reserved	
6Ah	FFh	Reserved	
6Bh	FFh	Reserved	

DEVICE OPERATION (CONTINUED)

RD COMMAND (READ DATA) OPERATION

The Read Data (READ) instruction is used to read memory data of a IS25LQ064 under normal mode running up to 50 MHz.

The READ instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MS} (most significant address) - A0 are decoded. The remaining bits (A23 – A_{MS}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 12 for the related Address Key.

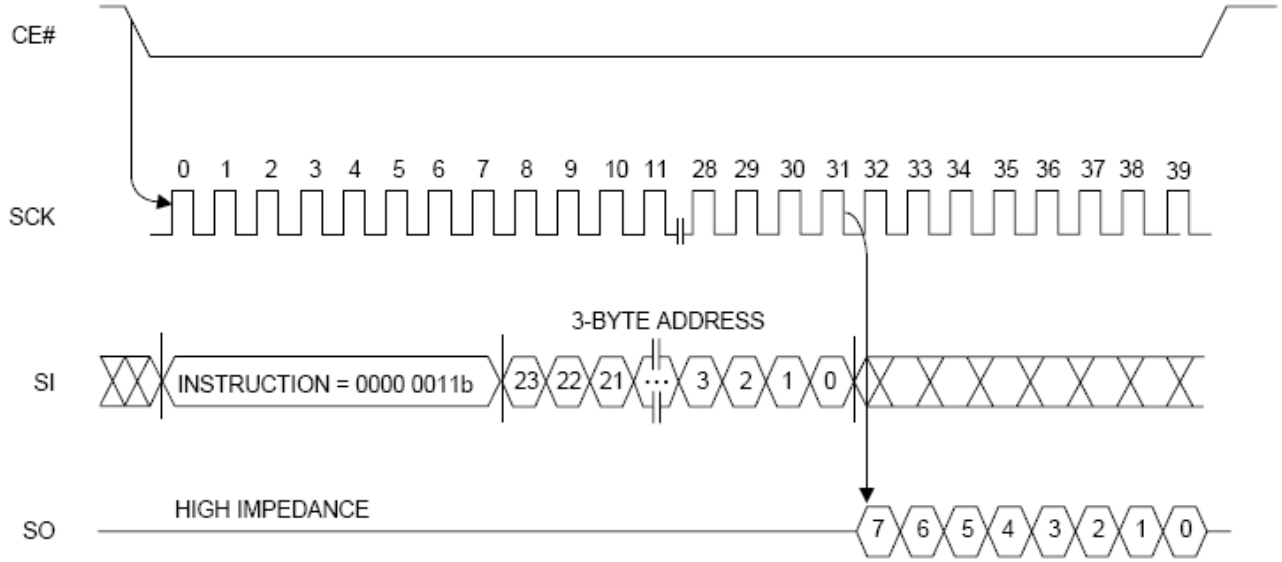
The first byte data (D7 - D0) addressed is then shifted out on the SO line, MSb first. A single byte of data, or up to the whole memory array, can be read out in one READ instruction. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (V_{IH}) after the data comes out. When the highest address of the devices is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Table 12. Address Key

Address	IS25LQ064
A_N (A_{MS} – A_0)	A23 - A0

Figure 1. Read Data Sequence



DEVICE OPERATION (CONTINUED)

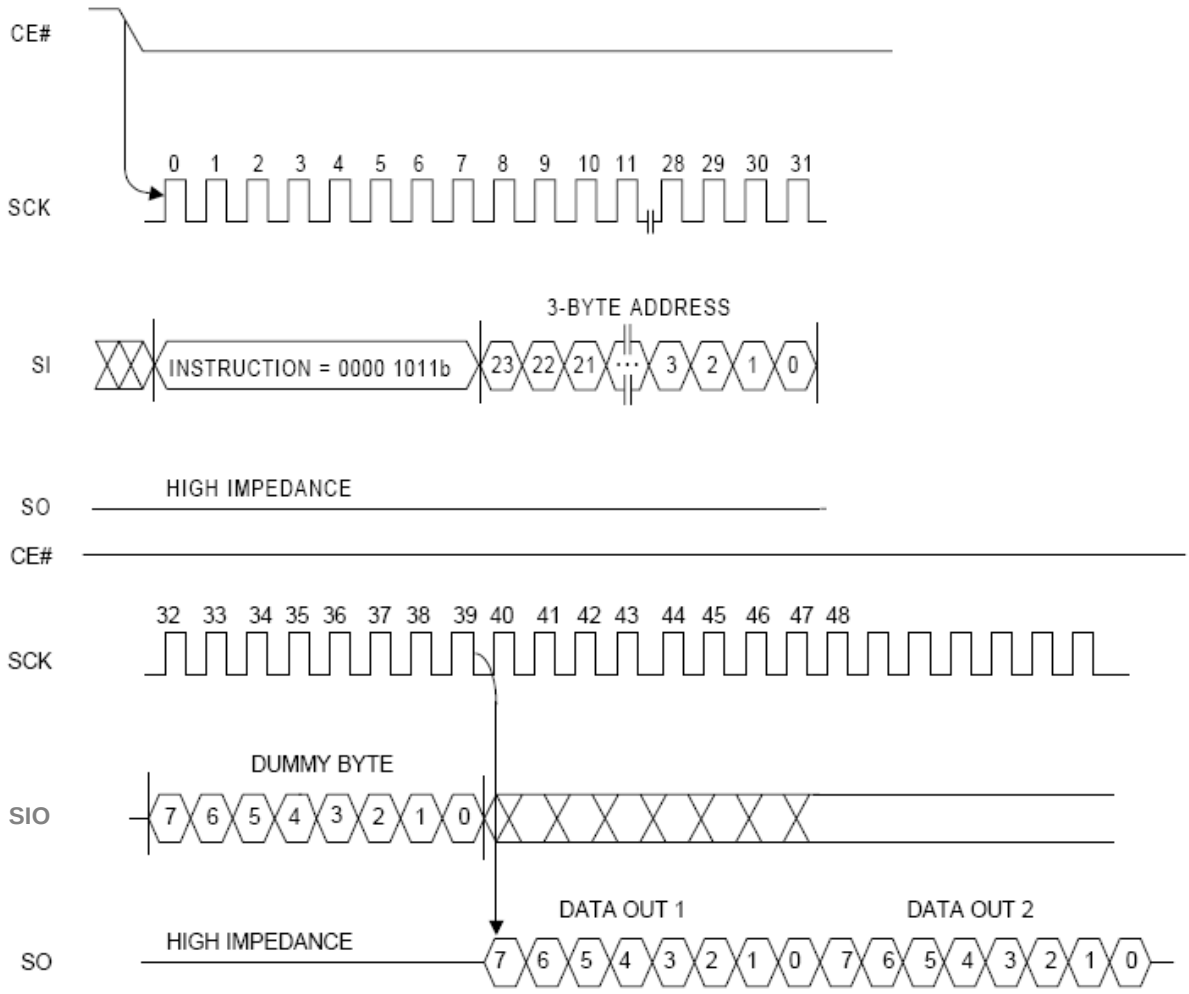
FR COMMAND (FAST READ DATA) OPERATION

The FAST_READ instruction is used to read memory data at up to a 133 MHz clock.

The FAST_READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST_READ instruction. The FAST_READ instruction is terminated by driving CE# high (V_{IH}). If a Fast Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 2. Fast Read Data Sequence



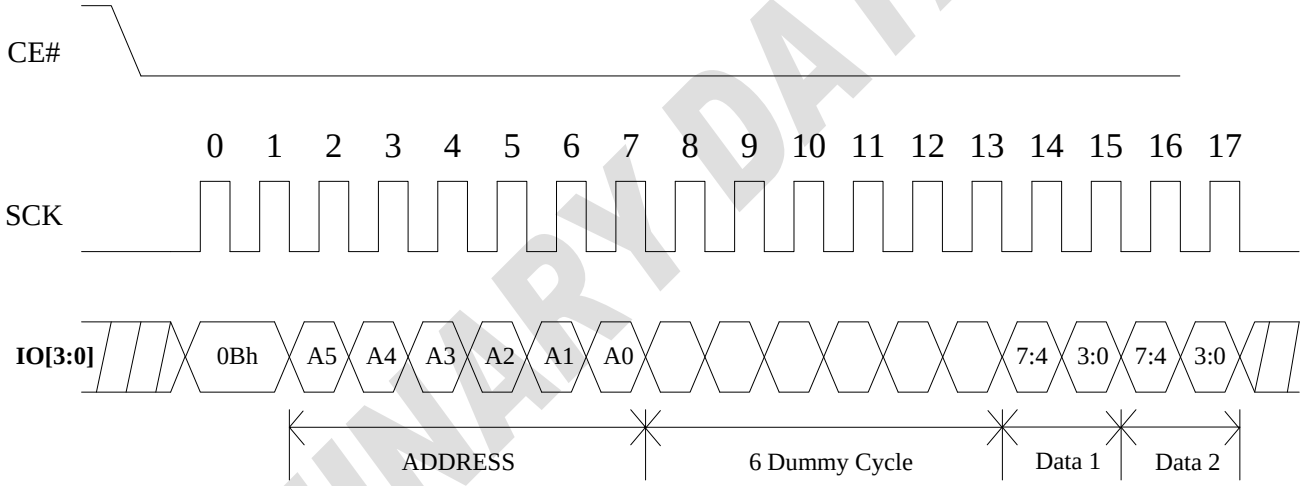
DEVICE OPERATION (CONTINUED)

FR QPI COMMAND (FAST READ DATA QPI) OPERATION

The QPI FAST_READ instruction is used to read memory data at up to a 133 MHz clock.

The FAST_READ instruction code(2 clocks) is followed by three address bytes (A23 - A0—6clocks) and mode bits, dummy byte (4clocks), transmitted via the QPI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.
.
The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST_READ instruction. The FAST_READ instruction is terminated by driving CE# high (V_{IH}). If a Fast Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 3. Fast Read Data Sequence , QPI Mode



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

DEVICE OPERATION (CONTINUED)

FRDIO COMMAND (FAST READ DUAL I/O) OPERATION

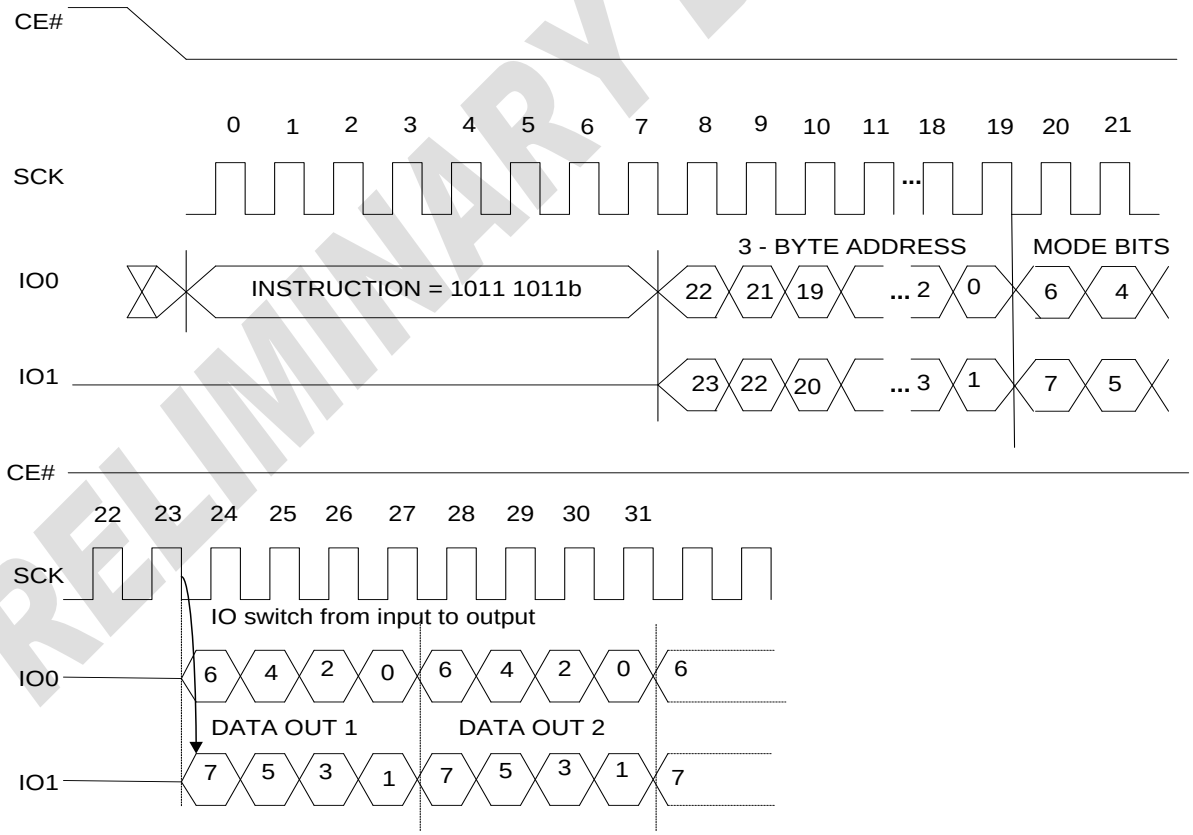
The FRDIO allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRDIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO0 and IO1 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSb is input on IO1, the next bit on IO0, and continues to shift in alternating on the two lines. The mode byte contains the value Ax, where x is a "don't care" value. Then the first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The MSb is output on IO1, while simultaneously the second bit is output on IO0. Figure 15 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

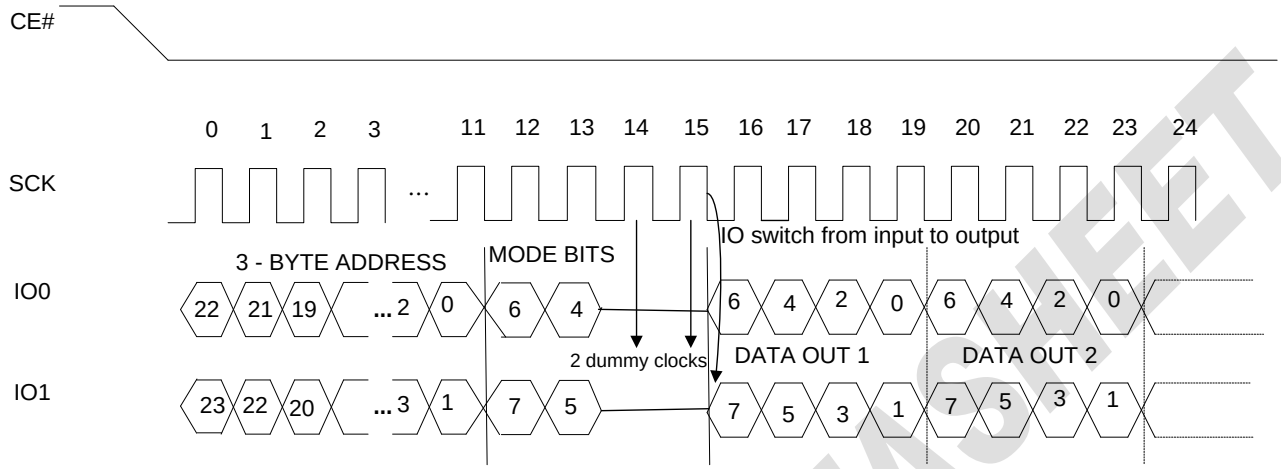
The device expects the next operation will be another FRDIO. It remains in this mode until it receives a Mode Reset (FFh) command. In subsequent FRDIO execution, the command code is not input, saving timing cycles as described in Figure 16. If a FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 4. Fast Read Dual I/O Sequence (with command decode cycles)



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

Figure 5. Fast Read Dual I/O Sequence (without command decode cycles)



*** If the mode bits=Ax (x don't care), it can execute the continuous read mode (without command)**
**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

DEVICE OPERATION (CONTINUED)

FRQIO COMMAND (FAST READ QUAD I/O) OPERATION

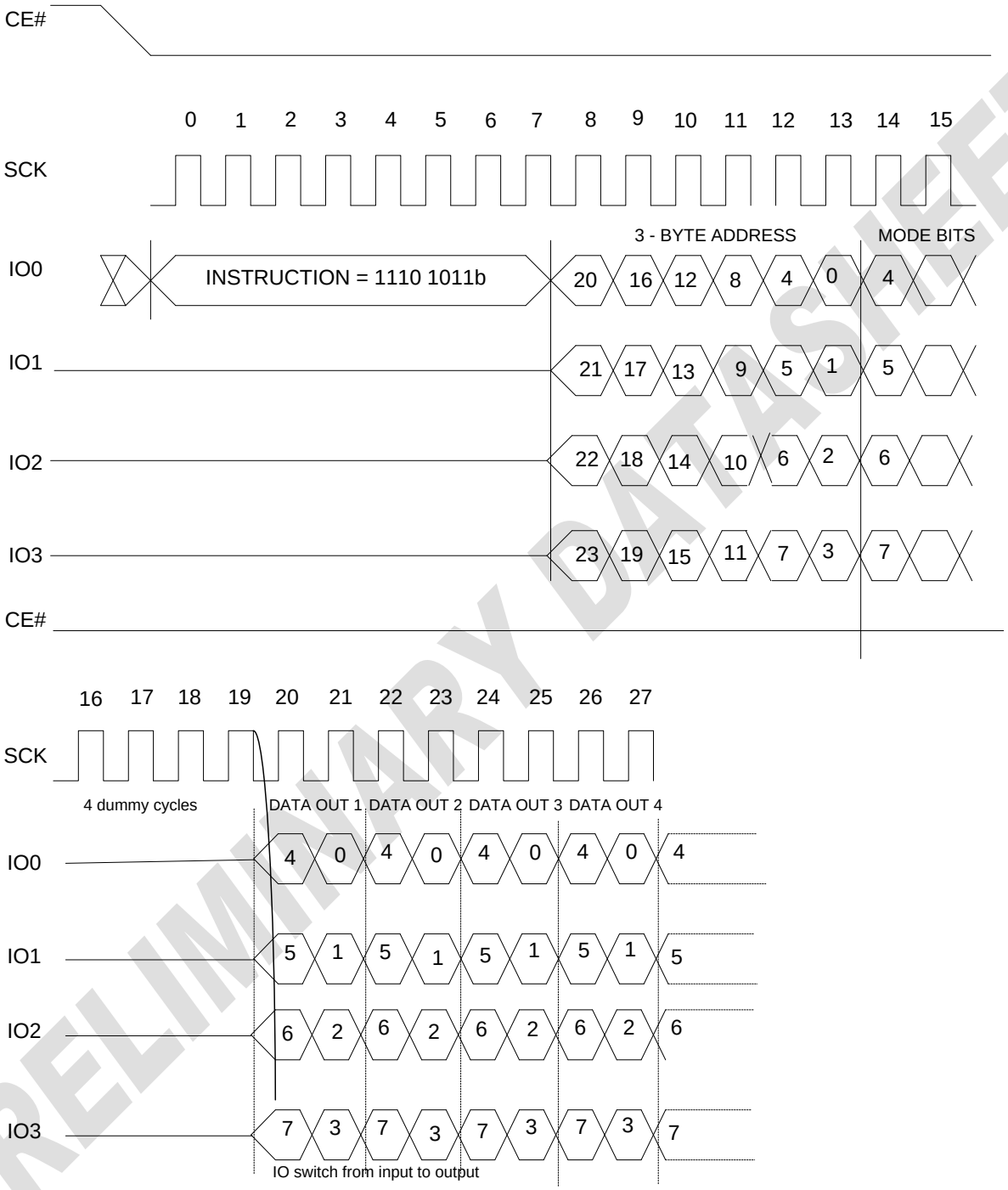
The FRQIO instruction allows the address bits to be input four bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRQIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO3, IO2, IO0 and IO1 lines, with each group of four bits latched-in during the rising edge of SCK. The address MSb is input on IO3, the next bit on IO2, the next bit on IO1, the next bit on IO0, and continue to shift in alternating on the four. The mode byte contains the value Ax, where x is a "don't care" value. After four dummy clocks, the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each group of four bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSb) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc. Figure 18 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQIO instruction. FRQIO instruction is terminated by driving CE# high (V_{IH}).

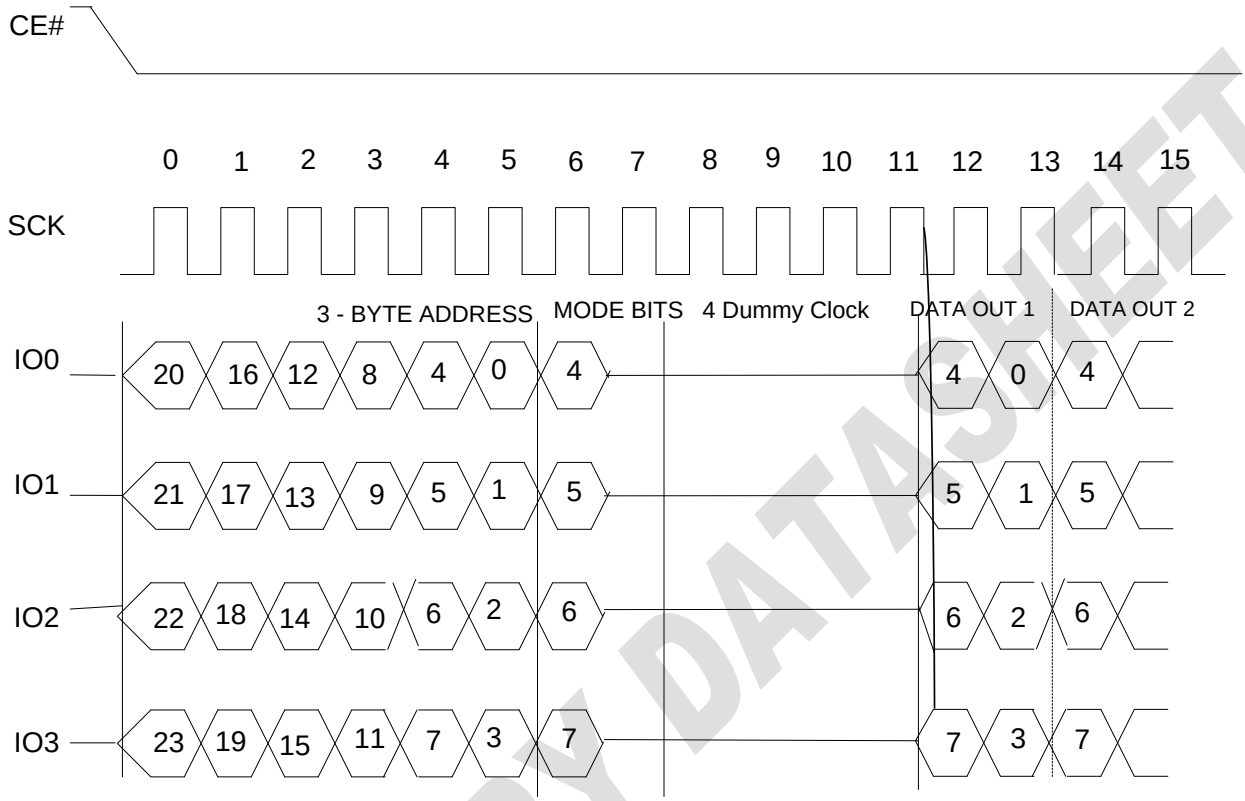
The device expects the next operation will be another FRQIO. It remains in this mode until it receives a Mode Reset (FFh) command. In subsequent FRDIO execution, the command code is not input, saving cycles as described in Figure 19. If a FRQIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 6. Fast Read Quad I/O Sequence (with command decode cycles)



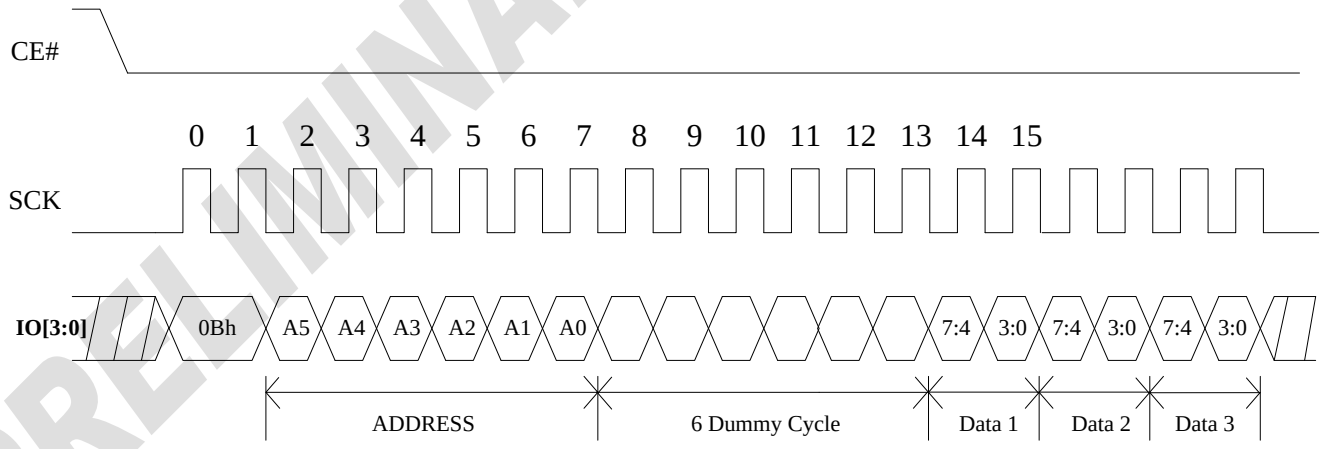
**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

Figure 7. Fast Read Quad I/O Sequence (without command decode cycles)



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

Figure 8. Fast Read Quad I/O Sequence (QPI Mode)



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

DEVICE OPERATION (CONTINUED)

PAGE_PROG COMMAND (PAGE PROGRAM) OPERATION

The Page Program (PAGE_PROG) instruction allows up to 256 bytes data to be programmed into memory in a single operation. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP2, BP1, BP0) bits. A PAGE_PROG instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of PAGE_PROG instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PAGE_PROG instruction code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PAGE_PROG instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. A byte cannot be reprogrammed without first erasing the whole sector or block.

Figure 9. Page Program Sequence

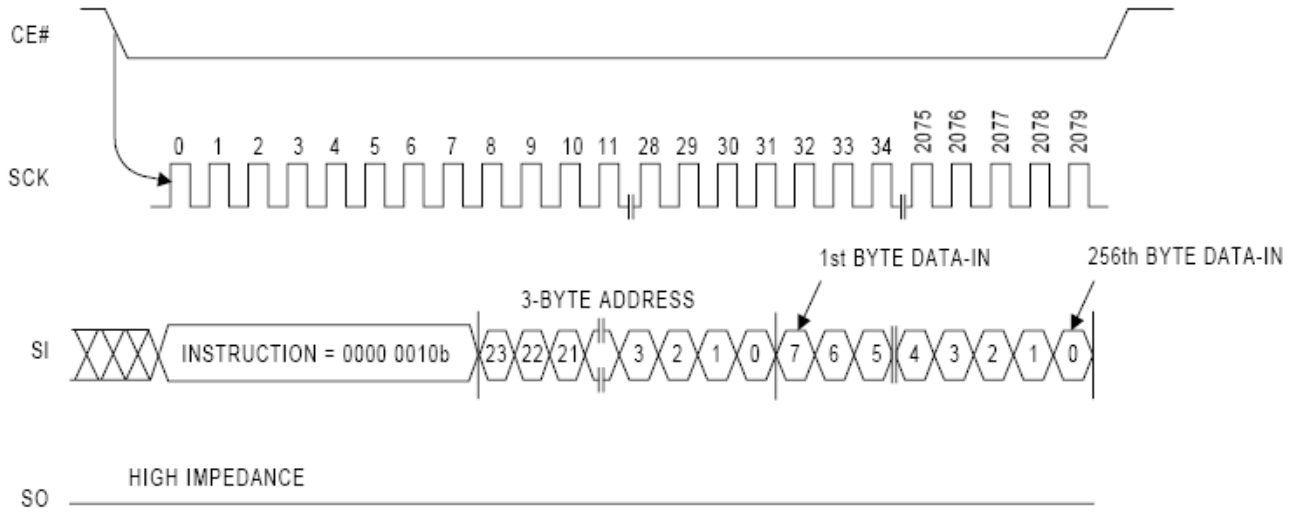
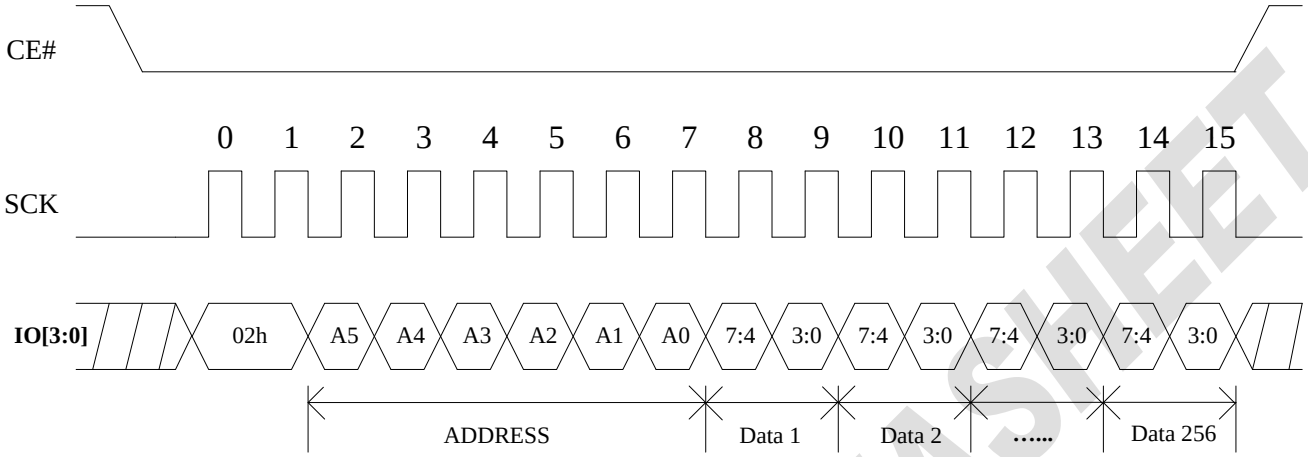


Figure 10. Page Program Sequence (QPI)



DEVICE OPERATION (CONTINUED)

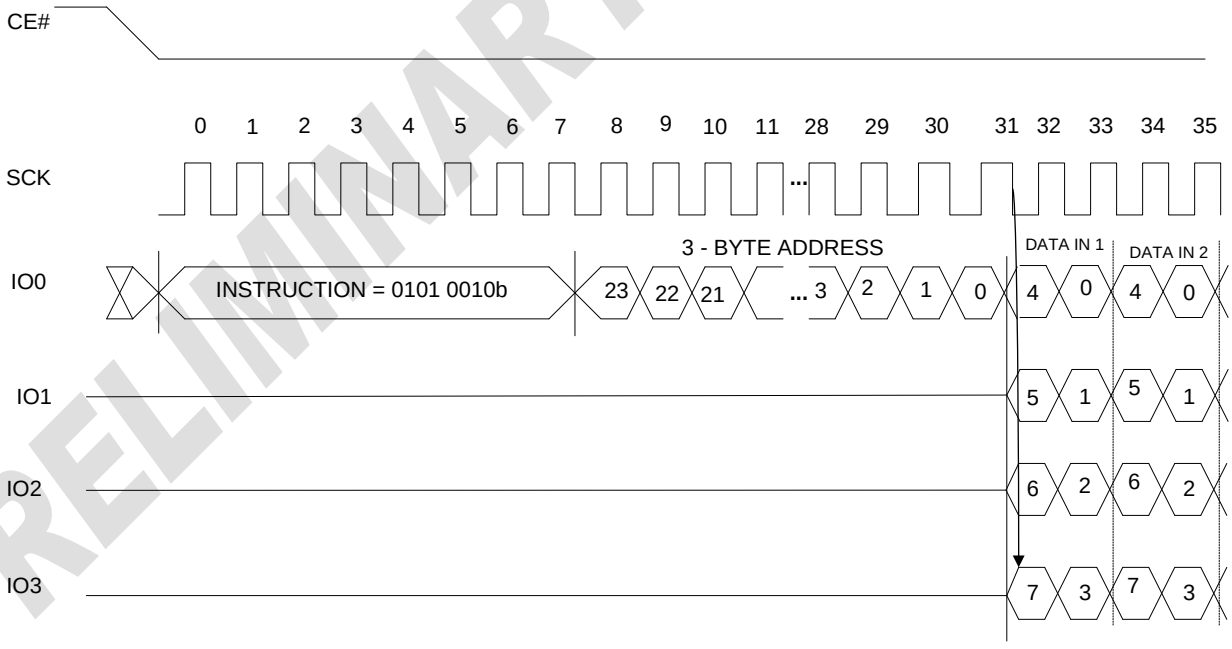
Quad Input Page Program operation

The Quad Input Page Program instruction allows up to 256 bytes data to be programmed into memory in a single operation with four pins (IO0, IO1, IO2 and IO3). The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A Quad Input Page Program instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of Quad Input Page Program instruction, the QE bit in the status register must be set to "1" and the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The Quad Input Page Program instruction code, three address bytes and program data (1 to 256 bytes) are input via the four pins (IO0, IO1, IO2 and IO3). Program operation will start immediately after the CE# is brought high, otherwise the Quad Input Page Program instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. A byte cannot be reprogrammed without first erasing the whole sector or block.



DEVICE OPERATION (CONTINUED)

ERASE OPERATION

The memory array of the IS25LQ064 is organized into uniform 4 KByte sectors or 32K/64 KByte uniform blocks (a block consists of sixteen adjacent sectors).

Before a byte can be reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to "1"). In order to erase the devices, there are three erase instructions available: Sector Erase (SECTOR_ER), Block Erase (BLOCK_ER) and Chip Erase (CHIP_ER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase or chip erase operation can be executed prior to any programming operation.

SECTOR_ER COMMAND (SECTOR ERASE) OPERATION

A SECTOR_ER instruction erases a 4 KByte sector Before the execution of a SECTOR_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is reset automatically after the completion of sector an erase operation.

A SECTOR_ER instruction is entered, after CE# is pulled low to select the device and stays low during the entire instruction sequence The SECTOR_ER instruction code, and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 22 for Sector Erase Sequence.

During an erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR instruction. If the WIP bit is "1", the erase operation is still in progress. If the WIP bit is "0", the erase operation has been completed.

BLOCK_ER COMMAND (BLOCK ERASE) OPERATION

A Block Erase (BLOCK_ER) instruction erases a 32/64 KByte block of the IS25LQ064. Before the execution of a BLOCK_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

The BLOCK_ER instruction code and three address bytes are input via SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BLOCK_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 23 for Block Erase Sequence.

CHIP_ER COMMAND (CHIP ERASE) OPERATION

A Chip Erase (CHIP_ER) instruction erases the entire memory array of a IS25LQ064. Before the execution of CHIP_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after completion of a chip erase operation.

The CHIP_ER instruction code is input via the SI. Erase operation will start immediately after CE# is pulled high, otherwise the CHIP_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 24 for Chip Erase Sequence.

DEVICE OPERATION (CONTINUED)

Figure 11. Sector Erase Sequence

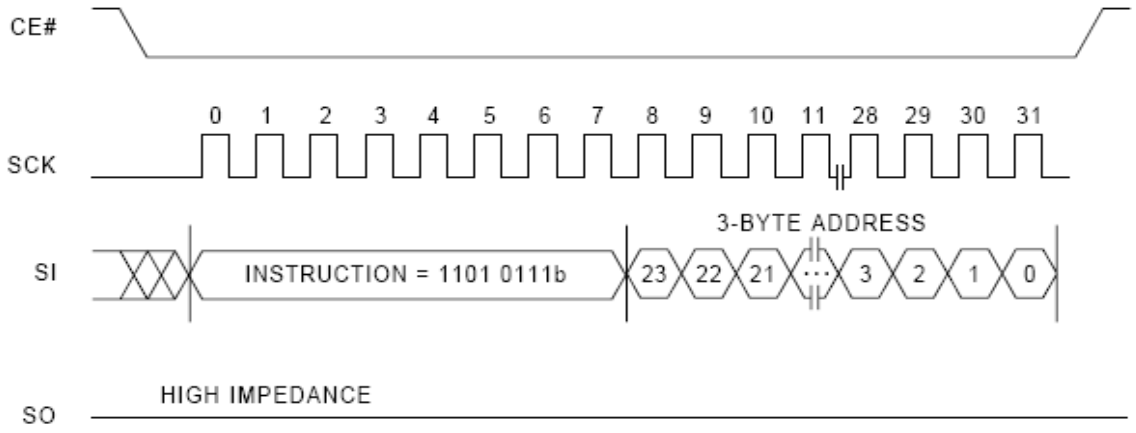


Figure 12. Sector Erase Sequence (QPI)

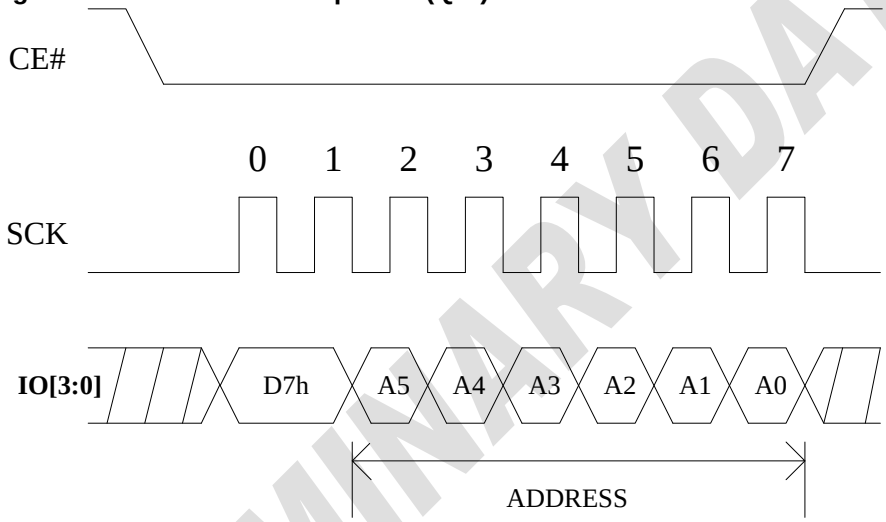


Figure 13. Block Erase Sequence

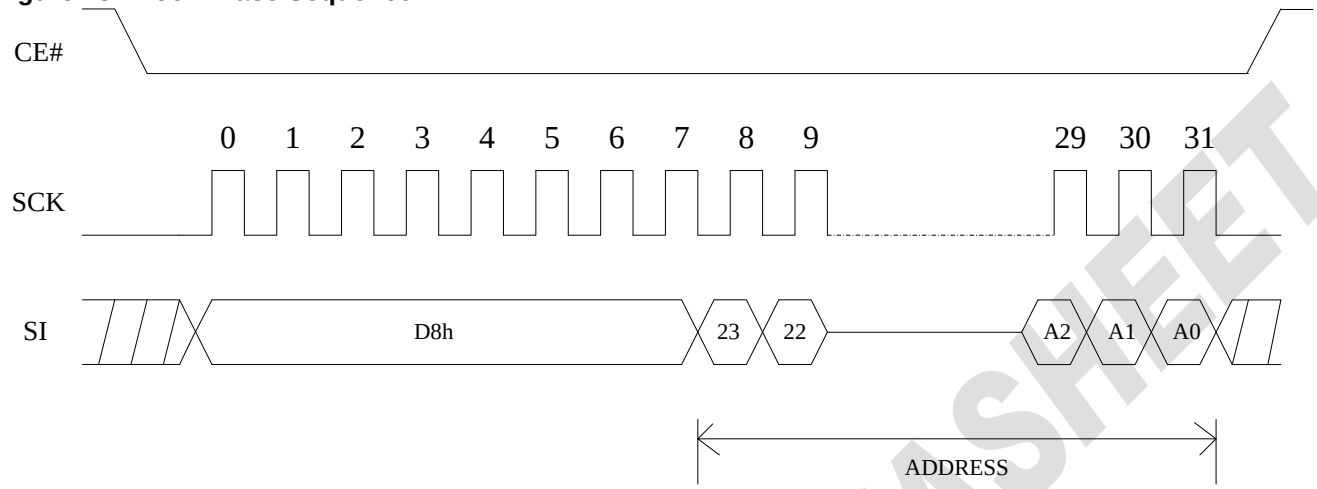


Figure 14. Block Erase Sequence (QPI)

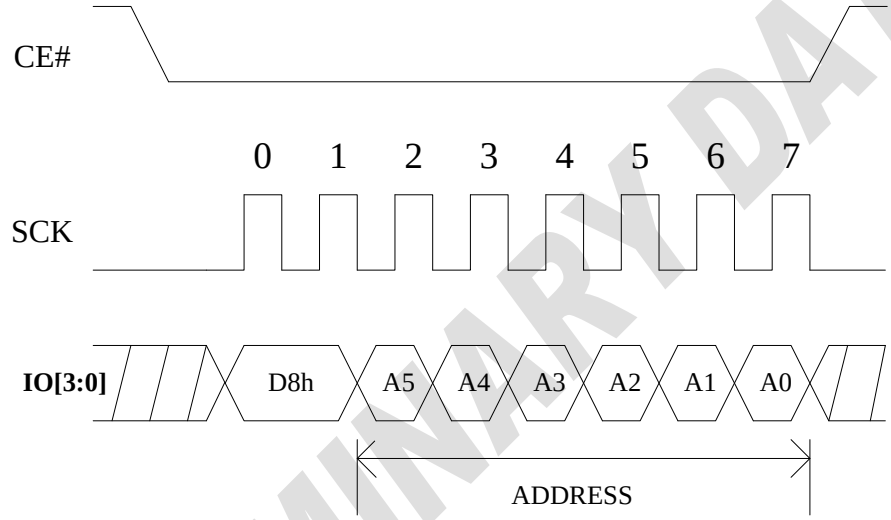


Figure 15. Block Erase(32K) Sequence

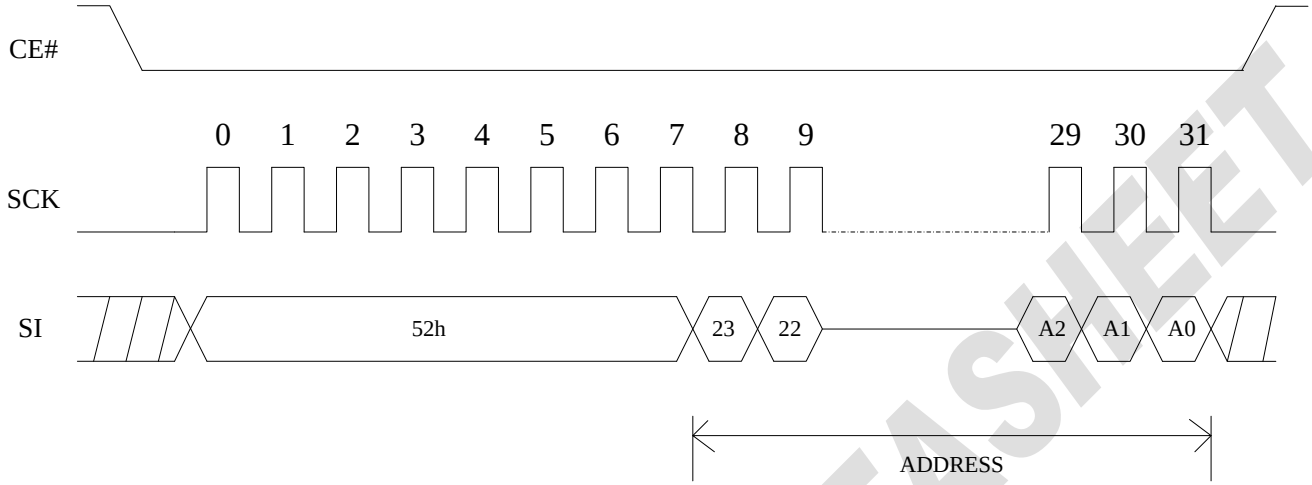


Figure 16. Block Erase(32K) Sequence (QPI)

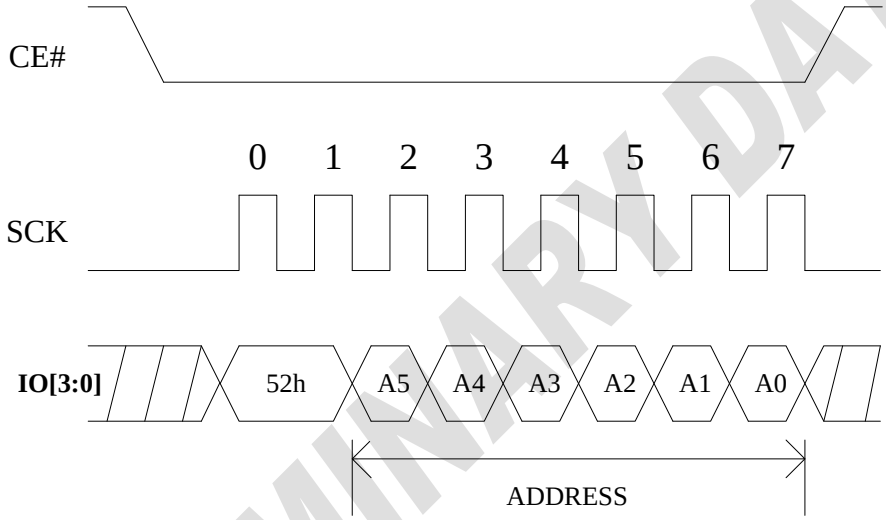


Figure 17. Chip Erase Sequence

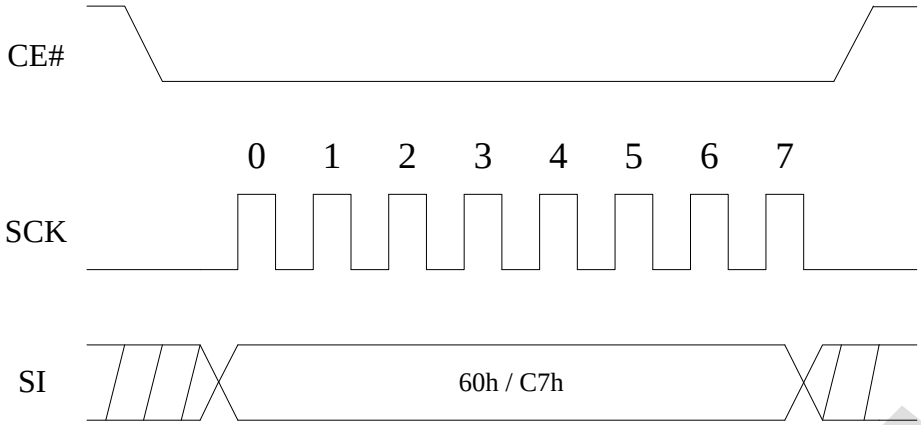
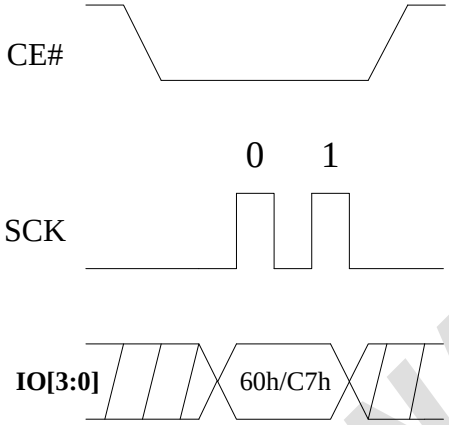


Figure 18. Chip Erase Sequence (QPI)



DEVICE OPERATION (CONTINUED)

WRITE ENABLE OPERATION

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit of the IS25LQ064 is reset to the write –protected state after power-up. The WEL bit must be write enabled before any write operation, including sector, block erase, chip erase, page program, write status register, and write configuration register operations. The WEL bit will be reset to the write-protect state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

Figure 19. Write Enable Sequence

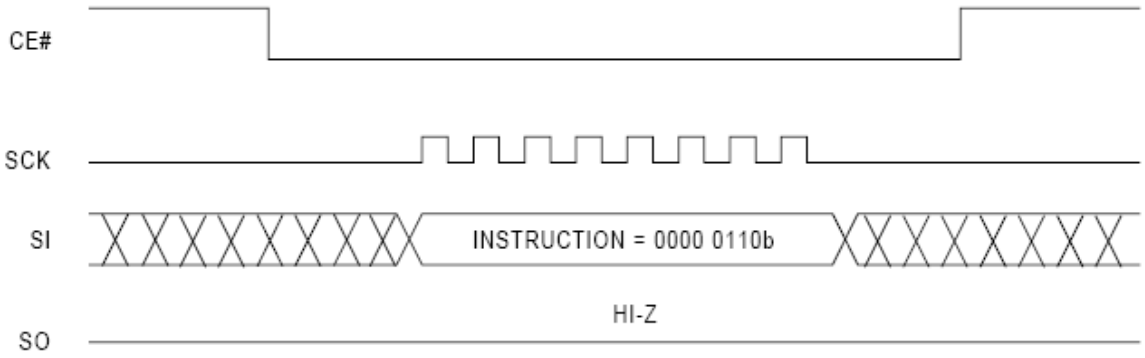
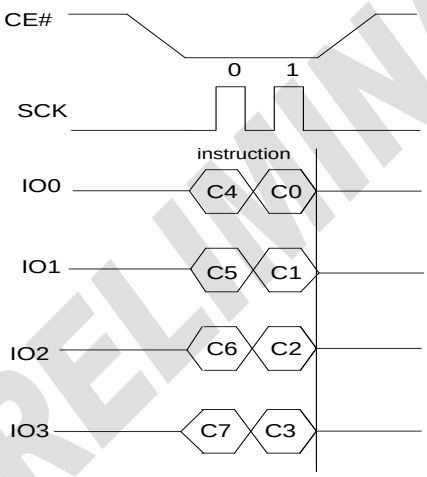


Figure 20. WRITE ENABLE OPERATION (QPI)



WRDI COMMAND (WRITE DISABLE) OPERATION

The Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction, since the WEL bit is automatically reset.

Figure 21. Write Disable Sequence

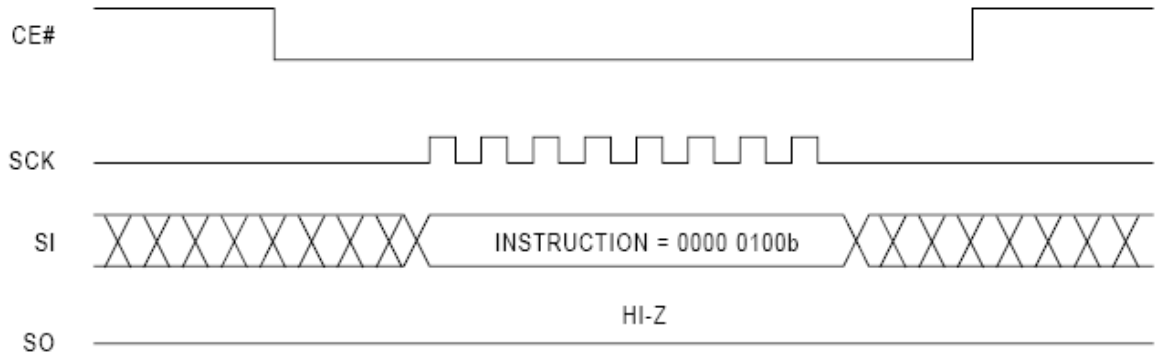
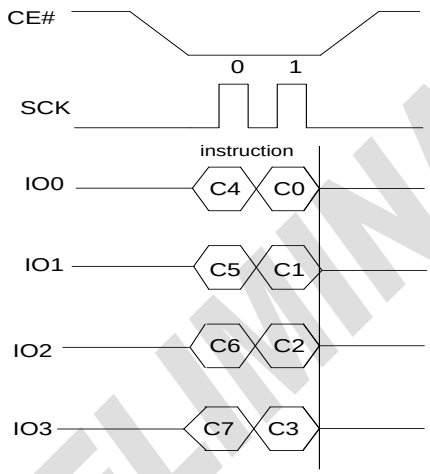


Figure 22. WRITE DISABLE OPERATION (QPI)



DEVICE OPERATION (CONTINUED)

RDSR COMMAND (READ STATUS REGISTER) OPERATION

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write status register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of Status Register.

Figure 23. Read Status Register Sequence

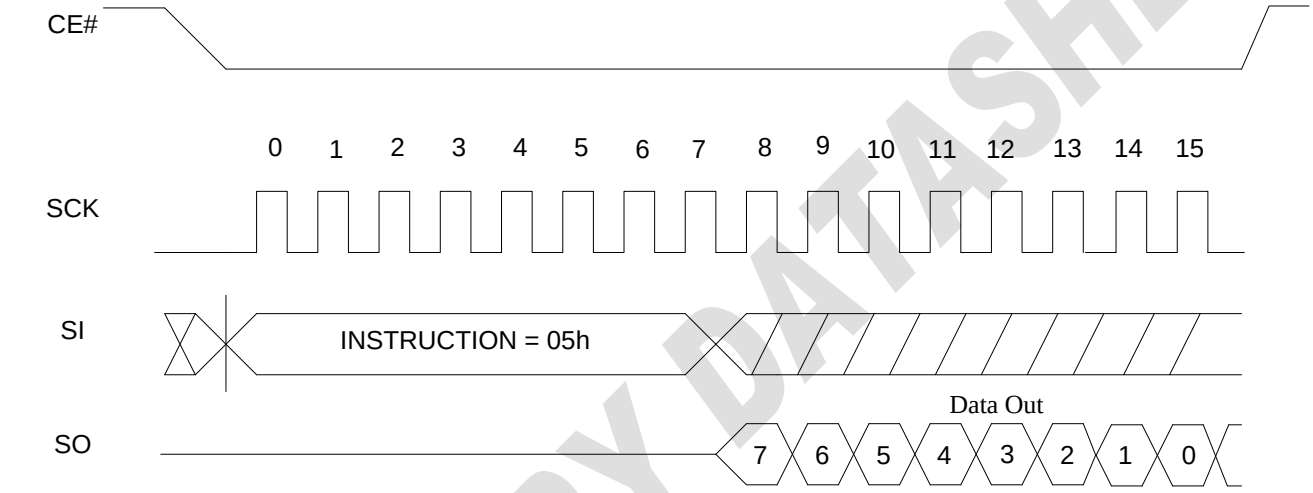
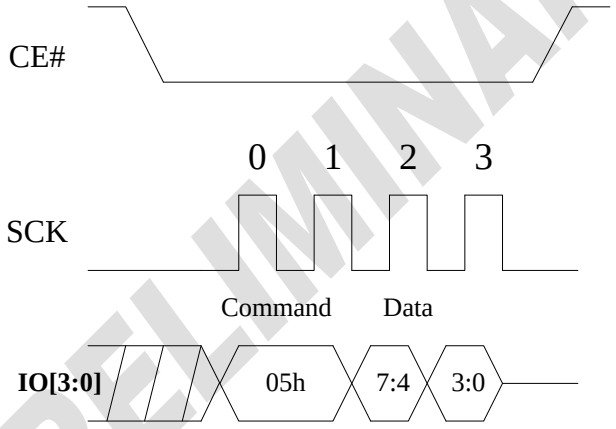


Figure 24. RDSR COMMAND (READ STATUS REGISTER) OPERATION (QPI)



WRSR COMMAND (WRITE STATUS REGISTER) OPERATION

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and status register write protection features by writing “0”s or “1”s into the non-volatile BP3, BP2, BP1, BP0, QE and SRWD bits.

Figure 25. Write Status Register Sequence

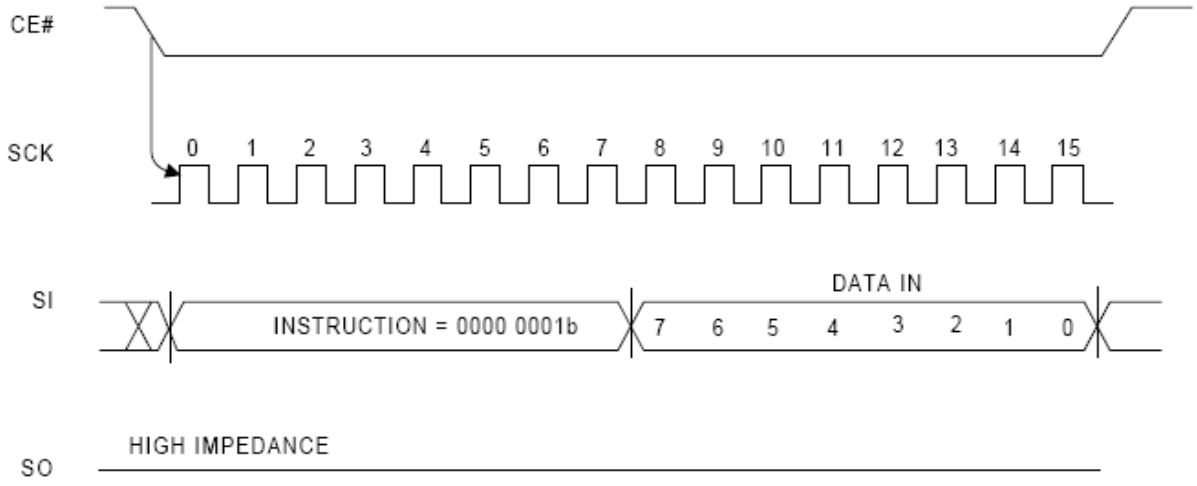
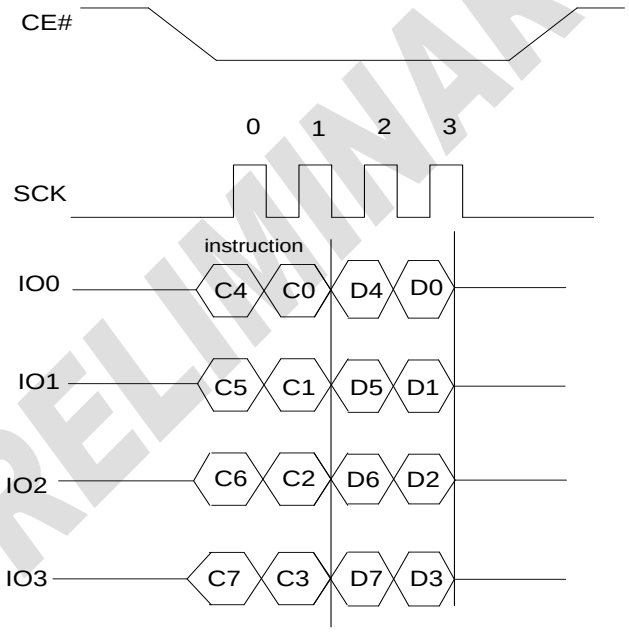


Figure 26. WRSR COMMAND (WRITE STATUS REGISTER) OPERATION (QPI)



DEVICE OPERATION (CONTINUED)

RDFR COMMAND (READ FUNCTION REGISTER) OPERATION

The Read Function Register (RDFR) instruction provides access to the Erase/Program suspend register. During the execution of a program, erase or write status register suspend, which can be used to check the suspend status.

Figure 27. Read Function Register Sequence

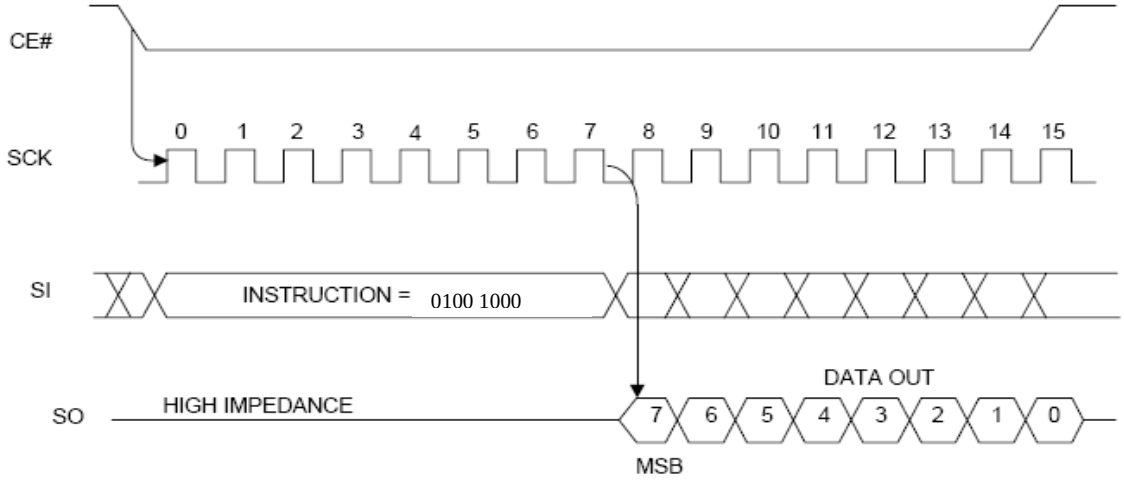
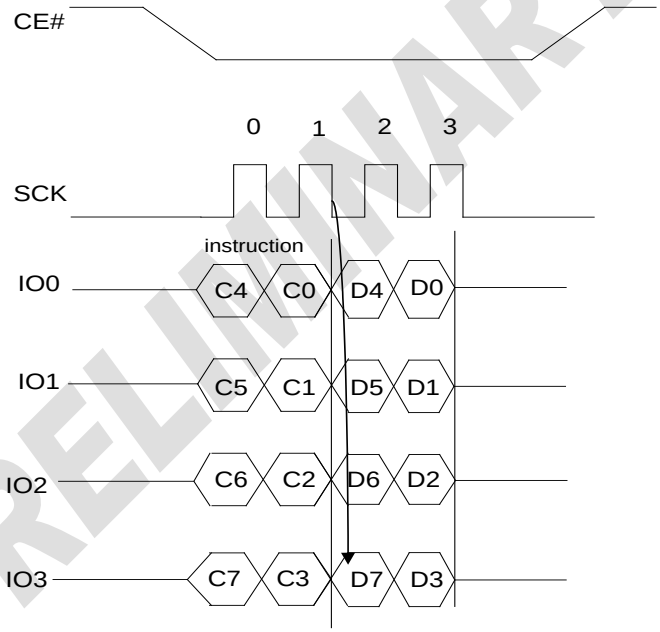


Figure 28. RDFR COMMAND (READ Function REGISTER) OPERATION (QPI)



DEVICE OPERATION (CONTINUED)

WRFR COMMAND (WRITE Function REGISTER) OPERATION

The Write Function Register (WRFR) instruction allows the user to lock the information row by bit 0. (IR lock)

Figure 29. Write Function Register Sequence

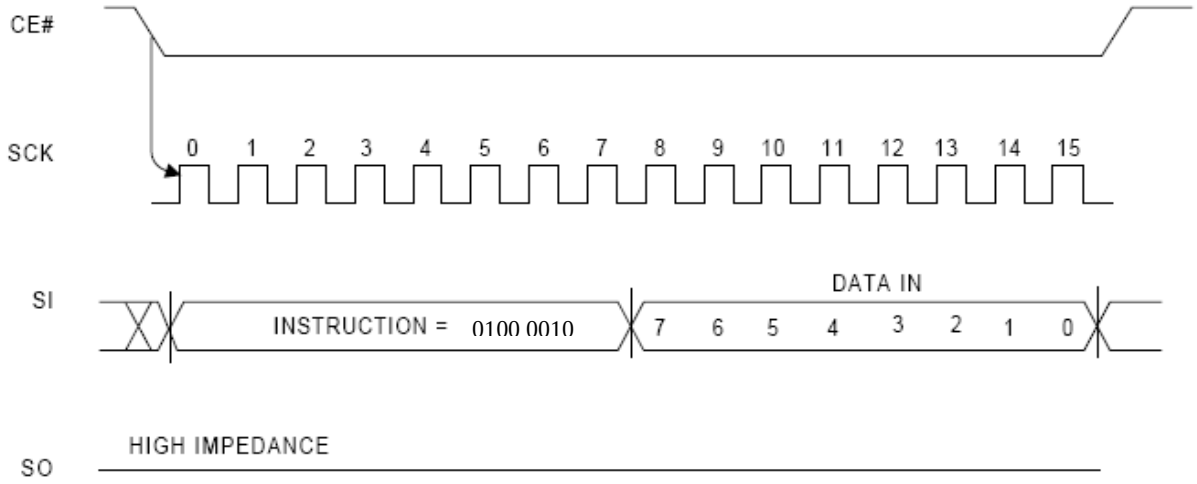
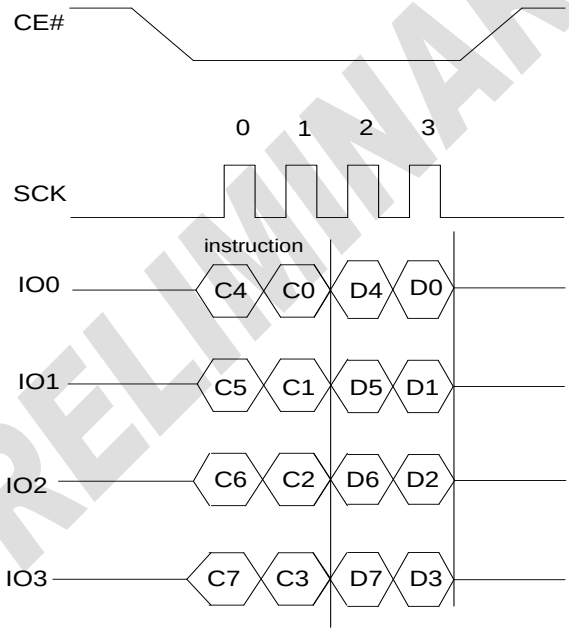


Figure 30. WRFR COMMAND (WRITE Function REGISTER) OPERATION (QPI)



DEVICE OPERATION (CONTINUED)

Enter Quad Peripheral Interface (QPI) mode OPERATION

The Enter Quad I/O (ENQIO) instruction, 35H, enables the flash device for QPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or a “Exit Quad I/O instruction” instruction.

Figure 31. Enter Quad Peripheral Interface OPERATION (QPI)

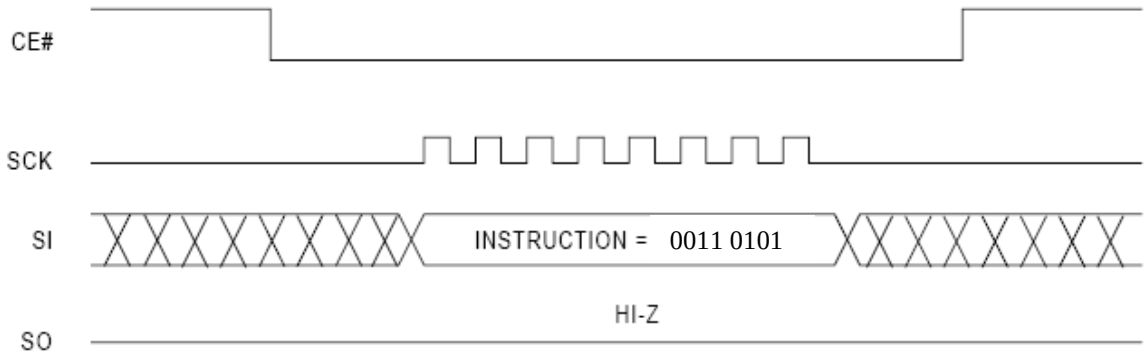
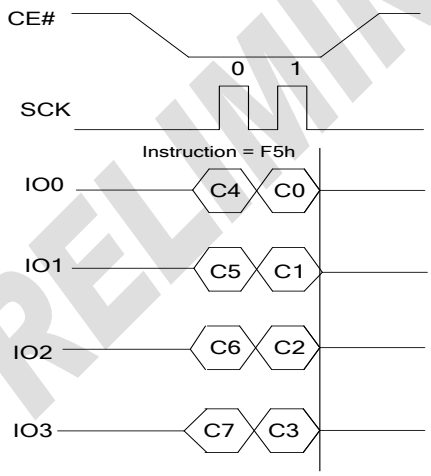


Figure 32. Exit Quad Peripheral Interface (QPI) mode OPERATION

The Exit Quad I/O instruction, F5H, resets the device to 1-bit SPI protocol operation. To execute a Exit Quad I/O operation, the host drives CE# low, sends the Exit Quad I/O command cycle (F5H) then, drives CE# high. The device just accepts SQI (2 clocks) command cycles.



DEVICE OPERATION (CONTINUED)

Program/Erase Suspend Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations.
To enter the suspend/ resume mode: issuing B0h for suspend; 30h for resume (SPI/QPI all acceptable)
Read Function register bit2 (PSUS) and bit3 (ESUS) to check suspend ready information.
Suspend to suspend ready timing: 20us.
Resume to another suspend timing: 1ms.

Program/Erase Suspend During Sector-Erase or Block-Erase

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted. (03h, 0Bh, BBh, EBh, 05h, ABh, 30h, 9Fh, ABh, 90h, 4Bh, 00h, 66h, 99h, AFh, C0h)
To execute a Program/Erase Suspend operation, the host drives CE# low, sends the Program/Erase Suspend command cycle (B0H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. The Function register indicates that the erase has been suspended by changing the ESUS bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit in the Status register or wait TWS. When ESUS bit is issued, the Write Enable Latch (WEL) bit will be reset.

Program/Erase Suspend During Page Programming

Program suspend allows the interruption of all program operations.
After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (03h, 0Bh, BBh, EBh, 05h, ABh, 30h, 9Fh, ABh, 90h, 4Bh, 00h, 66h, 99h, AFh, C0h)
To execute a Program/Erase Suspend operation, the host drives CE# low, sends the Program/Erase Suspend command cycle (B0H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. The Function register indicates that the programming has been suspended by changing the PSUS bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit in the Status register or wait TWS.

Program/Erase Resume

Program/Erase Resume restarts a Program/Erase command that was suspended, and changes the suspend status bit in the (ESUS or PSUS) back to '0'. To execute a Program/Erase Resume operation, the host drives CE# low, sends the Program/Erase Resume command cycle (30H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. To determine if the internal, self-timed Write operation completed, poll the WIP bit in the Status register, or wait the specified time TSE, TBE or TPP for Sector- Erase, Block-Erase, or Page-Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times TSE, TBE or TPP.

Deep Power Down

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (enter into Power-Down mode), the standby current is reduced from Isb1 to Isb2). During the Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. The instruction is initiated by driving the CE# pin low and shifting the instruction code “B9h” as show in the figure 29. The CE# pin must be driven high after the instruction has been latched. If this is not done the Power-Down will not be executed. After CE# pin driven high, the power-down state will entered within the time duration of t_{DPD}. While in the power-down state only the Release from Power-down / RDID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. It can support in SPI and QPI mode.

Figure 32. Enter Deep Power Down Mode Operation. (SPI)

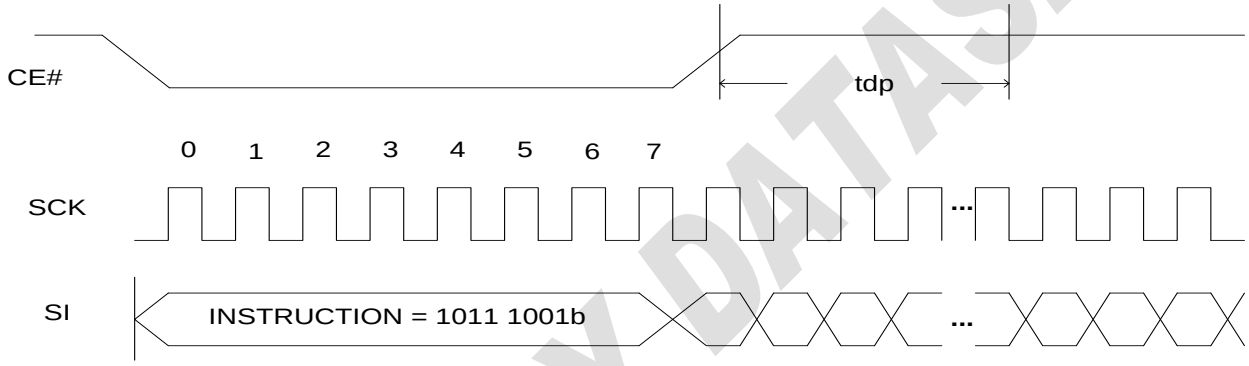


Figure 33. Deep Power Down Sequence (QPI)

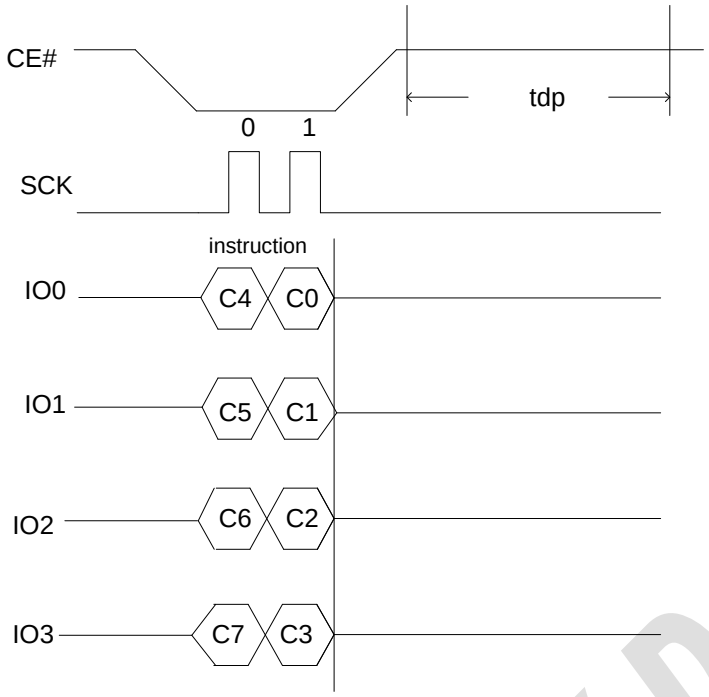


Figure 30. Release Power Down Sequence (SPI)

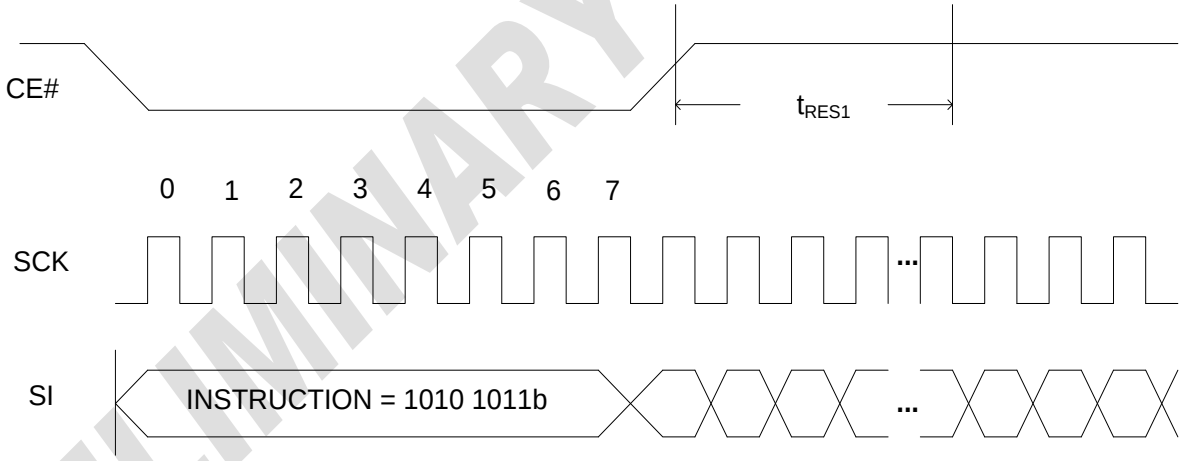
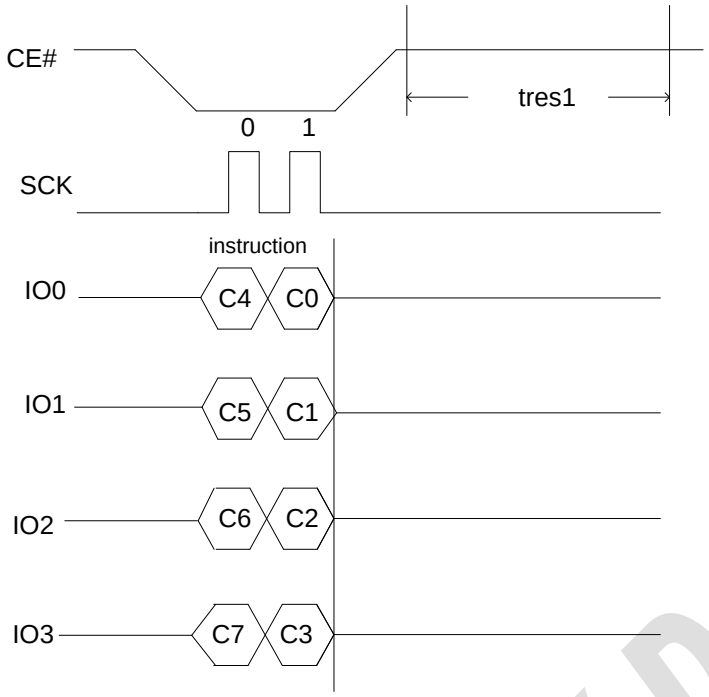


Figure 31. Release Power Down Sequence (QPI)



DEVICE OPERATION (CONTINUED)

SRP Command (Set Read Parameters)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around"

This device supports Burst Read in both SPI and QPI mode. To set the Burst length, following command operation is required issuing command: "C0h" in the first Byte (8-clocks), following burst length data defining wrap around enable with "0h" and disable with"1h".
The wrap around unit is defined within the 256Byte page, with random initial address. It's defined as "wrap-around mode disable" for the default state of the device. To exit wrap around, it is required to issue another "C0" command to set bit3 = 0. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another "C0" command to set bit0 and bit1.(Detail information in Table 8.Burst Length Data).QPI "0Bh" "EBh" and SPI (EBh, 03h, 0Bh, BBh) support wrap around feature after wrap around enable. Burst read is supported in both SPI and QPI mode. The device id default without Burst read.

Figure 32. Set Read Parameters Operation.

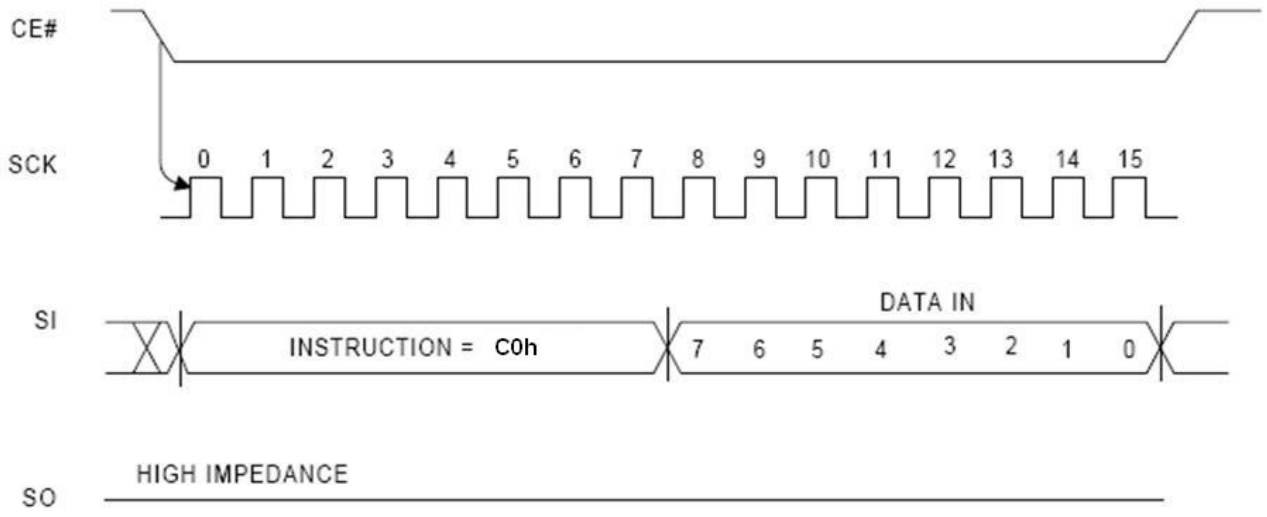
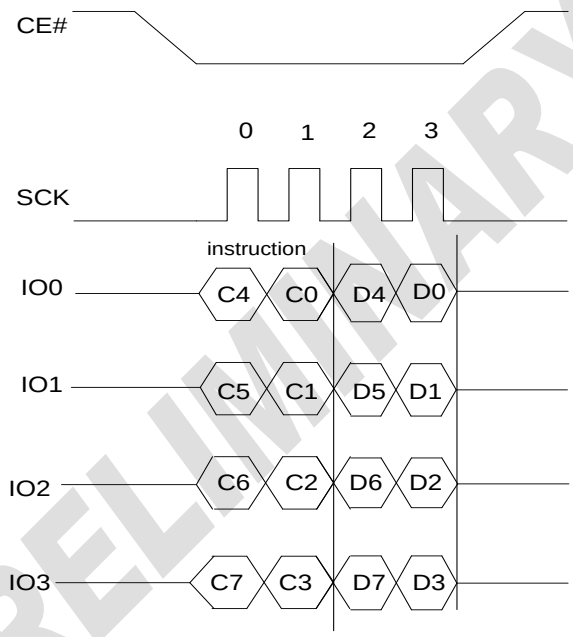


Figure 33. Set Read Parameters Operation. (QPI)



DEVICE OPERATION (CONTINUED)

RDID COMMAND (READ PRODUCT IDENTIFICATION)/ Release Power-down OPERATION

The Release from Power-down /read Device ID instruction is a multi-purpose instruction. It can support bot SPI and QPI mode.The Read Product Identification (RDID) instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not same as RDID or JEDEC ID instruction. It's not recommended to use for new design. For new design, please use RDID or JEDEC ID instruction.
The RDES instruction code is followed by three dummy bytes, each bit being latched-in on SI during the rising edge of SCK. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDES instruction is ended by CE# goes high. The Device ID1 outputs repeatedly if continuously send the additional clock cycles on SCK while CE# is at low.

To release the device from the power-down state Mode, the instruction is issued by driving the CE# pin low, shifting the instruction code "ABh" and driving CE# high as shown in figure 3.
Release from power-down will take the time duration of t_{RES1} before the device will resume normal operation and other instructions are accepted. The CE# pin must remain high during the t_{RES1} time duration. If the Release from Power-down / RDID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effects on the current cycle

Table 12. Product Identification

Product Identification		Data
Manufacturer ID	First Byte	9Dh
	Second Byte	7Fh
Device ID:	Device ID1	Device ID2
IS25LQ0064	16h	47h

Figure 34. Read Product Identification Sequence

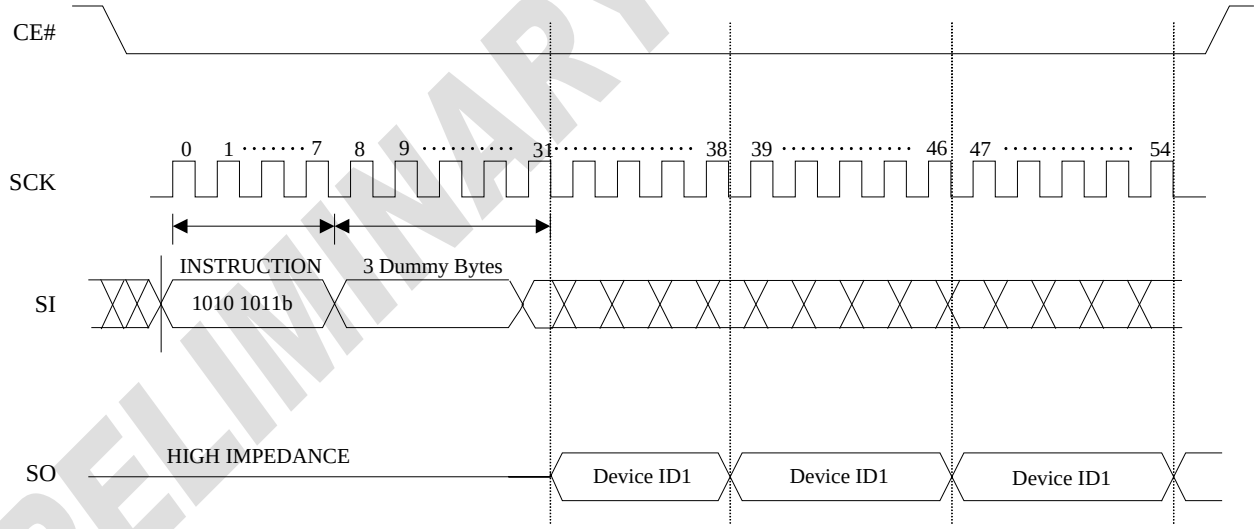
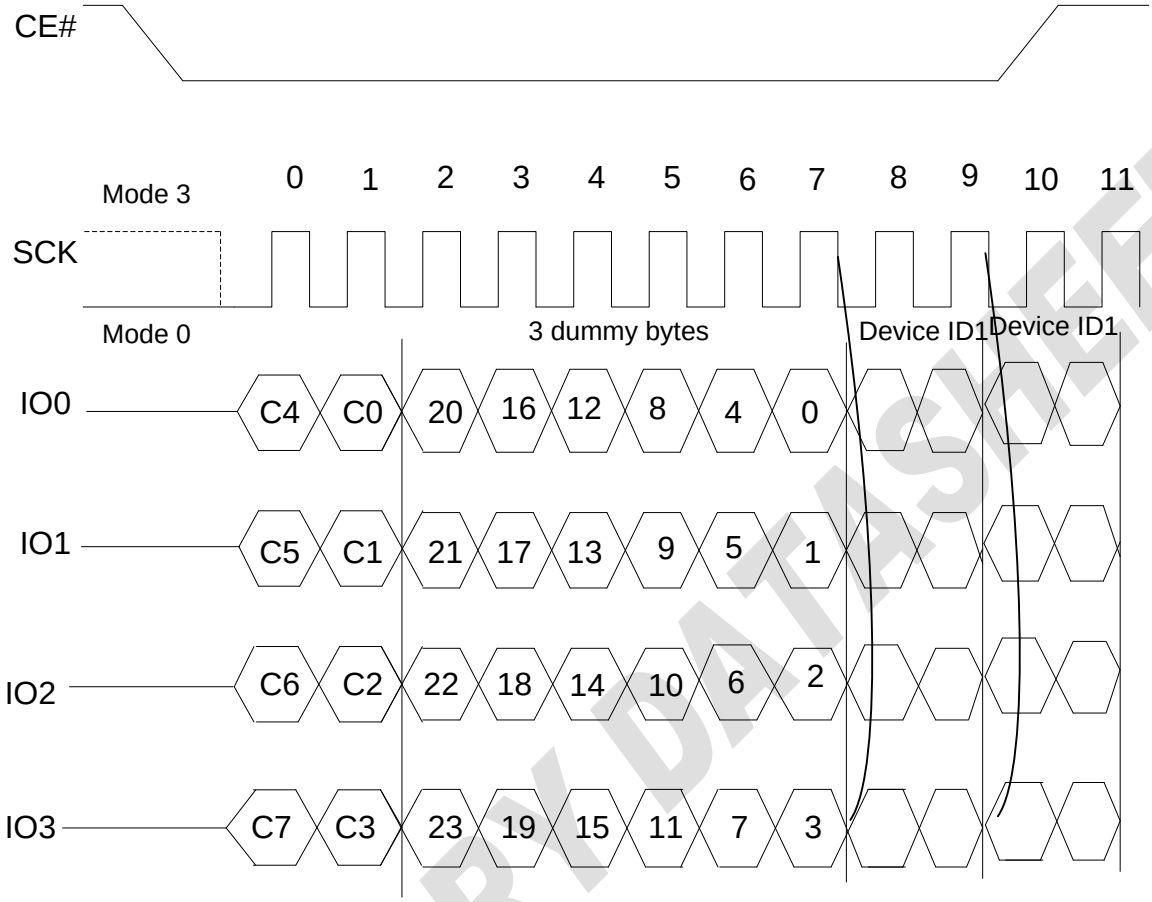


Figure 35. Read Product Identification Sequence (QPI)



DEVICE OPERATION (CONTINUED)

JEDEC ID READ COMMAND (READ PRODUCT IDENTIFICATION BY JEDEC ID) OPERATION

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of devices. Refer to Table 12 Product Identification for pFlash Manufacturer ID and Device ID. After the JEDEC ID READ command is input, the First Manufacturer ID (9Dh) is shifted out on SO with the MSB first, followed by the first Device ID (16h) and the Device ID2 (48h, in the case of the IS25LQ0064), each bit shifted out during the falling edge of SCK. If CE# stays low after the last bit of the Device ID is shifted out, the Manufacturer ID and Device ID will loop until CE# is pulled high.

Figure 36. Read Product Identification by JEDEC ID READ Sequence

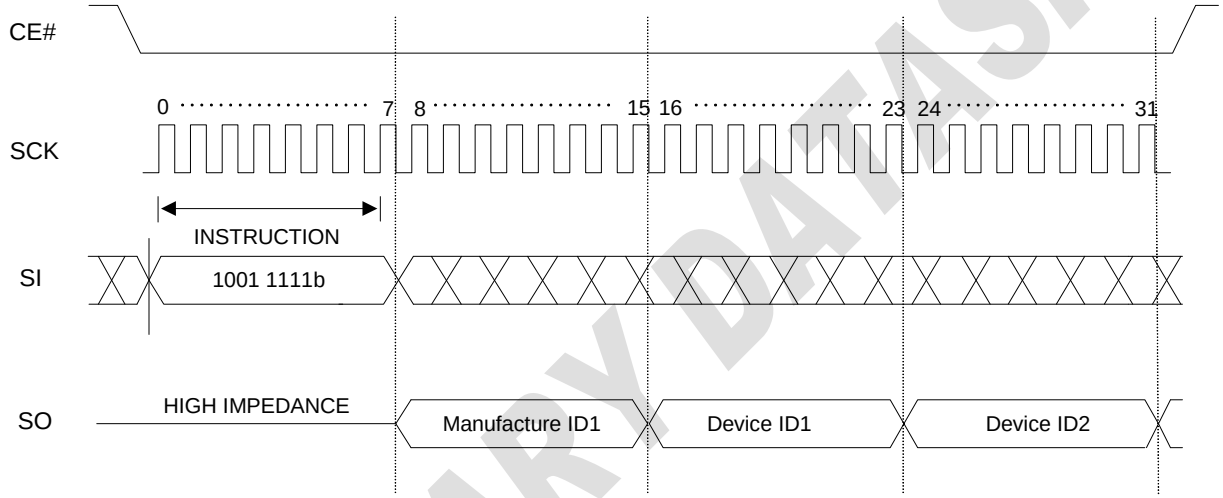
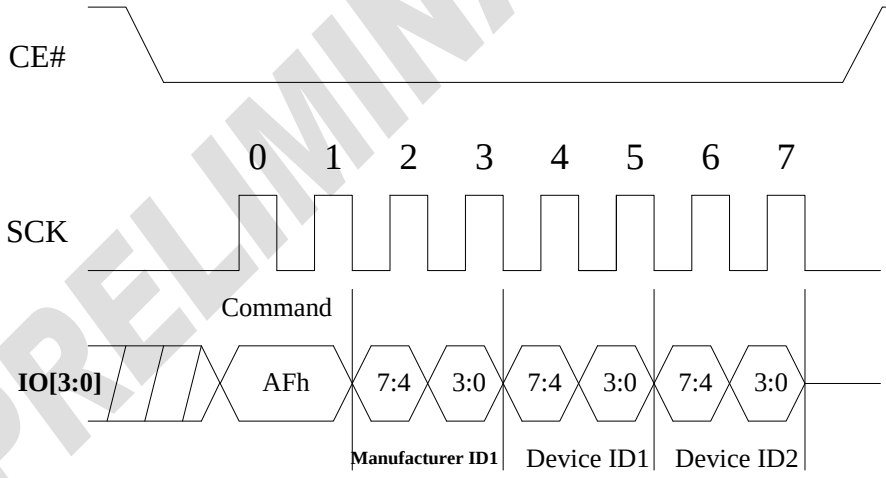


Figure 37. RDIDQ COMMAND (Read ID in QPI Mode) OPERATION

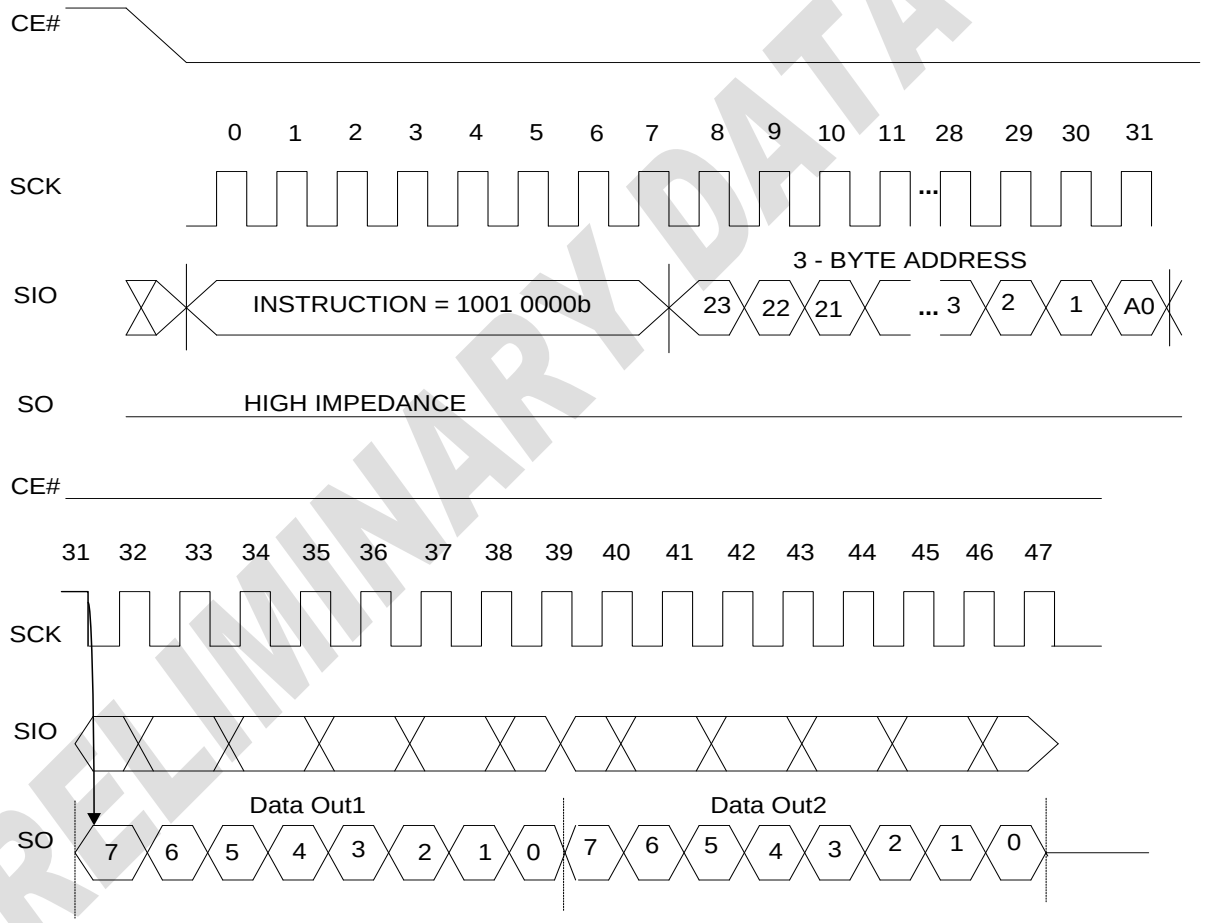


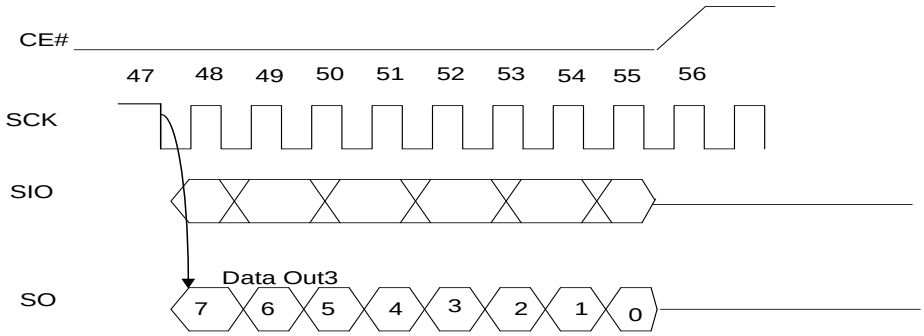
DEVICE OPERATION (CONTINUED)

RDMDID COMMAND (READ DEVICE MANUFACTURER AND DEVICE ID) OPERATION

The Read Product Identification (RDID) instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 12 Product Identification for pFLASH™ manufacturer ID and device ID. The RDID instruction code is followed by two dummy bytes and one byte address (A7~A0), each bit being latched-in on SI during the rising edge of SCK. If one byte address is initially set to A0 = 0, then the first manufacturer ID (9Dh) is shifted out on SO with the MSB first, the device ID1 and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of SCK. If one byte address is initially set to A0 = 1, then device ID1 will be read first, then followed by the first manufacture ID (9Dh) and then second manufacture ID (7Fh). The manufacture and device ID can be read continuously, alternating from one to the others. The instruction is completed by driving CE# high.

Figure 38. Read Product Identification by RDMDID READ Sequence





Note :
(1) ADDRESS A0 = 0, will output the 1st manufacture ID (9Dh) first -> device ID1 -> 2nd manufacture ID (7Fh)
ADDRESS A0 = 1, will output the device ID1 -> 1st manufacture ID (9D) -> 2nd manufacture ID (7Fh)

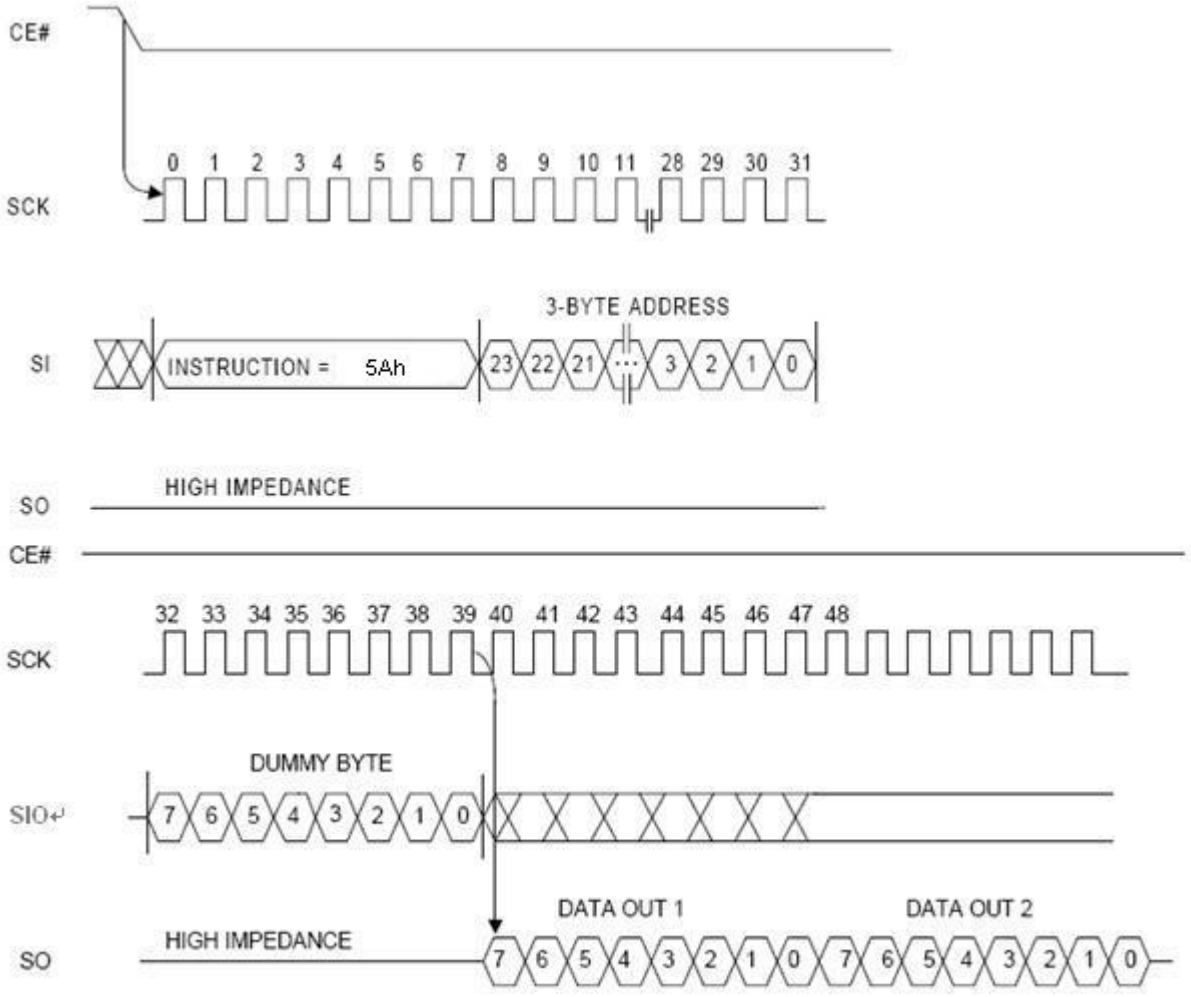
DEVICE OPERATION (CONTINUED)

RDSFDP COMMAND (Read SFDP) OPERATION

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as FAST_READ: CS# goes low' send RDSFDP instruction (5Ah)' send 3 address bytes on SI pin' send 1 dummy byte on SI pin' read SFDP code on SO' to end RDSFDP operation can use CS# to high at any time during data out.

Figure 39. RDSFDP COMMAND (Read SFDP) OPERATION



No Operation (NOP)

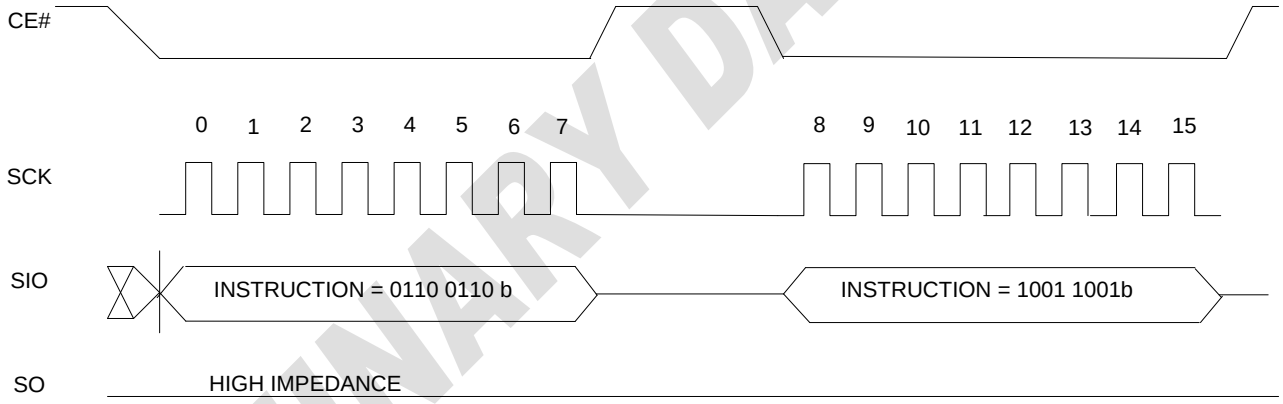
The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command. It can use in the SPI and QPI mode.
To execute a NOP, the host drives CE# low, sends the NOP command cycle (00H), then drives CE# high.

DEVICE OPERATION (CONTINUED)

Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Reset operation is used as a system (software) reset that puts the device in normal operating mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).
The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.
Execute the CE# pin low → sends the Reset-Enable command (66H), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99H), and drives CE# high.
A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

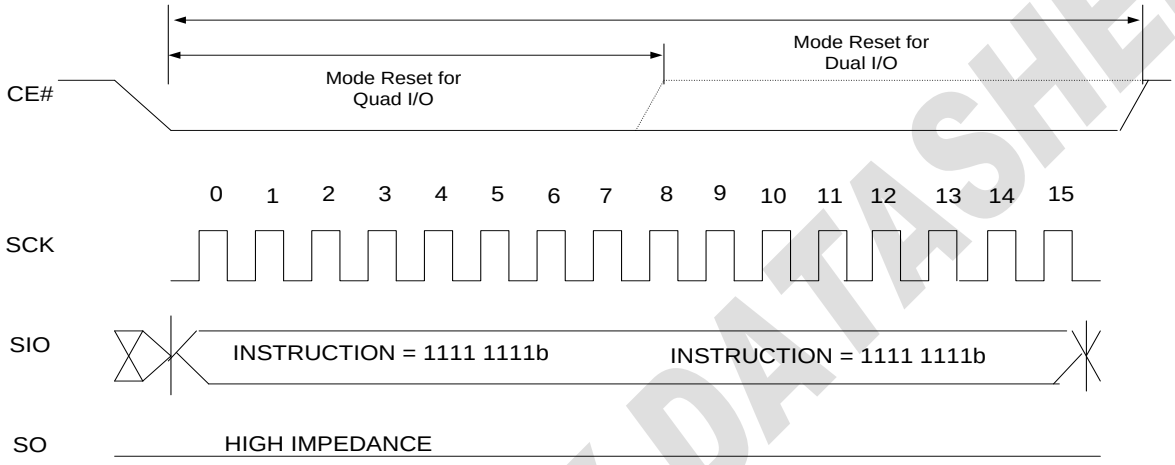
Figure 41. Software Reset COMMAND (RSTEN + RST) OPERATION



MR COMMAND (MODE RESET) OPERATION

The Mode Reset command is used to conclude subsequent FRDIO and FRQIO operations. It resets the Mode bits to a value that is not Ax. It should be executed after an FRDIO or FRQIO operation, and is recommended also as the first command after a system reset. The timing sequence is different depending whether the MR command is used after an FRDIO or FRQIO, as shown in Figure 20.

Figure 42, Mode Reset Command



DEVICE OPERATION (CONTINUED)

Security information Row

The first 16bytes in IRL0 is determined by pFlash. If customer have special requirement, please contact with pFlash in advance.

Information Row Address

IRL0 : A23-16 = 00h , A15-8 = 00h , A7-0 = Byte address
IRL1 : A23-16 = 00h , A15-8 = 10h , A7-0 = Byte address
IRL2 : A23-16 = 00h , A15-8 = 20h , A7-0 = Byte address
IRL3 : A23-16 = 00h , A15-8 = 30h , A7-0 = Byte address

To lock the OTP memory:

Bit 7~4 of the Function Register is used to permanently lock the OTP memory array.
□When Function Register bit IRLx = '0', the 256 bytes of the OTP memory array can be programmed.
□When Function Register bit IRLx = '1', the 256 bytes of the OTP memory array are read-only and cannot be programmed anymore.

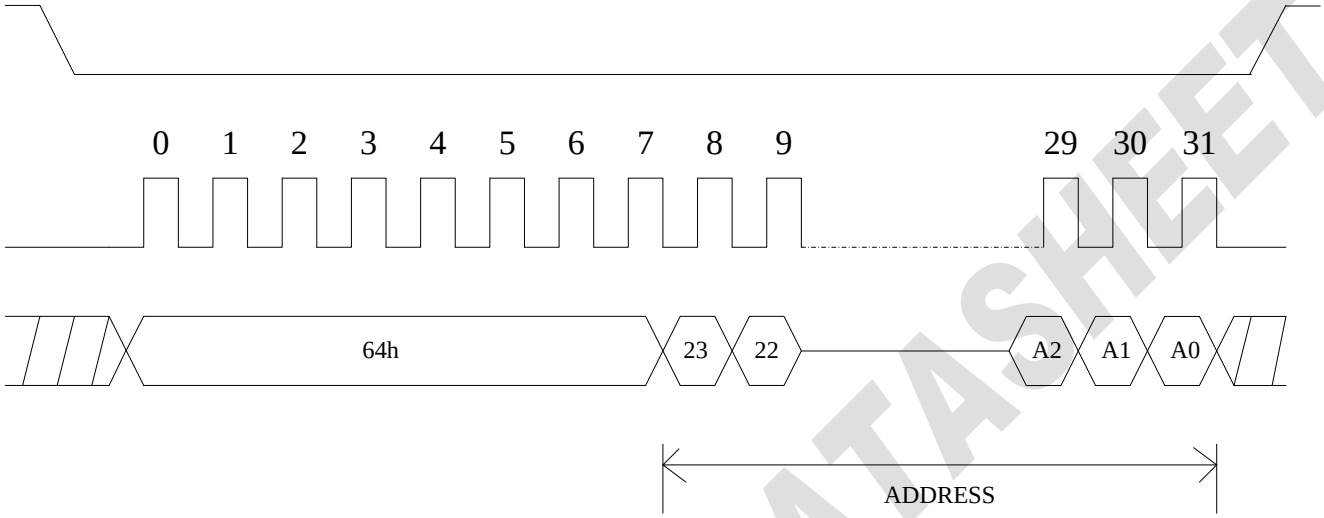
Once a bit of the OTP memory has been programmed to '1', it can no longer be set to '0'.
Therefore, as soon as Function Register is set to '1', the 256 bytes of the OTP memory array become read-only in a permanent way.
Any program OTP (POTP) instruction issued while an erase, program or write cycle is in progress is rejected without having any effect on the cycle that is in progress

IRER COMMAND (Information Row Erase) OPERATION

Information Row Erase instruction erases the Information Row x (x : 0~3) array , the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is reset automatically after the completion of sector an erase operation.

A ILER instruction is entered, after CE# is pulled low to select the device and stays low during the entire instruction sequence The IRER instruction code, and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 22 for IRER Sequence.

Figure 43. IPER COMMAND (Information Row Erase) OPERATION



IRP COMMAND (Information Row Program) OPERATION

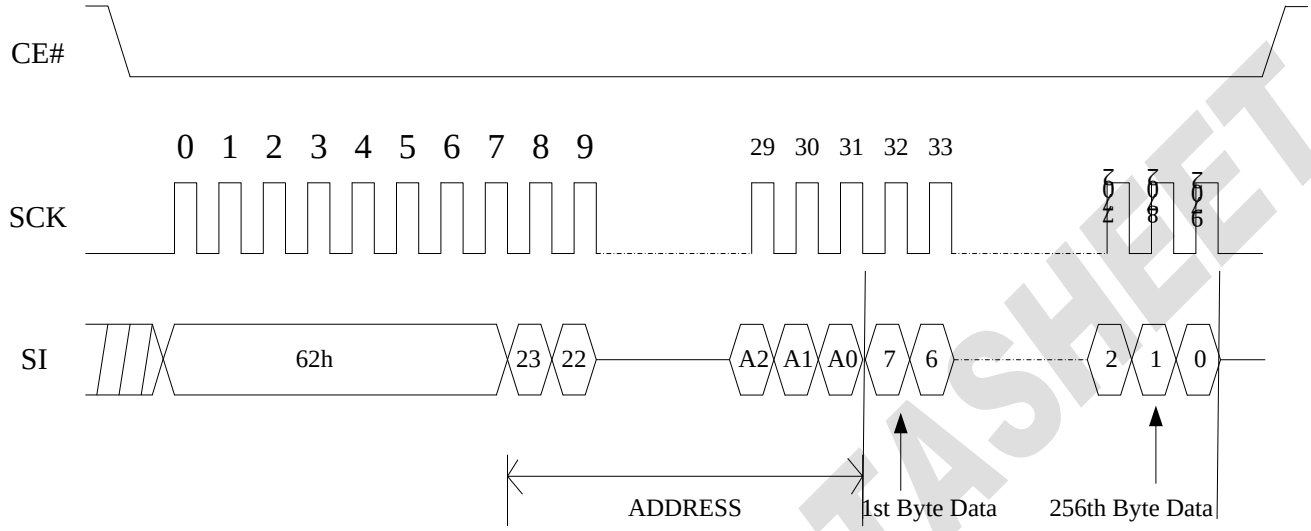
The Information Row Program (IRP) instruction allows up to 256 bytes data to be programmed into memory in a single operation.Before the execution of PAGE_PROG instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The ILP instruction code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the ILP instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. A byte cannot be reprogrammed without first erasing the whole sector or block.

Figure 44. IRP COMMAND (Information Row Program) OPERATION



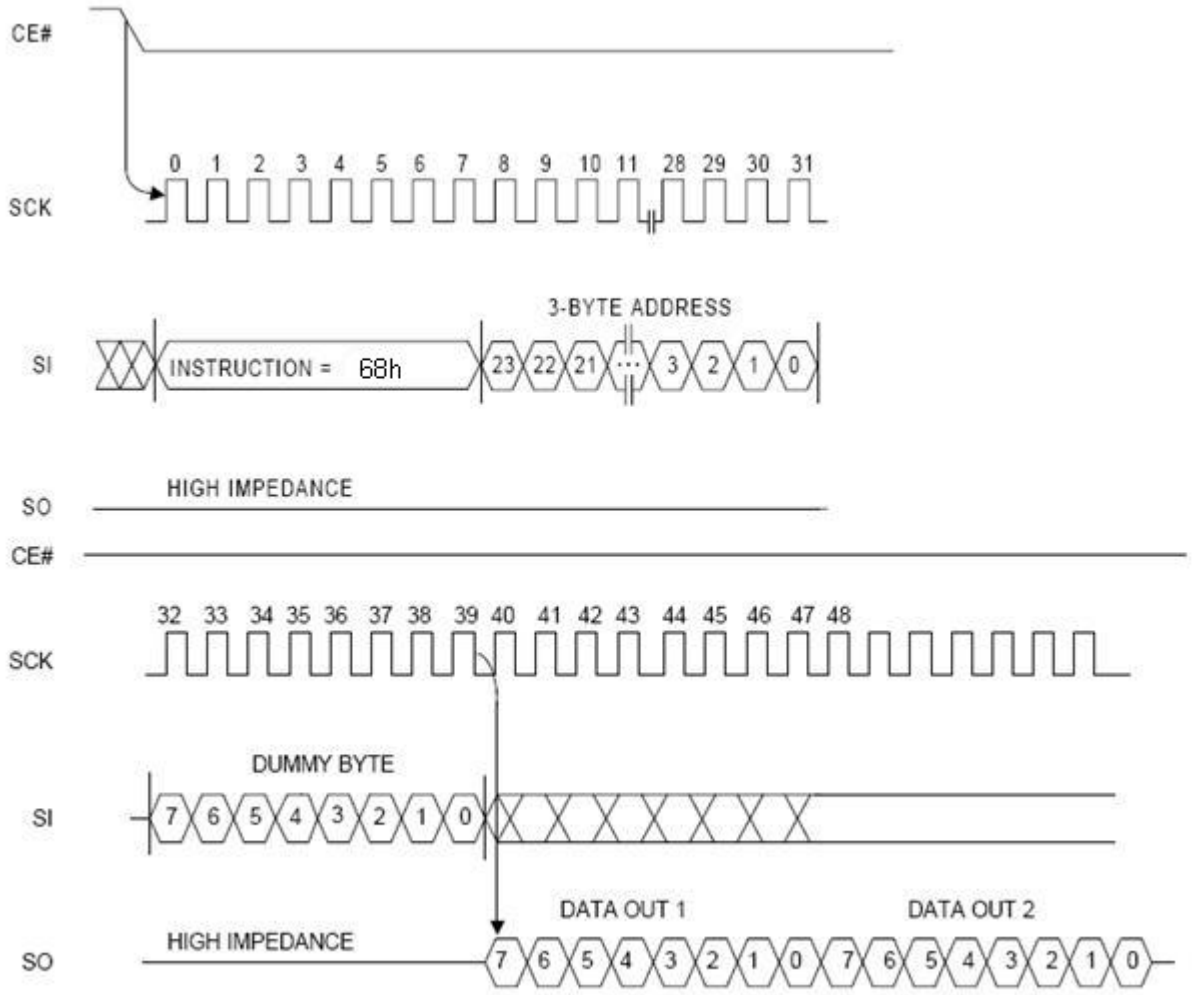
IRRD COMMAND (Information Row Read) OPERATION

The IRRD instruction is used to read memory data at up to a 133 MHz clock.

The IRRD instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single IRRD instruction. The IRRD instruction is terminated by driving CE# high (V_{IH}). If a IRRD instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle

Figure 45. IRRD COMMAND (Information Row Read) OPERATION



DEVICE OPERATION (CONTINUED)

FRDTR COMMAND (FAST READ DTR Mode) OPERATION

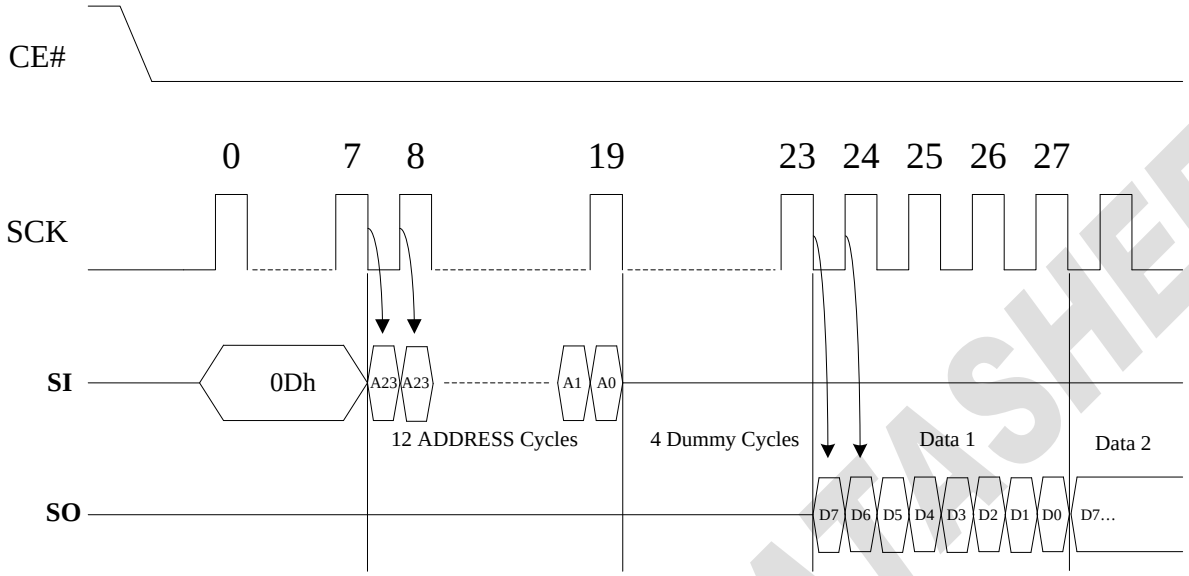
The FRDTR instruction is for doubling reading data out, signals are triggered on both rising and falling edge of clock. The address is latched on both rising and falling edge of SCLK, and data of each bit shifts out on both rising and falling edge of SCLK at a maximum frequency fc2. The 2-bit address can be latched-in at one clock, and 2-bit data can be read out at one clock, which means one bit at rising edge of clock, the other bit at falling edge of clock. The first address byte can be at any location.

The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FRDTR instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FRDTR instruction is: CS# goes low ’ sending FRDTR instruction code (1bit per clock) ’ 3-byte address on SI (2-bit per clock) ’ 6-dummy clocks (default) on SI ’ data out on SO (2-bit per clock) ’ to end FRDTR operation can use CS# to high at any time during data out. (Please refer to Figure 19)

While Program/Erase/Write Status Register cycle is in progress, FRDTR instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 46. FRDTR COMMAND (Fast Read DTR Mode) OPERATION



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

FRDDTR COMMAND (FAST READ Dual IO DTR Mode) OPERATION

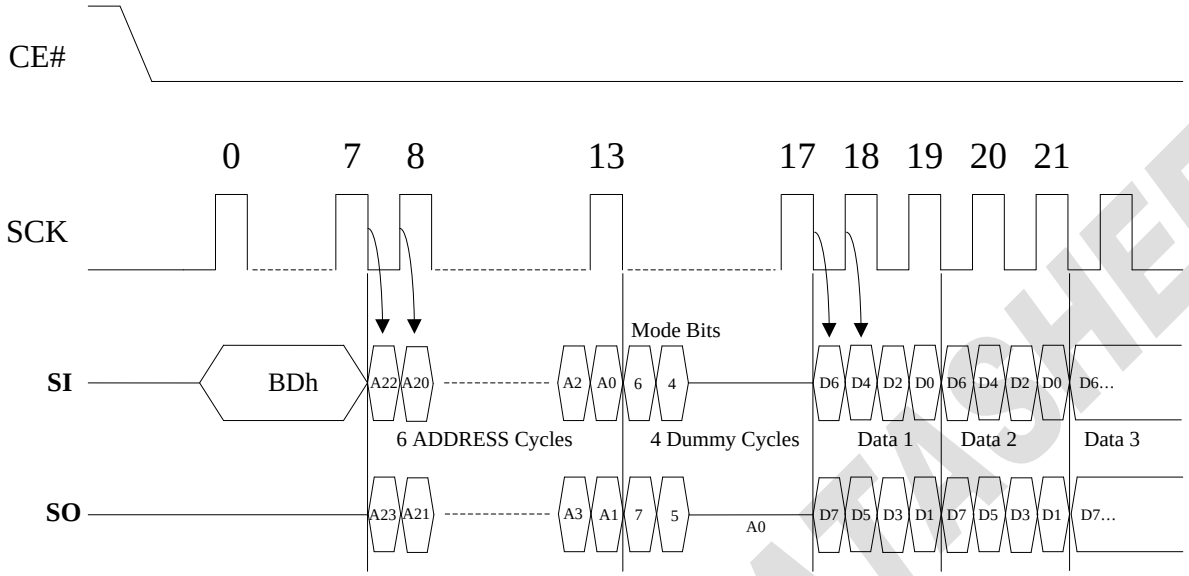
The FRDDTR instruction enables Double Transfer Rate throughput on dual I/O of Serial Flash in read mode. The address (interleave on dual I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on dual I/O pins) shift out on both rising and falling edge of SCLK at a maximum frequency ft2. The 4-bit address can be latched-in at one clock, and 4-bit data can be read out at one clock, which means two bits at rising edge of clock, the other two bits at falling edge of clock. The first address byte can be at any location.

The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FRDDTR instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing FRDDTR instruction, the following address/dummy/ data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing FRDDTR instruction is: CS# goes low ’ sending FRDDTR instruction (1-bit per clock) ’ 24-bit address interleave on SIO1 & SIO0 (4-bit per clock) ’ 6-bit dummy clocks on SIO1 & SIO0 ’ data out interleave on SIO1 & SIO0 (4-bit per clock) ’ to end FRDDTR operation can use CS# to high at any time during data out (Please refer to Figure 21 for 2 x I/O Double Transfer Rate Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, FRDDTR instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 47. FRDDTR COMMAND (Fast Read Dual IO DTR Mode) OPERATION



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

FRQDTR COMMAND (FAST READ Quad IO DTR Mode) OPERATION

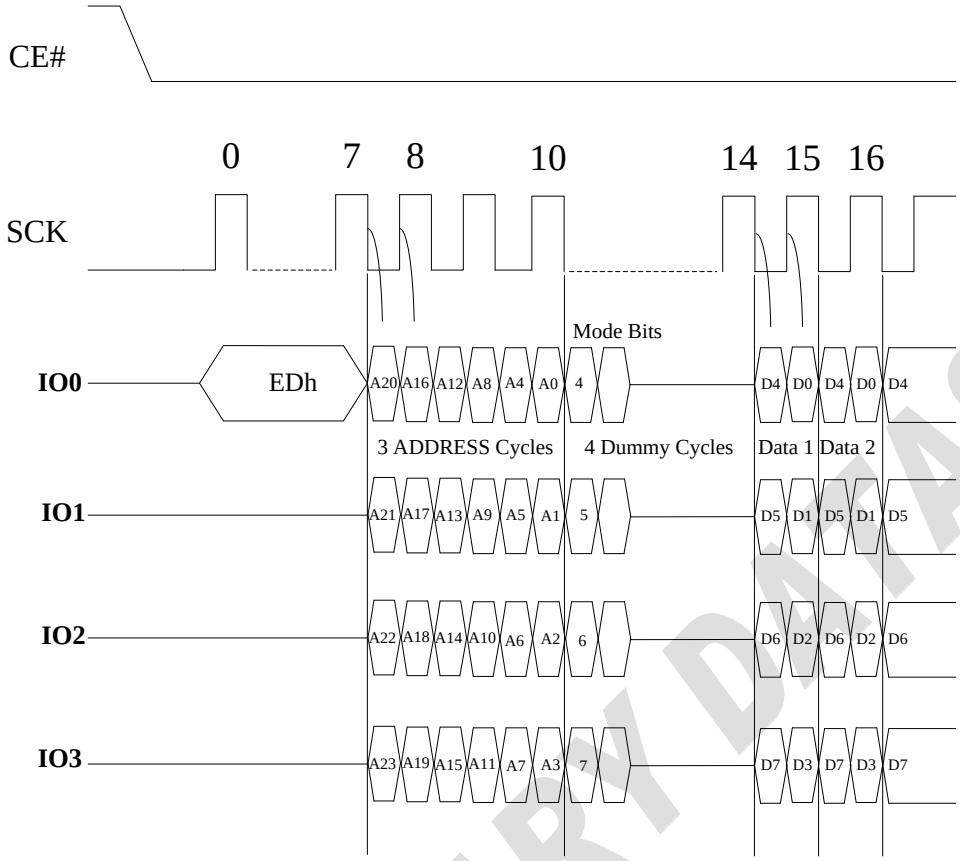
The FRQDTR instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the FRQDTR instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK at a maximum frequency fq2. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FRQDTR instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing FRQDTR instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

The sequence of issuing FRQDTR instruction is: CS# goes low ’ sending FRQDTR instruction (1-bit per clock) ’ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) ’ 8 dummy clocks ’ data out interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) ’ to end FRQDTR operation can use CS# to high at any time during data out (Please refer to Figure 24 for 4 x I/O Read Mode Double Transfer Rate Timing Waveform).

Another sequence of issuing enhanced mode of FRQDTR instruction especially useful in random access is: CS# goes low ’ sending FRQDTR instruction (1-bit per clock) ’ 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) ’ performance enhance toggling bit P[7:0] ’ 7 dummy clocks ’ data out(8-bit per clock) still CS# goes high ’ CS# goes low (eliminate 4 Read instruction) ’ 24-bit random access address (Please refer to Figure 25 for 4x I/O Double Transfer Rate read enhance performance mode timing waveform).

While Program/Erase/Write Status Register cycle is in progress, FRQDTR instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 48. FRQDTR COMMAND (Fast Read Quad IO DTR Mode) OPERATION



**** Number of dummy cycles depends on clock speed. Detail information in Table 10. Read Dummy Cycles**

ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-55°C to +130°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to VCC + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to VCC + 0.5 V
VCC (2)		-0.5 V to +6.0 V

Notes:
1. Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device conditions that exceed those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot V_{CC} by + 2.0 V for a period of time not to exceed 20 ns. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot GND by -2.0 V for a period of time not to exceed 20 ns.

DC AND AC OPERATING RANGE

Part Number	IS25LQ064
Operating Temperature (Extended Grade)	-40°C to 105°C
Operating Temperature (Industrial Grade)	-40°C to 85°C
Operating Temperature (Automotive, A1 Grade)	-40°C to 85°C
Operating Temperature (Automotive, A2 Grade)	-40°C to 105°C
Operating Temperature (Automotive, A3 Grade)	-40°C to 125°C
Vcc Power Supply	2.3 V – 3.6 V

DC CHARACTERISTICS

Applicable over recommended operating range from:
V_{CC} = 2.3 V to 3.6 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.6V at 50MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.6V at 50MHz, SO = Open			15	20	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.6V, CE# = V_{CC}				30	□A
I_{SB2}	Vcc Standby Current TTL	V_{CC} =3.6V, CE# = V_{IH} to V_{CC}				3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	□A
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 135°C				1	□A
V_{IL}	Input Low Voltage			-0.5		0.3V_{CC}	V
V_{IH}	Input HIgh Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.3V < V_{CC} < 3.6V	I_{OL} = 2.1 mA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 □A	V_{CC} - 0.2			V

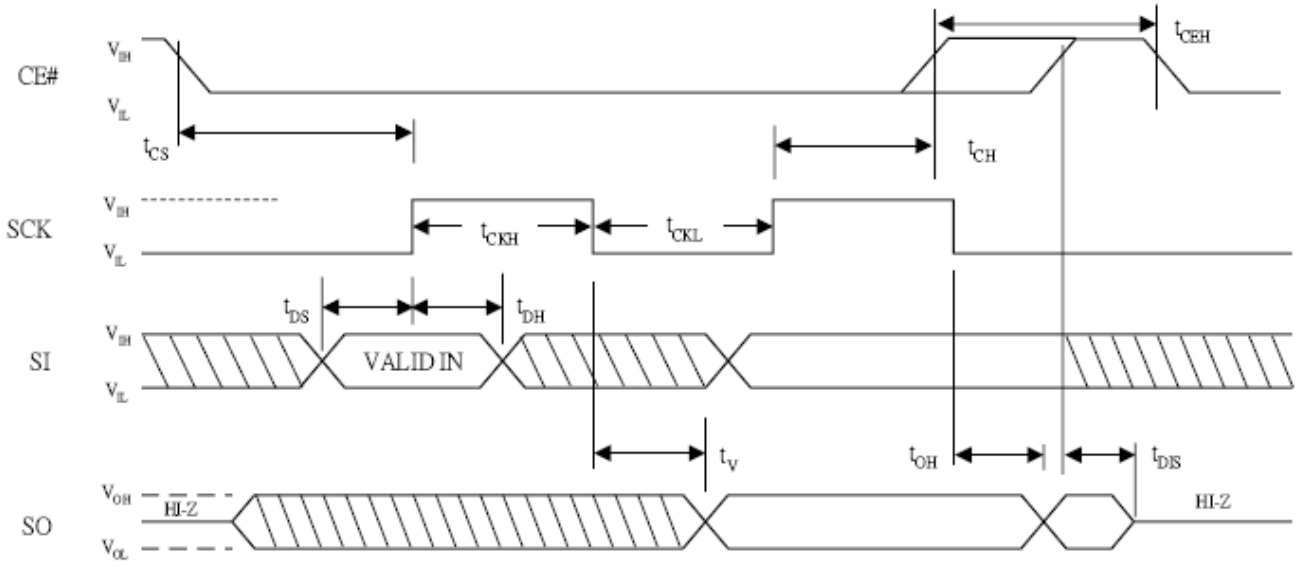
AC CHARACTERISTICS

Applicable over recommended operating range from V_{CC} = 2.3 V to 3.6 V
C_L = 1 TTL Gate and30 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{CT}	Clock Frequency for fast read mode	0		133	MHz
f_C	Clock Frequency for read mode	0		50	MHz
fc2	Clock Frequency for fast read DTR mode	0		66	MHz
ft2	Clock Frequency for fast read Dual I/O DTR mode	0		66	MHz
fq2	Clock Frequency for fast read Quad I/O DTR mode	0		66	MHz
t_{RI}	Input Rise Time			8	ns
t_{FI}	Input Fall Time			8	ns
t_{CKH}	SCK High Time	4			ns
t_{CKL}	SCK Low Time	4			ns
t_{CEH}	CE# High Time	7			ns
t_{CS}	CE# Setup Time	5			ns
t_{CH}	CE# Hold Time	5			ns
t_{DS}	Data In Setup Time	2			ns
t_{DH}	Data in Hold Time	2			ns
t_{HS}	Hold Setup Time	8			ns
t_{HD}	Hold Time	5			ns
t_V	Output Valid			8	ns
t_{OH}	Output Hold Time Normal Mode	2			ns
t_{LZ}	Hold to Output Low Z			12	ns
t_{HZ}	Hold to Output High Z			12	ns
t_{DIS}	Output Disable Time			8	ns
t_{EC}	Sector Erase Time		50	150	ms
	Block Erase Time (32Kbyte)		0.25	0.75	s
	Block Erase time (64Kbyte)		0.5	1.5	s
	Chip Erase Time (32Mb)		30	60	s
t_{PP}	Page Program Time		0.6	1.5	ms
t_{VCS}	V_{CC} Set-up Time	50			□S
t_{res1}	Release deep power down			3	□S
t_{dp}	Deep power down			3	□S
t_w	Write Status Register time		10	15	ms
tsus	Suspend to suspend ready			20	us
trs	Resume to another suspend			1	ms
tsrst	Software Reset cover time			15	ms
Tws	Suspend time			20	us

AC CHARACTERISTICS (CONTINUED)

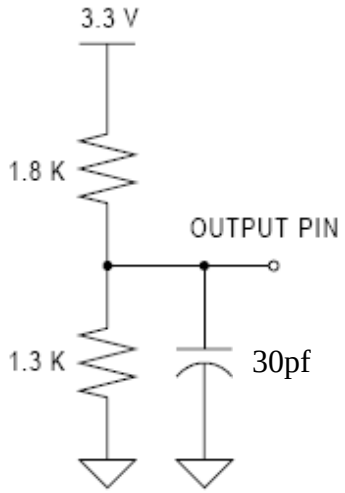
SERIAL INPUT/OUTPUT TIMING (1)



Note: 1. For SPI Mode 0 (0,0)

AC CHARACTERISTICS (CONTINUED)

OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

Note: 1. Input Pulse Voltage : 0.2Vcc to 0.8Vcc.
2. Input Timing Reference Voltages :
0.3Vcc to 0.7Vcc.
3. Output Timing Reference Voltage : Vcc/2.

POWER-UP AND POWER-DOWN

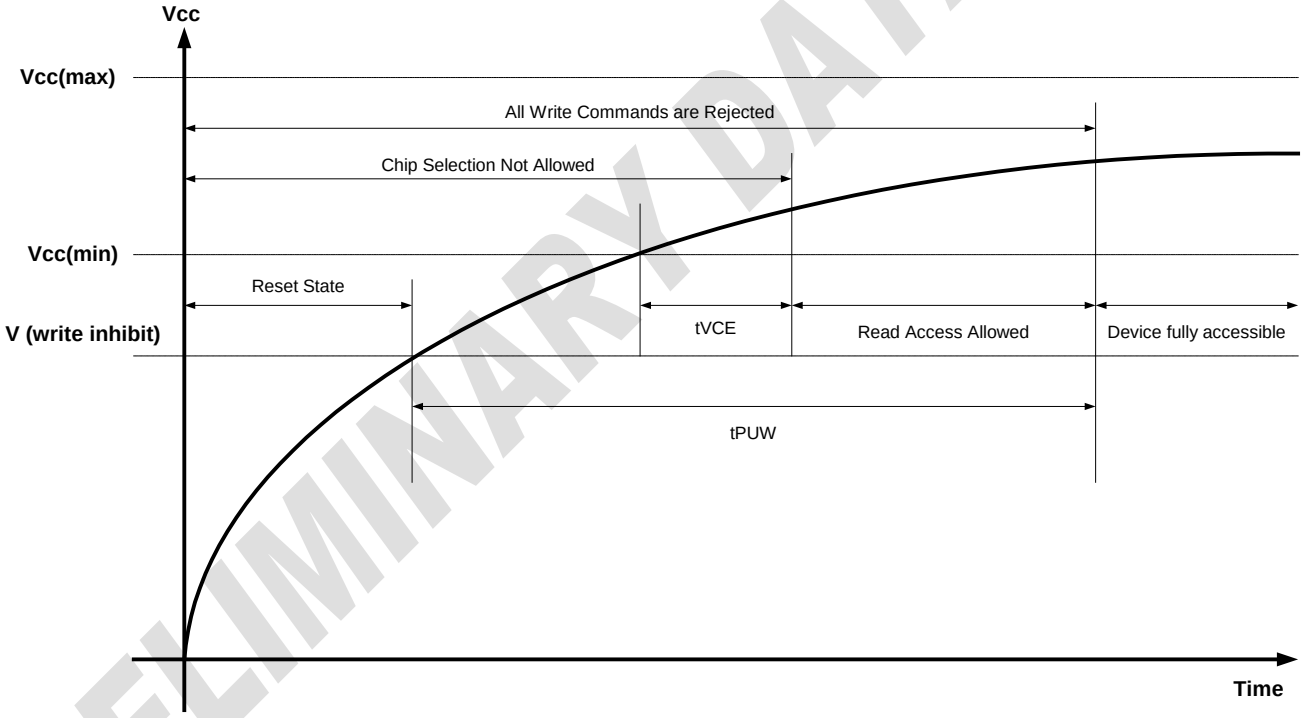
At Power-up and Power-down, the device must not be selected (CE# must follow the voltage applied on Vcc) until Vcc reaches the correct value:
- Vcc(min) at Power-up, and then for a further delay of tVCE
0 Vss at Power-down

Usually a simple pull-up resistor on CE# can be used to insure safe and proper Power-up and Power-down. To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while Vcc is less than the POR threshold value (Vwi) during power up, the device does not respond to any instruction until a time delay of tPUW has elapsed after the moment that Vcc rised above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, Vcc is still below Vcc(min). No Write Status Register, Program or Erase instructions should be sent until the later of:
- tPUW after Vcc passed the VWI threshold
- tVCE after Vcc passed the Vcc(min) level

At Power-up, the device is in the following state:
- The device is in the Standby mode
- The Write Enable Latch (WEL) bit is reset

At Power-down, when Vcc drops from the operating voltage, to below the Vwi, all write operations are disabled
and the device does not respond to any write instruction.

Power up timing



Symbol	Parameter	Min.	Max.	Unit
t_{VCE} *1	Vcc(min) to CE# Low	10		us
t_{PUW} *1	Power-Up time delay to Write instruction	1	10	ms
V_{WI} *1	Write Inhibit Voltage		1.9	V
Note : *1. These parameters are characterized only.				

PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	50	200	
Block Erase Time	s	0.25	1	
Chip Erase Time (64Mb)	s	22.5	30	
Page Programming Time	ms	0.6	1.5	
Byte Program	us	8	25	

Note: These parameters are characterized and are not 100% tested.

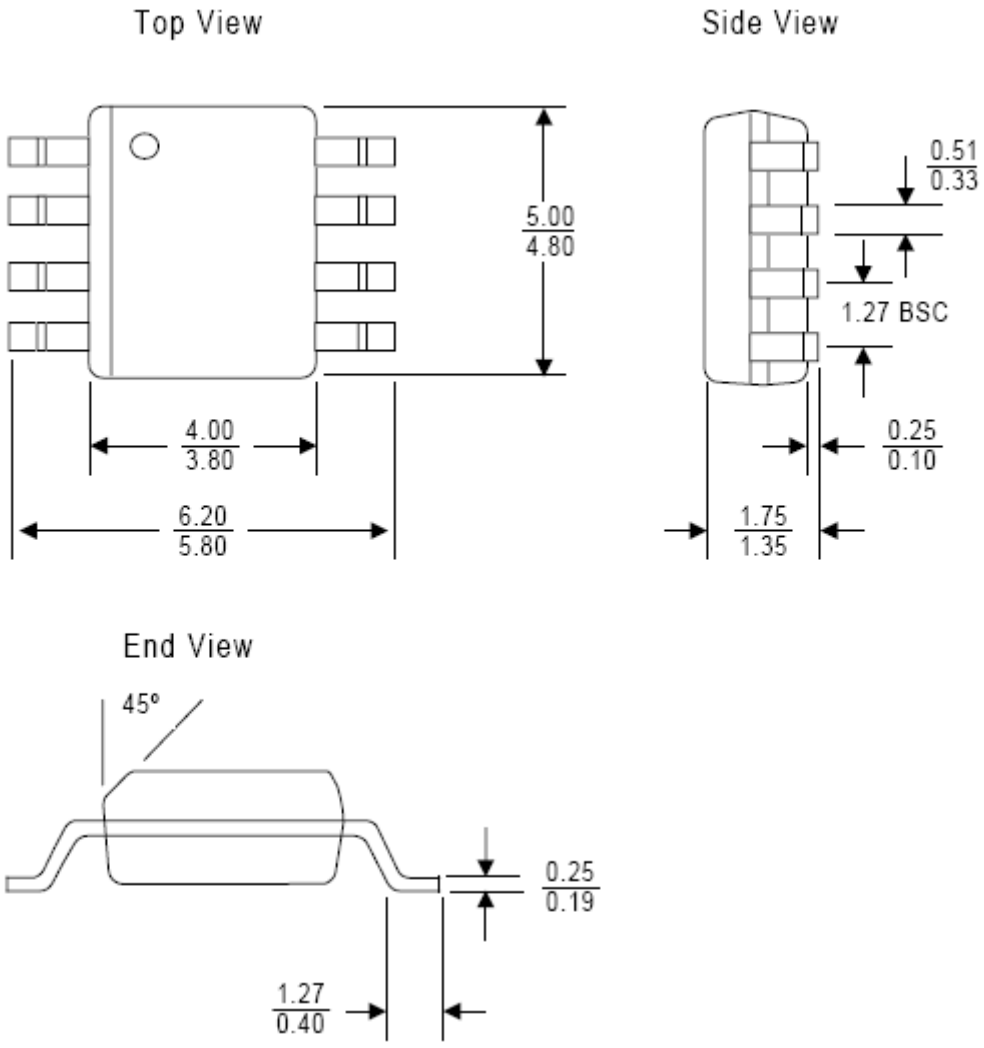
RELIABILITY CHARACTERISTICS

Parameter	Min	Typ	Unit	Test Method
Endurance	100,000		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD – Human Body Model	2,000		Volts	JEDEC Standard A114
ESD – Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: These parameters are characterized and are not 100% tested.

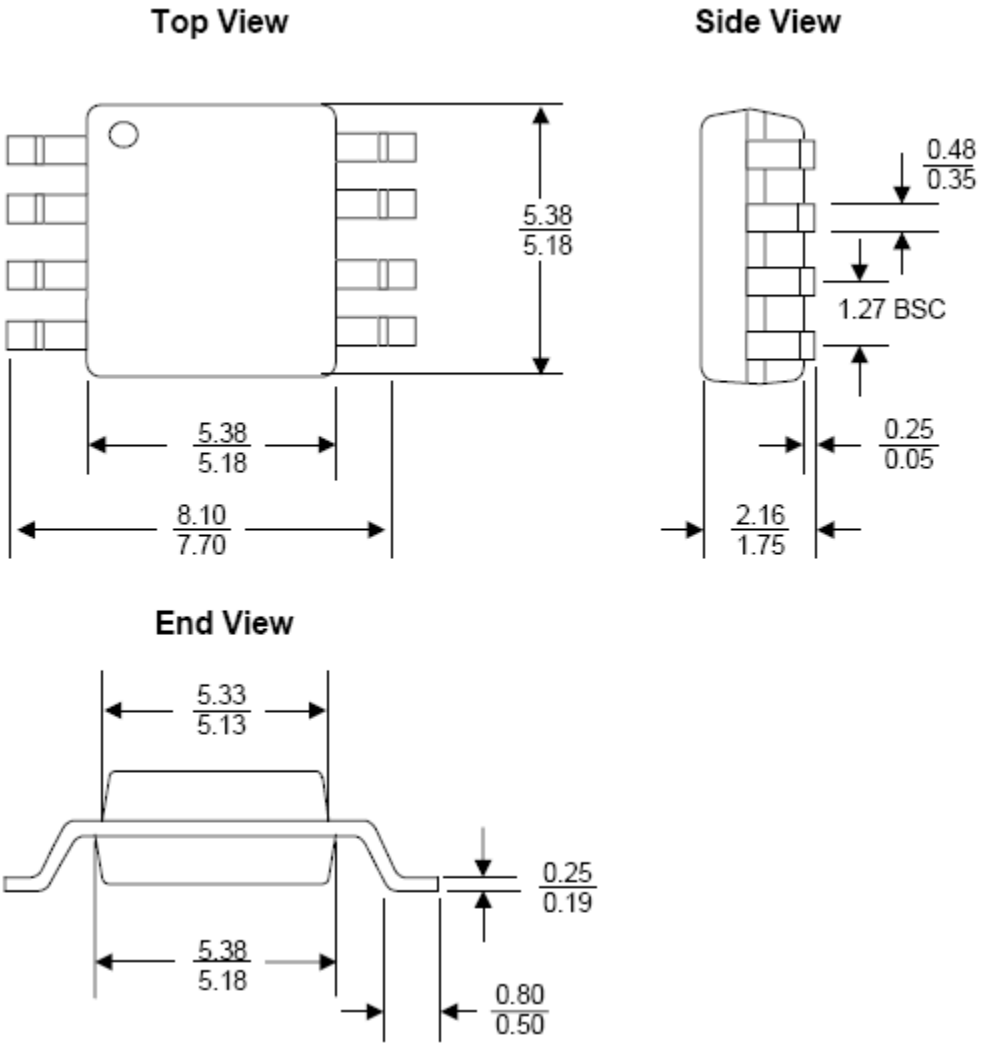
PACKAGE TYPE INFORMATION

JN
8-Pin JEDEC 150mil Broad Small Outline Integrated Circuit (SOIC) Package (measure in millimeters)



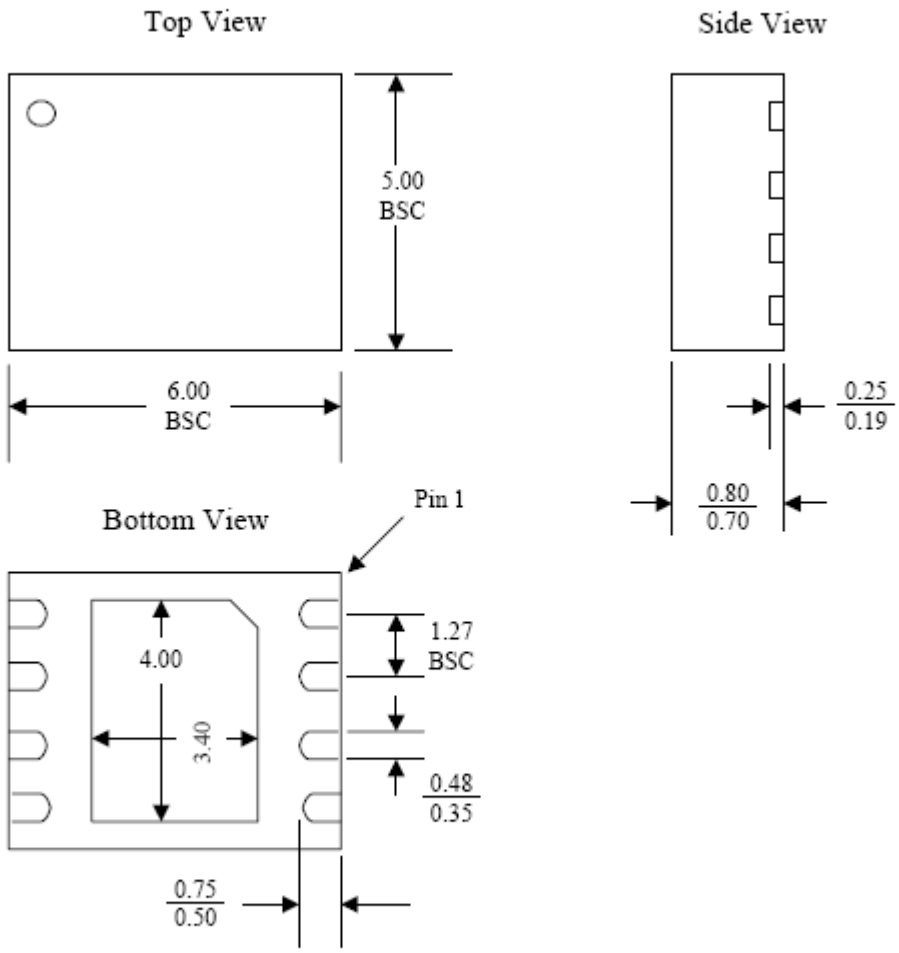
PACKAGE TYPE INFORMATION (CONTINUED)

JB
8-Pin JEDEC 208mil Broad Small Outline Integrated Circuit (SOIC) Package
(measure in millimeters)



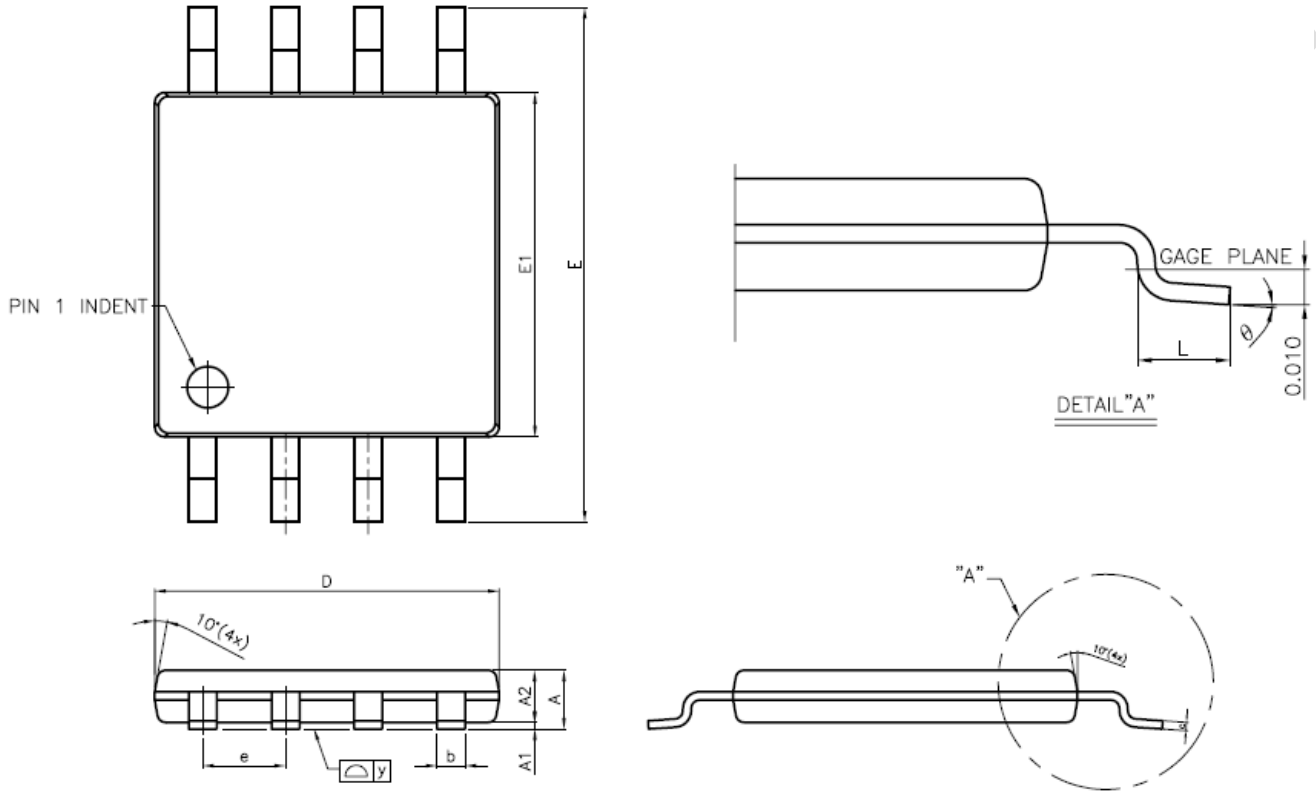
PACKAGE TYPE INFORMATION (CONTINUED)

JK
8-Contact Ulta-Thin Small Outline No-Lead (WSON) Package (measure in millimeters)



PACKAGE TYPE INFORMATION (CONTINUED)

JF
8-Pin 208mil VSOP Package



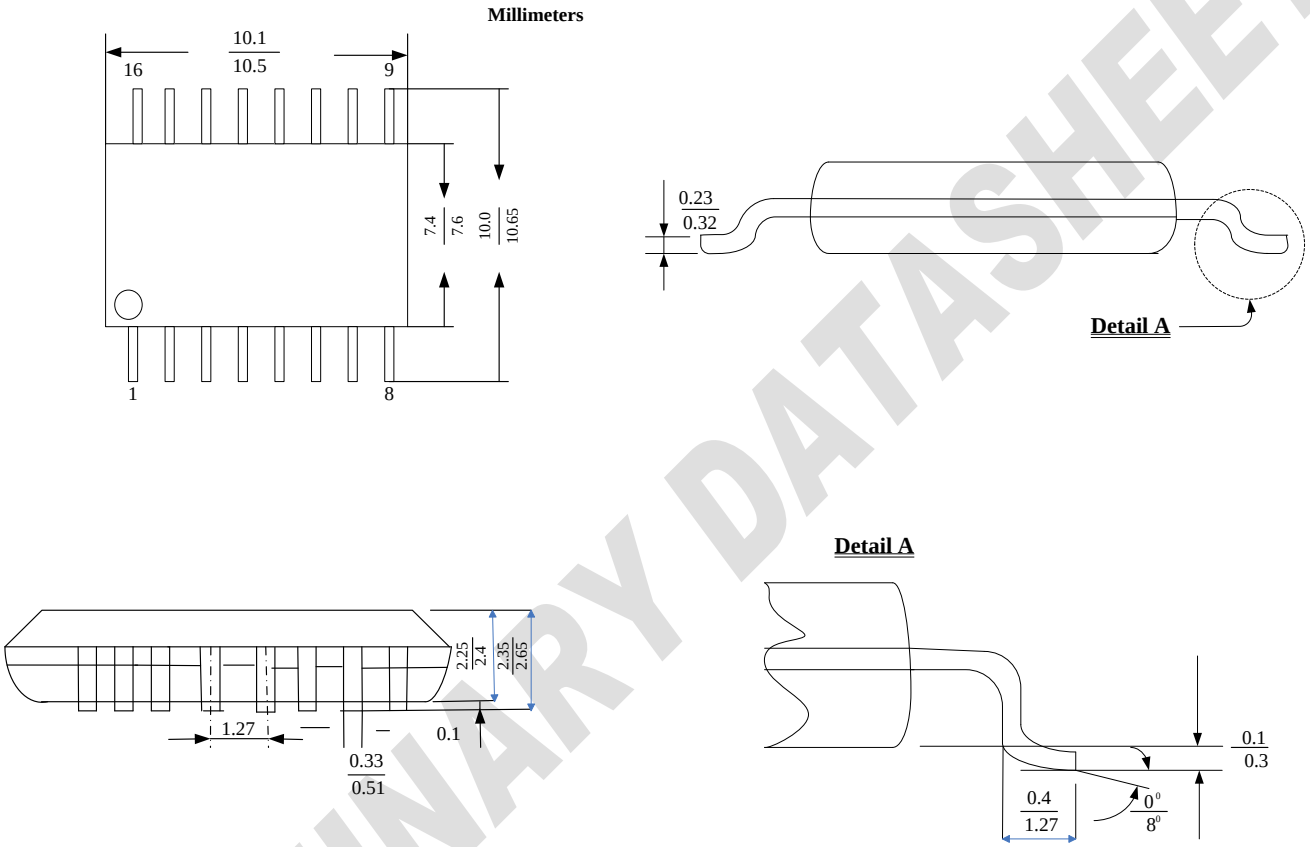
NOTE :

1. CONTROLLING DIMENSION : INCH
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
4. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
5. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.00	—	—	0.039
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.80	0.85	0.030	0.031	0.033
b	0.35	0.42	0.48	0.014	0.017	0.019
c	—	0.127 REF.	—	—	0.005 REF.	—
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	—	1.27	—	—	0.050	—
L	0.50	0.65	0.80	0.020	0.026	0.031
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

PACKAGE TYPE INFORMATION (CONTINUED)

JM
16 pin – 16-lead Plastic Small Outline, 300 mils body width, package outline



Appendix1: Safe Guard function

Safe Guard function is a security function for customer to protect by sector (4Kbyte).
Every sector has one bit register to decide it will under safe guard protect or not. (“0”means protect and “1” means not protect by safe guard.) IS25LQ064 (sector 0~sector 2047)

Mapping table for safe guard register

		Address	D7	D6	D5	D4	D3	D2	D1	D0
Block0	Sector0	000h	1	1	1	1	1	1	1	0
	Sector1	000h	1	1	1	1	1	1	0	1
	Sector2	000h	1	1	1	1	1	0	1	1
	Sector3	000h	1	1	1	1	0	1	1	1
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Sector14	001h	1	0	1	1	1	1	1	1
	Sector15	001h	0	1	1	1	1	1	1	1
Block1	Sector All	002h	0 = protect , 1=unprotect							
Block2	Sector All	003h	0 = protect , 1=unprotect							
Block3	Sector All	004h	0 = protect , 1=unprotect							
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Block124	Sector All	0FBh	0 = protect , 1=unprotect							
Block125	Sector All	0FCh	0 = protect , 1=unprotect							
Block126	Sector All	0FDh	0 = protect , 1=unprotect							
Block127	Sector2031	0FEh	1	1	1	1	1	1	1	0
	Sector2032	0FEh	1	1	1	1	1	1	0	1
	Sector2033	0FEh	1	1	1	1	1	0	1	1
	Sector2034	0FEh	1	1	1	1	0	1	1	1
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Sector2046	0FFh	1	0	1	1	1	1	1	1
	Sector2047	0FFh	0	1	1	1	1	1	1	1

Note: if safe guard function is enabled, the chip/block erase command will be disabled in the block which have any sector under safe guard protect.

Read Safe Guard register

The READ Safe Guard instruction code is transmitted via the SIO line, followed by three address bytes (A23 - A0) of the first register location to be read. The first byte data (D7 - D0) addressed is then shifted out on the SO line, MSb first. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (V_{IH}) after the data comes out.

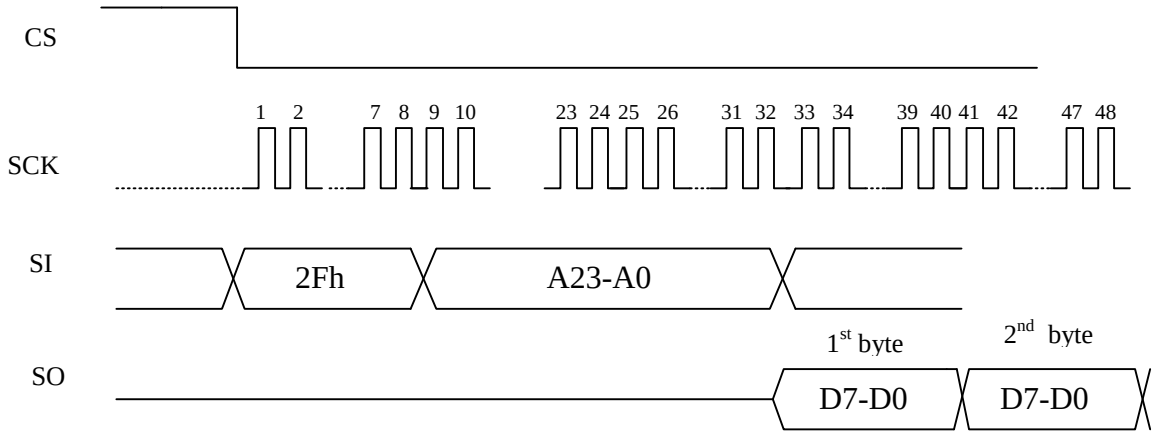


Fig a. Timing waveform of Read Safe guard register

Erase Safe Guard register

If we want to erase the safe guard register to let the flash into unprotect status, it needs five continuous instructions. If any instruction is wrong, the erase command will be ignored. Erase wait time follow product erase timing spec.
Fig b. shows the complete steps for Erase safe guard register.

Program Safe Guard register

If we want to erase the safe guard register to let the flash into unprotect status, it needs five continuous instructions. If any instruction is wrong, the program command will be ignored. The Program safe guard instruction allows up to 256 bytes data to be programmed into memory in a single operation. Program wait time follow product program timing spec.

Fig c. shows the complete steps for program safe guard register.

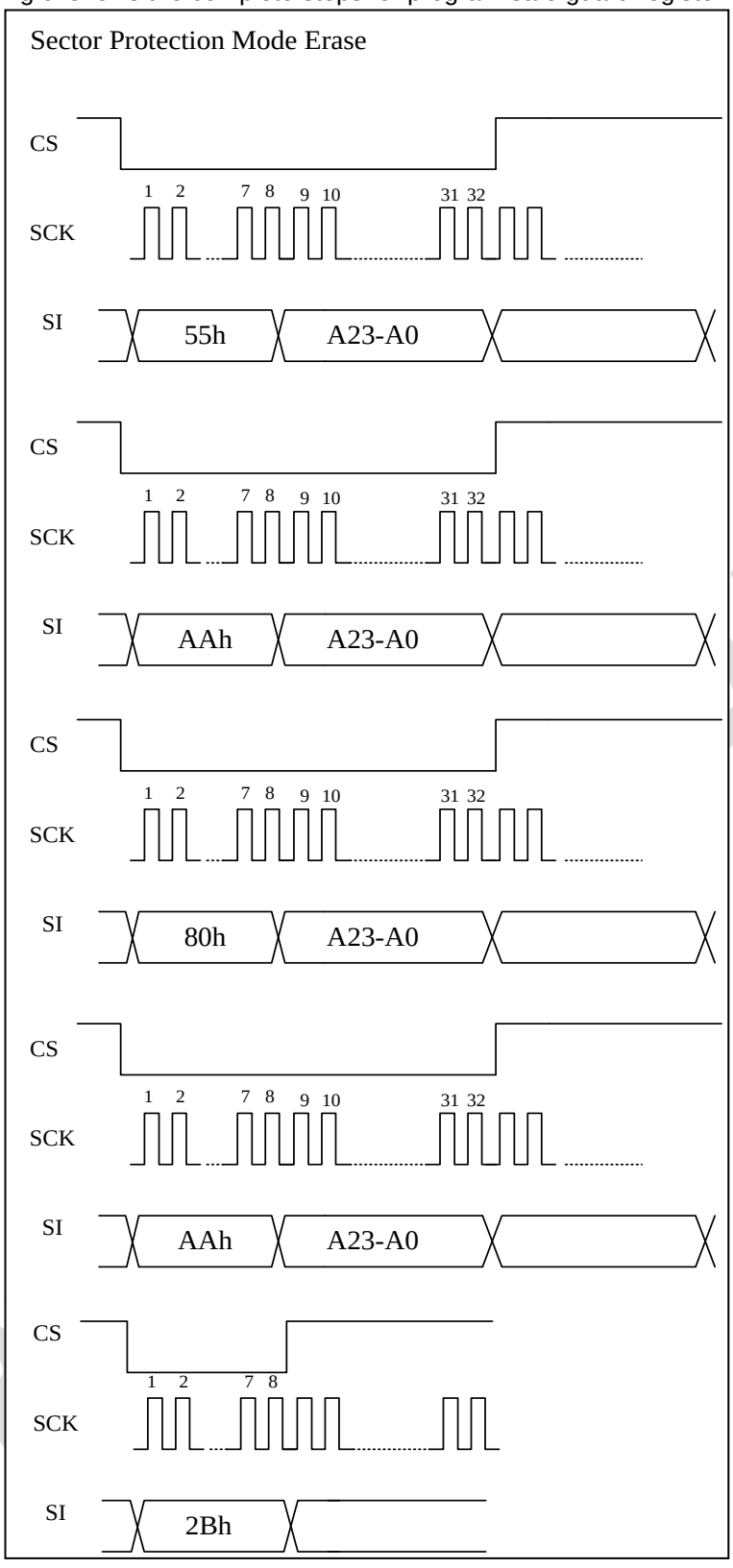
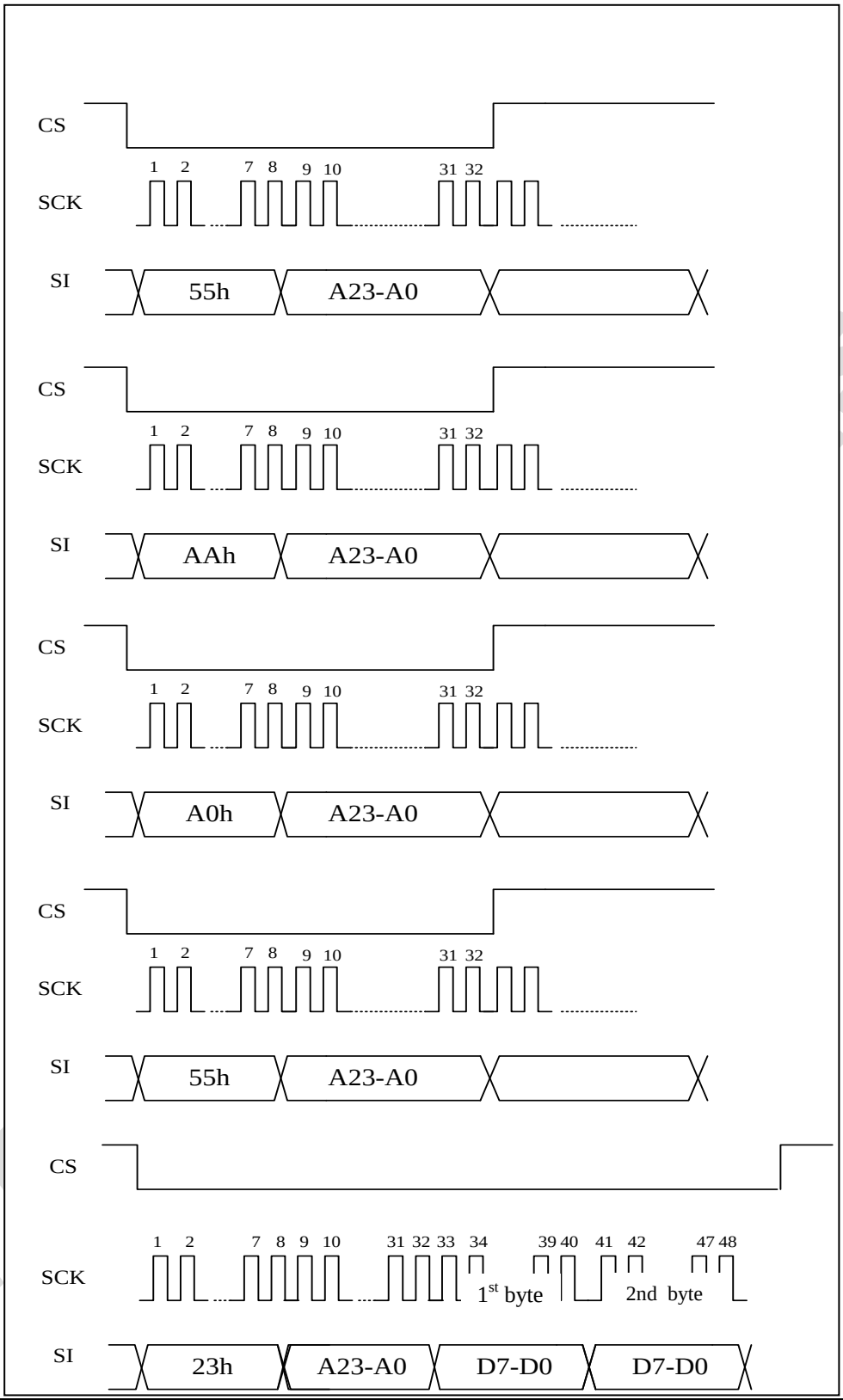
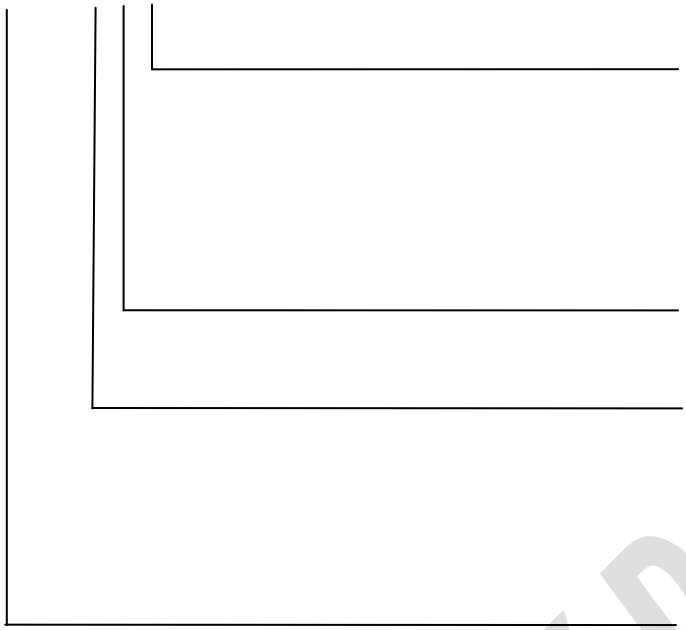


Fig c. program safe guard register



PRODUCT ORDERING INFORMATION

IS25LQ* - JN L E**



Temperature Range
E = Extended Grade (-40°C to +105°C)
I = Industrial Grade (-40°C to +85°C)
A1 = Automotive, A1 Grade (-40°C to +85°C)
A2 = Automotive, A2 Grade (-40°C to +105°C)
A3 = Automotive, A3 Grade (-40°C to +125°C)

Environmental Attribute
L = Lead-free (Pb-free) package

Package Type
JN = 8-pin SOIC 150mil
JB = 8-pin SOIC 208-mil
JK = 8-pin WSON
JF = 8-pin VSOP 208-mil
JM = 16-pin SOIC 300-mil

Device Number
IS25LQ064

ORDERING INFORMATION:

Density	Frequency (MHz)	Order Part Number	Package
64M	133	IS25LQ064-JNLE	8-pin SOIC 150mil
		IS25LQ064-JBLE	8-pin SOIC 208-mil
		IS25LQ064-JKLE	8-pin WSON
		IS25LQ064-JFLE	8-pin VSOP 208-mil
		IS25LQ064-JMLE	16-pin SOIC 300-mil
		IS25LQ064-JNLI	8-pin SOIC 150mil
		IS25LQ064-JBLI	8-pin SOIC 208-mil
		IS25LQ064-JKLI	8-pin WSON
		IS25LQ064-JFLI	8-pin VSOP 208-mil
		IS25LQ064-JMLI	16-pin SOIC 300-mil
		IS25LQ064-JNLA1	8-pin SOIC 150mil
		IS25LQ064-JBLA1	8-pin SOIC 208-mil
		IS25LQ064-JKLA1	8-pin WSON
		IS25LQ064-JFLA1	8-pin VSOP 208-mil
		IS25LQ064-JMLA1	16-pin SOIC 300-mil
		IS25LQ064-JNLA2	8-pin SOIC 150mil
		IS25LQ064-JBLA2	8-pin SOIC 208-mil
		IS25LQ064-JKLA2	8-pin WSON
		IS25LQ064-JFLA2	8-pin VSOP 208-mil
		IS25LQ064-JMLA2	16-pin SOIC 300-mil
		IS25LQ064-JNLA3	8-pin SOIC 150mil
		IS25LQ064-JBLA3	8-pin SOIC 208-mil
		IS25LQ064-JKLA3	8-pin WSON
		IS25LQ064-JFLA3	8-pin VSOP 208-mil
		IS25LQ064-JMLA3	16-pin SOIC 300-mil