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PCA9534
REMOTE 8-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS
SCPS124C−SEPTEMBER 2006−REVISED OCTOBER 2007

FEATURES

- **Low Standby Current Consumption of 1 μA Max**
- **I^{2}C to Parallel Port Expander**
- **Open-Drain Active-Low Interrupt Output**
- **Operating Power-Supply Voltage Range of 2.3 V to 5.5 V**
- **5-V Tolerant I/O Ports**
- **400-kHz Fast I^{2}C Bus**
- **Three Hardware Address Pins Allow up to Eight Devices on the I^{2}C/SMBus**
- **Input/Output Configuration Register**
- **Polarity Inversion Register**
- **Internal Power-On Reset**

- **Power-Up With All Channels Configured as Inputs**
- **No Glitch on Power Up**
- **Noise Filter on SCL/SDA Inputs**
- **Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
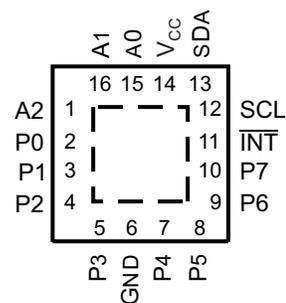 - **1000-V Charged-Device Model (C101)**
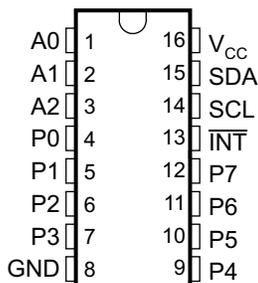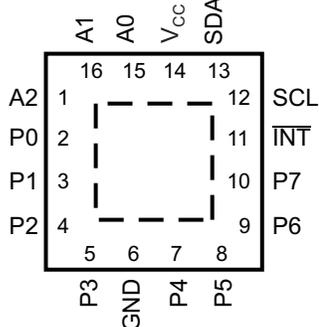
DESCRIPTION/ORDERING INFORMATION

This 8-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL), serial data (SDA)].

The PCA9534 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) register. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9534 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I^{2}C/SMBus state machine.

The PCA9534 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^{2}C bus. Thus, the PCA9534 can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.

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Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^{2}C address and allow up to eight devices to share the same I^{2}C bus or SMBus.

The PCA9534 is pin-to-pin and I^{2}C address compatible with the PCF8574. However, software changes are required due to the enhancements in the PCA9534 over the PCF8574.

The PCA9534 is a low-power version of the PCA9554. The only difference between the PCA9534 and PCA9554 is that the PCA9534 eliminates an internal I/O pullup resistor, which dramatically reduces power consumption in the standby mode when the I/Os are held low.

The PCA9534A and PCA9534 are identical, except for their fixed I^{2}C address. This allows for up to 16 of these devices (8 of each) on the same I^{2}C bus.

ORDERING INFORMATION

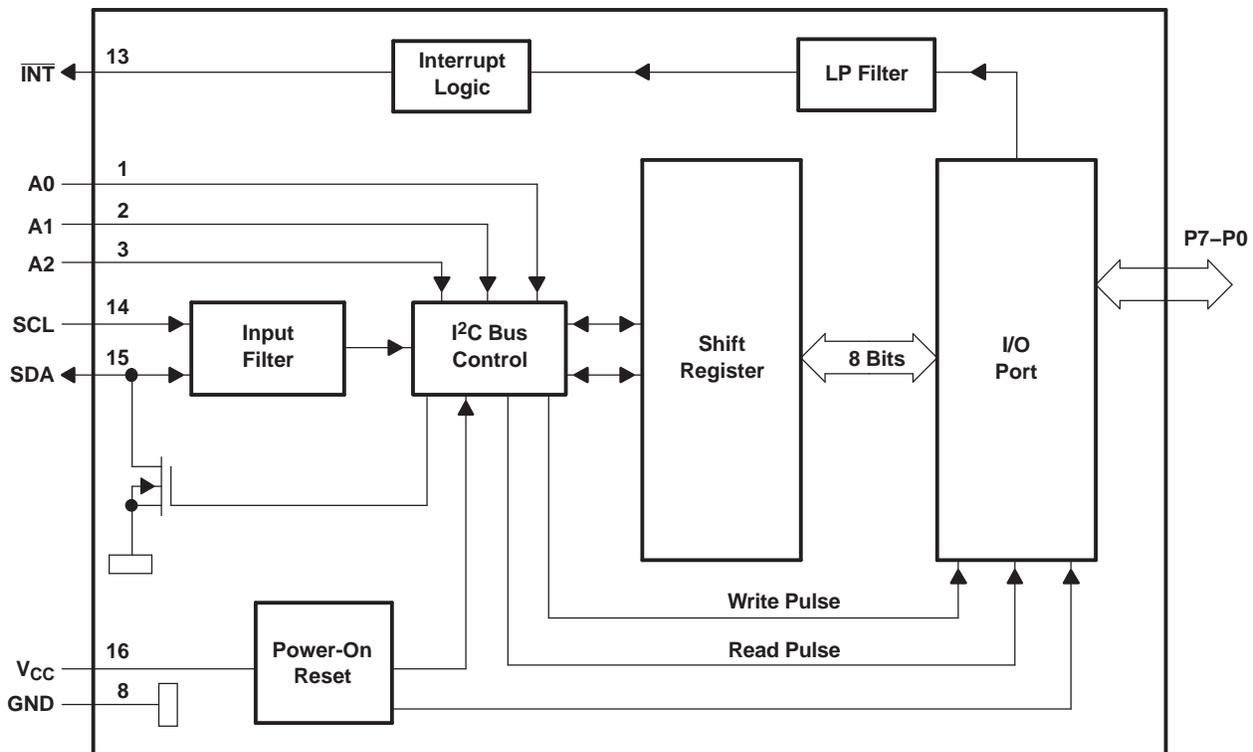| T$_A$	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGT	Reel of 3000	PCA9534RGTR	PREVIEW
	QFN – RGV	Reel of 2500	PCA9534RGVR	PD534
	QSOP – DBQ	Reel of 2500	PCA9534DBQR	PD534
	SOIC – DW	Tube of 40	PCA9534DW	PCA9534
		Reel of 2000	PCA9534DWR	
	SSOP – DB	Reel of 2000	PCA9534DBR	PD534
		Tube of 80	PCA9534DBT	
	TSSOP – PW	Tube of 90	PCA9534PW	PD534
		Reel of 2000	PCA9534PWR	
	TVSOP – DGV	Reel of 2000	PCA9534DGVR	PD534

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
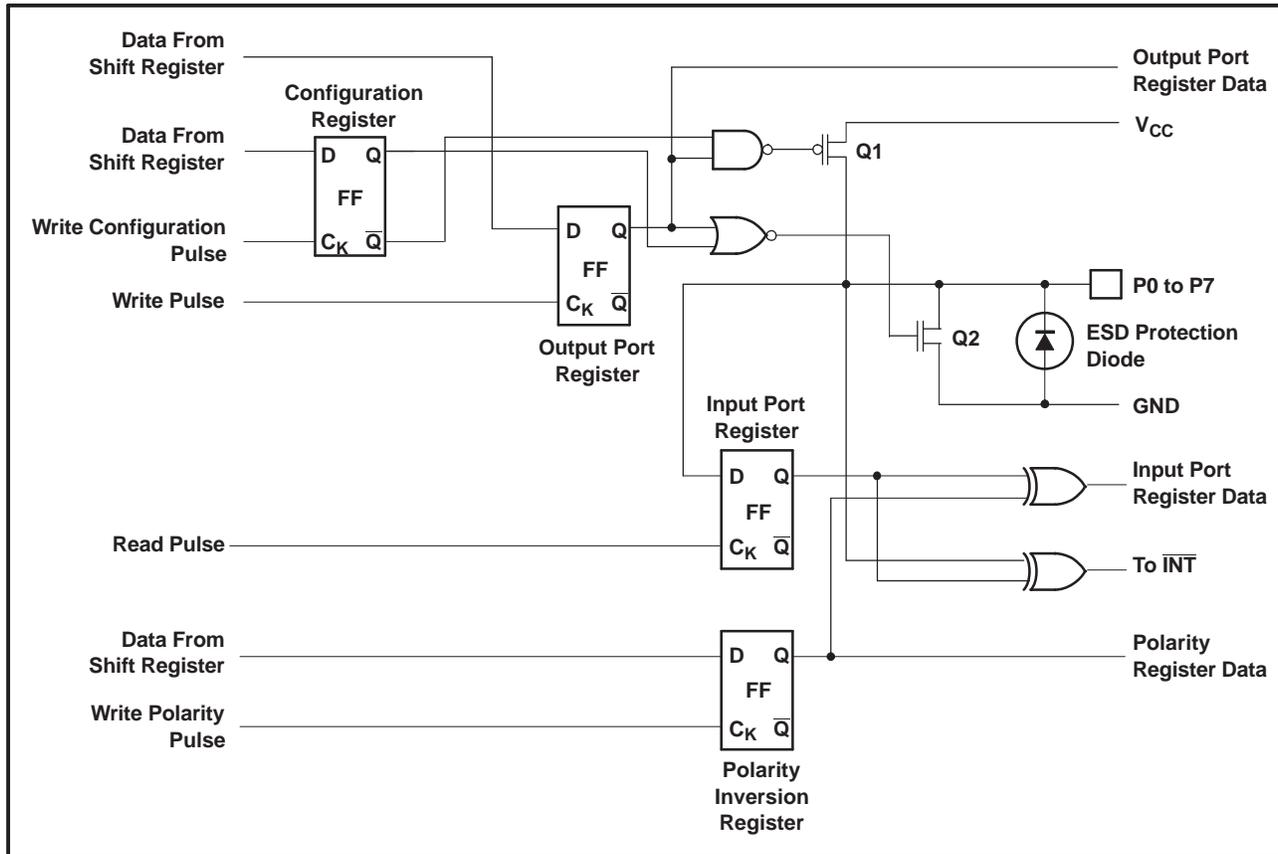
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TERMINAL FUNCTIONS

NO.		NAME	DESCRIPTION
QSOP (DBQ), SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT AND RGV)		
1	15	A0	Address input. Connect directly to V_{CC} or ground.
2	16	A1	Address input. Connect directly to V_{CC} or ground.
3	1	A2	Address input. Connect directly to V_{CC} or ground.
4	2	P0	P-port input/output. Push-pull design structure.
5	3	P1	P-port input/output. Push-pull design structure.
6	4	P2	P-port input/output. Push-pull design structure.
7	5	P3	P-port input/output. Push-pull design structure.
8	6	GND	Ground
9	7	P4	P-port input/output. Push-pull design structure.
10	8	P5	P-port input/output. Push-pull design structure.
11	9	P6	P-port input/output. Push-pull design structure.
12	10	P7	P-port input/output. Push-pull design structure.
13	11	$\overline{INT}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
14	12	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
15	13	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
16	14	V_{CC}	Supply voltage

LOGIC DIAGRAM (POSITIVE LOGIC)

A. Pin numbers shown are for DB, DBQ, DGV, DW, or PW package.

B. All I/Os are set to inputs at reset.

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SIMPLIFIED SCHEMATIC OF P0 TO P7

A. At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

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A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
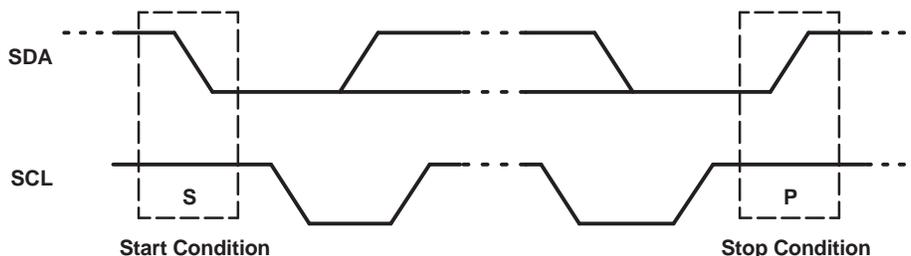

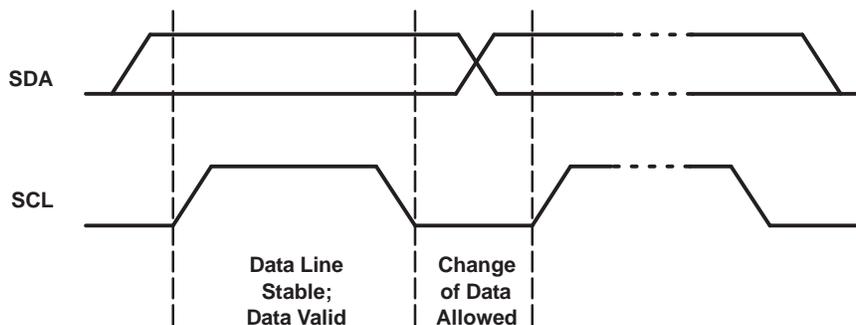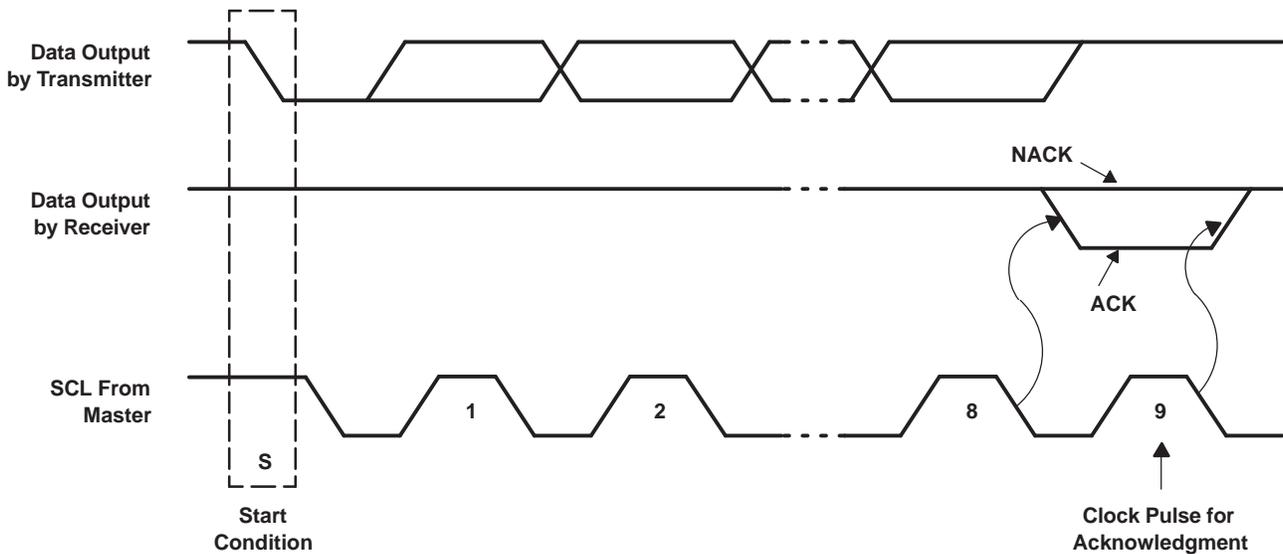**Figure 1. Definition of Start and Stop Conditions**

Figure 2. Bit Transfer

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Figure 3. Acknowledgment on I^{2}C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^{2}C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

Device Address

Figure 4 shows the address byte of the PCA9534.
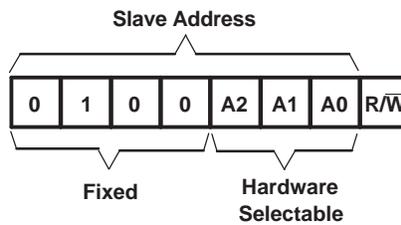
Figure 4. PCA9534 Address

Address Reference

INPUTS			I^{2}C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

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The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the PCA9534. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.
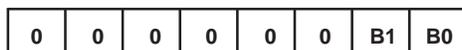
0	0	0	0	0	0	B1	B0

Figure 5. Control Register Bits

Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I²C device know that the Input Port register will be accessed next.

Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

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The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9534 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9534 registers and I^{2}C/SMBus state machine will initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Interrupt Output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. In a Stop event, $\overline{\text{INT}}$ is cleared after the rising edge of SDA. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and PCA9534 through write and read commands.

Writes

Data is transmitted to the PCA9534 by sending the device address and setting the least significant bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 6 and Figure 7). There is no limitation on the number of data bytes sent in one write transmission.
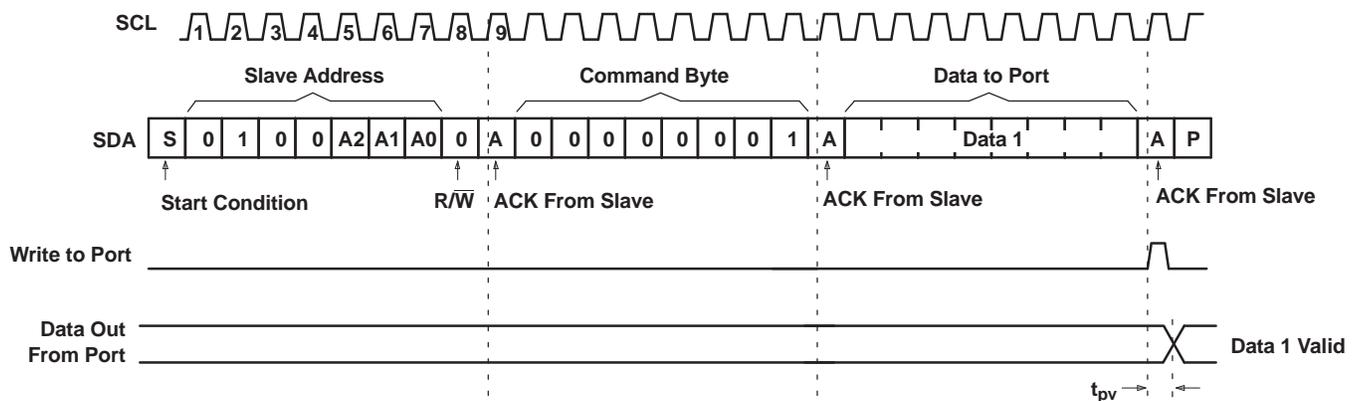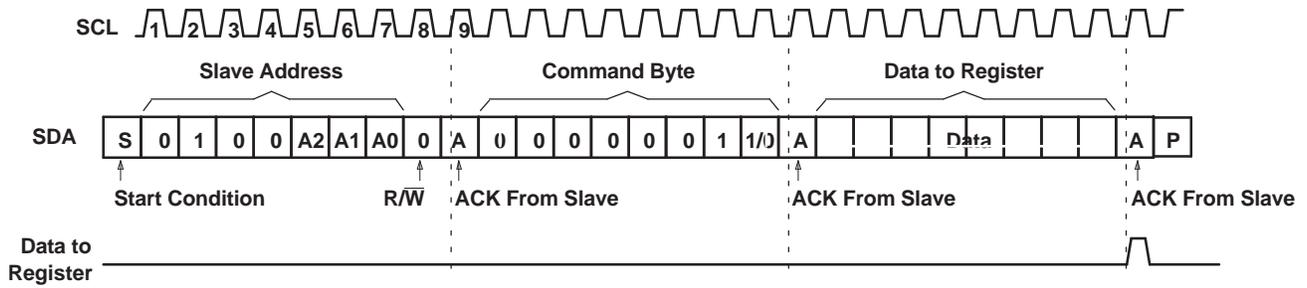

Figure 6. Write to Output Port Register

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Figure 7. Write to Configuration or Polarity Inversion Registers

Reads

The bus master first must send the PCA9534 address with the LSB set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9534 (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.
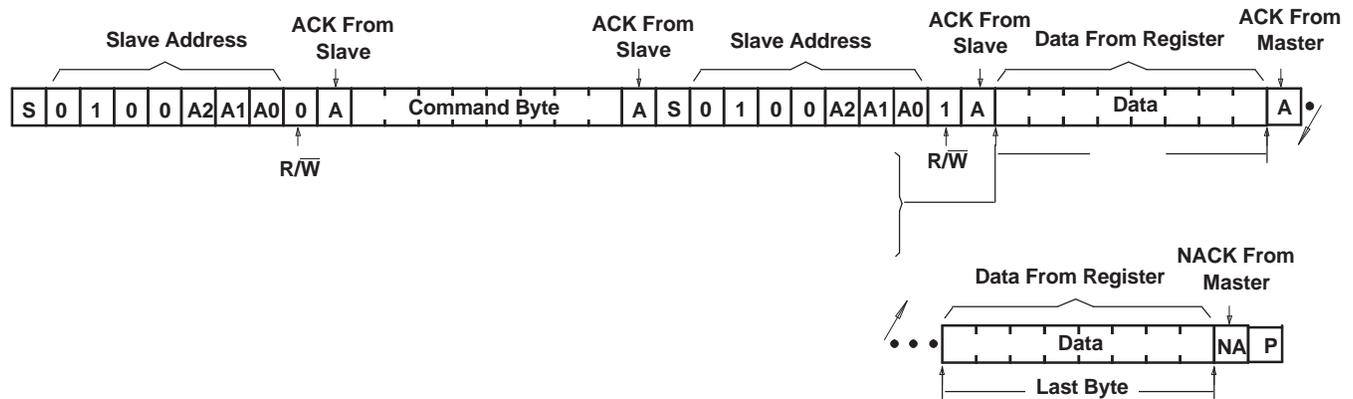
Figure 8. Read From Register

Figure 9. Read Input Port Register
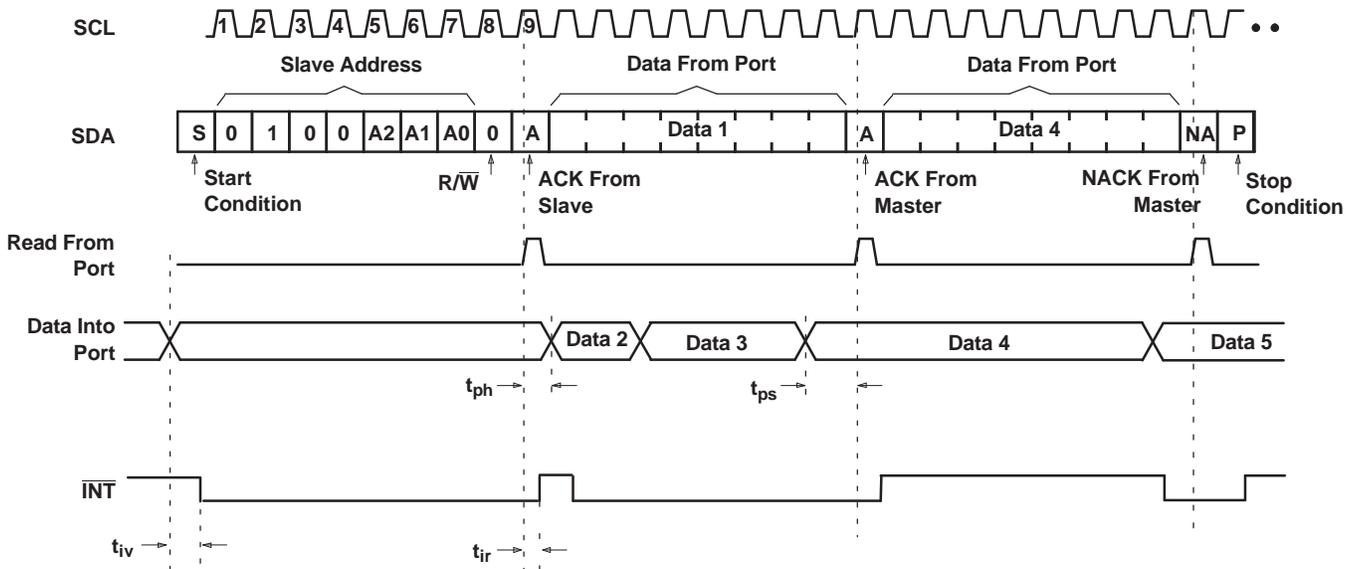
A. This figure assumes that the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and the actual data transfer from the P Port. See Figure 8 for these details.

Product Folder Link(s): *PCA9534*

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range[2]		−0.5	6	V
V_O	Output voltage range[2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance[3]	DB package		82	°C/W
		DBQ package		90	
		DGV package		86	
		DW package		46	
		PW package		88	
		RGT package		TBD	
		RGV package		51	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A0, A1, A2, P7–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A0, A1, A2, P7–P0	−0.5	0.8	
I_{OH}	High-level output current	P7–P0		−10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		−40	85	°C

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Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	8		mA
	P port[3]	$V_{OL} = 0.5$ V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		$V_{OL} = 0.7$ V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	INT	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A0, A1, A2					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	$V_I =$ GND	2.3 V to 5.5 V			−1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{scl} = 400$ kHz	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{scl} = 100$ kHz	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	$V_I =$ GND, $I_O = 0$, I/O = inputs, $f_{scl} = 0$ kHz	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		All LED I/Os at $V_I = 4.3$ V, $f_{scl} = 0$ kHz	5.5 V			1	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P0) must be limited to a maximum current of 200 mA.

Product Folder Link(s): *PCA9534*

I^{2}C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 10)

			STANDARD MODE I^{2}C BUS		FAST MODE I^{2}C BUS		UNIT
			MIN	MAX	MIN	MAX	
t_{scl}	I^{2}C clock frequency		0	100	0	400	kHz
t_{sch}	I^{2}C clock high time		4		0.6		µs
t_{scl}	I^{2}C clock low time		4.7		1.3		µs
t_{sp}	I^{2}C spike time			50		50	ns
t_{sds}	I^{2}C serial-data setup time		250		100		ns
t_{sdh}	I^{2}C serial-data hold time		0		0		ns
t_{icr}	I^{2}C input rise time			1000	$20 + 0.1C_b$ [1]	300	ns
t_{icf}	I^{2}C input fall time			300	$20 + 0.1C_b$ [1]	300	ns
t_{ocf}	I^{2}C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ [1]	300	ns
t_{buf}	I^{2}C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I^{2}C Start or repeated Start condition setup		4.7		0.6		µs
t_{sth}	I^{2}C Start or repeated Start condition hold		4		0.6		µs
t_{sps}	I^{2}C Stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I^{2}C bus capacitive load			400		400	ns

(1) C_b = total capacitive of one bus in pF

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 11 and Figure 12)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I^{2}C BUS		FAST MODE I^{2}C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	INT		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	INT		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		200		200	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
TEMPERATURE

V_{CC} = 5 V

f_{SCL} = 400 kHz
I/Os unloaded

V_{CC} = 3.3 V

V_{CC} = 2.5 V

I_{CC} – Supply Current – µA

T_A – Free-Air Temperature – °C
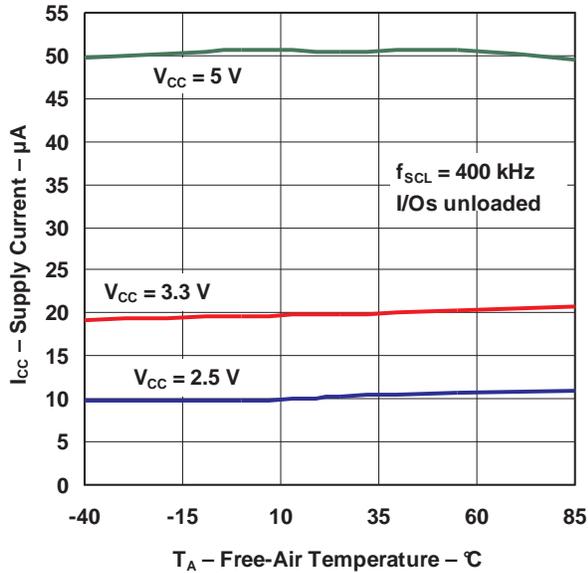
QUIESCENT SUPPLY CURRENT
vs
TEMPERATURE

V_{CC} = 5 V

V_{CC} = 3.3 V

V_{CC} = 2.5 V

SCL = V_{CC}

I_{CC} – Supply Current – nA

T_A – Free-Air Temperature – °C
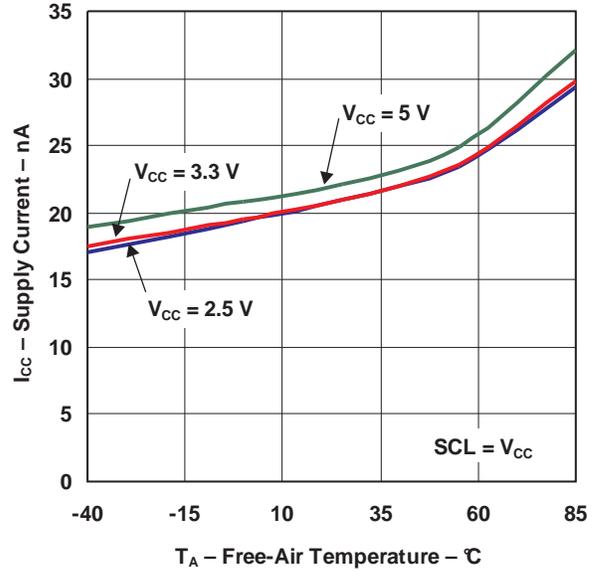
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

f_{SCL} = 400 kHz
I/Os unloaded

I_{CC} – Supply Current – µA

V_{CC} – Supply Voltage – V
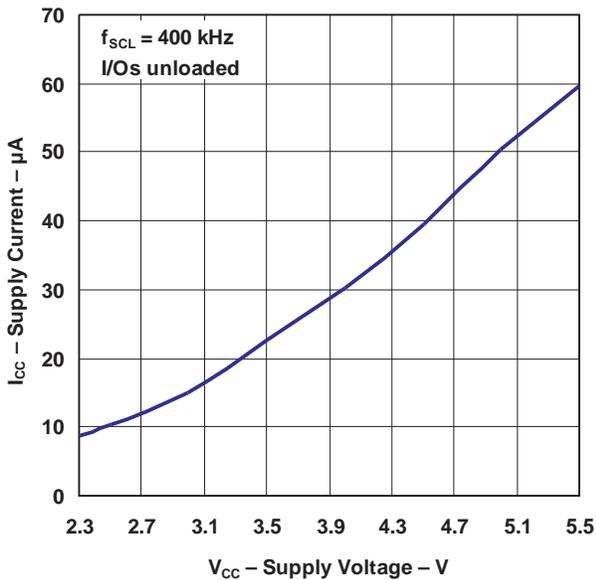
SUPPLY CURRENT
vs
NUMBER OF I/Os HELD LOW

V_{CC} = 5 V

T_A = −40°C

T_A = 25°C

T_A = 85°C

I_{CC} – Supply Current – µA

Number of I/Os Held Low

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Product Folder Link(s): *PCA9534*

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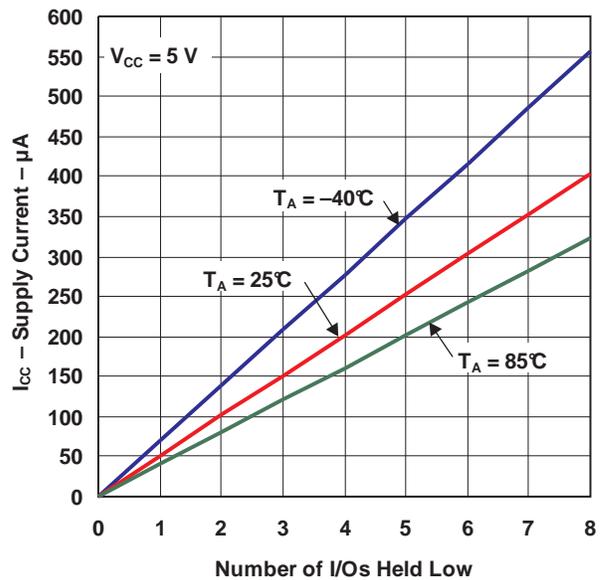
TYPICAL CHARACTERISTICS (continued)

I/O OUTPUT LOW VOLTAGE
vs
TEMPERATURE
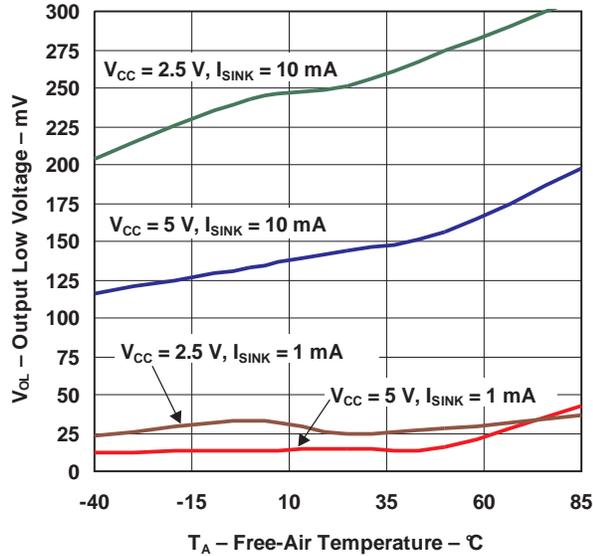
I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE
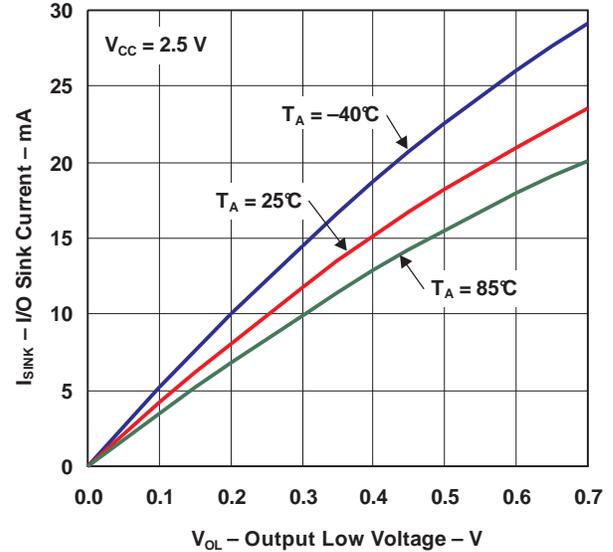
I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

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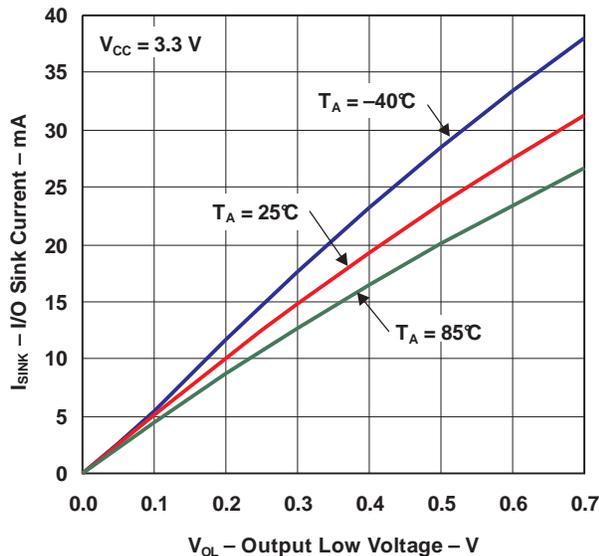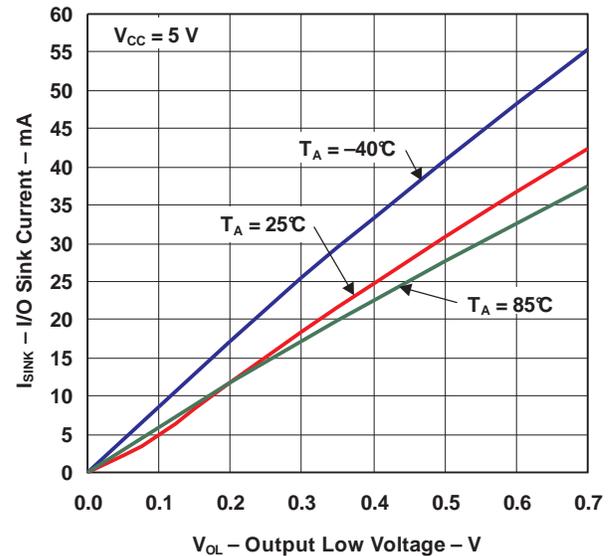
TYPICAL CHARACTERISTICS (continued)

I/O OUTPUT HIGH VOLTAGE
vs
TEMPERATURE
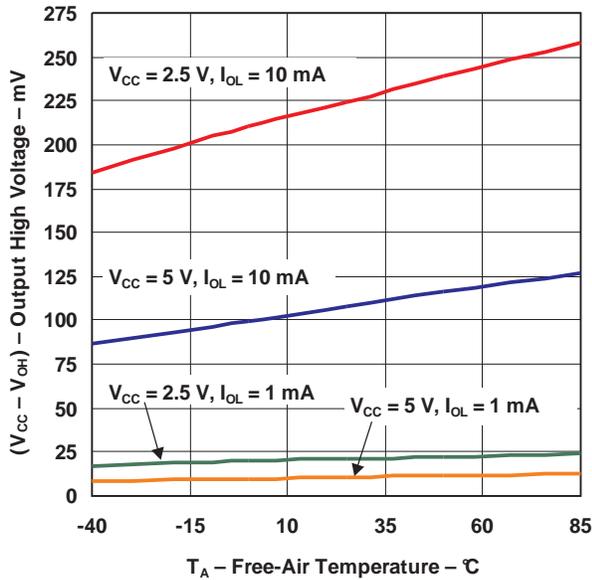
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE
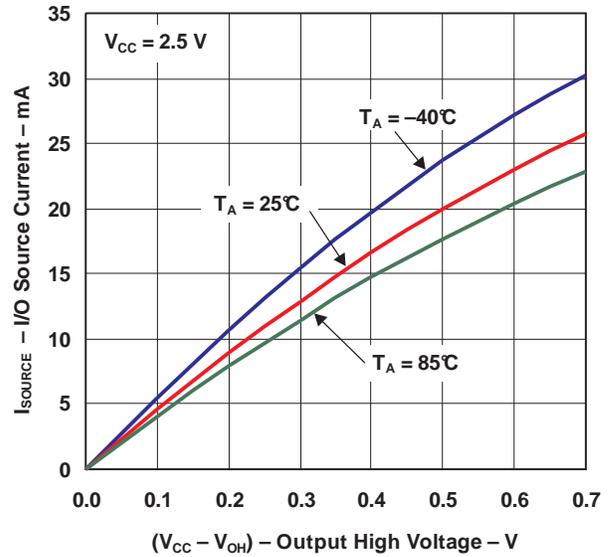
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

Product Folder Link(s): *PCA9534*
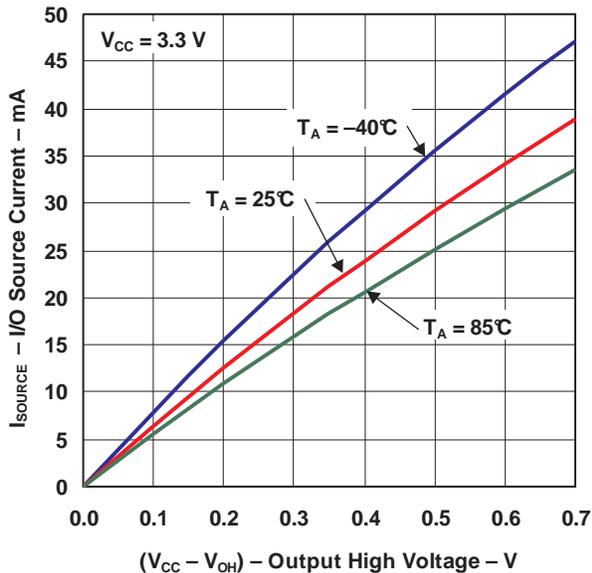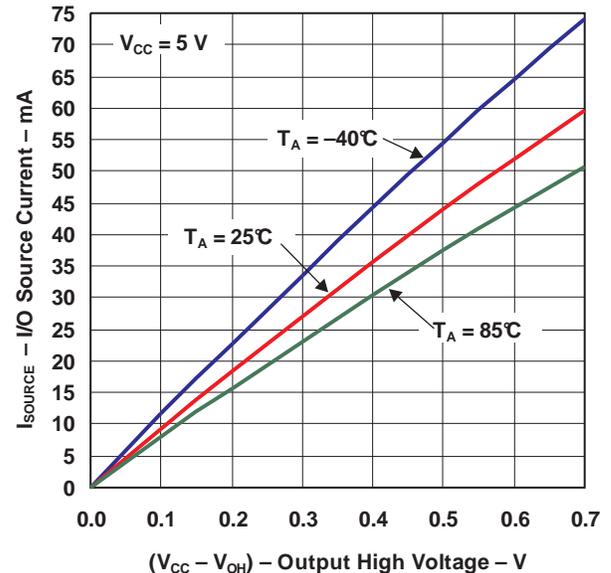
TYPICAL CHARACTERISTICS (continued)

OUTPUT HIGH VOLTAGE
vs
SUPPLY VOLTAGE

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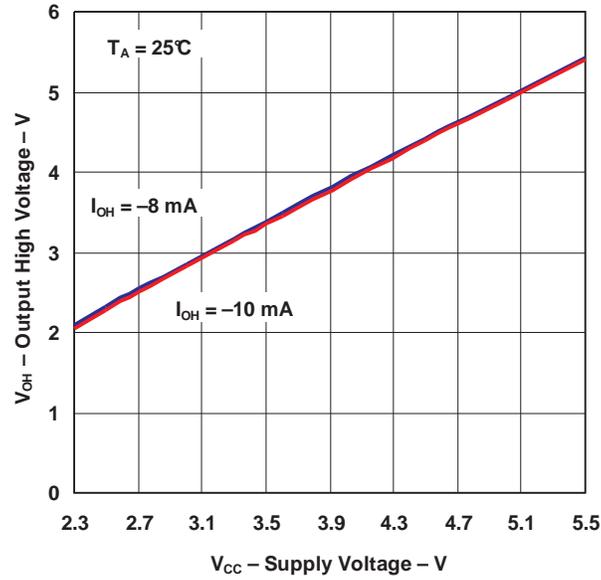
PARAMETER MEASUREMENT INFORMATION
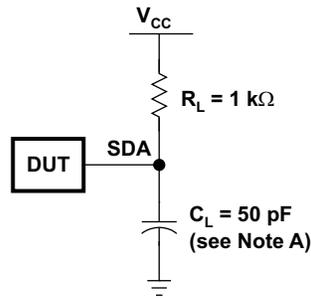
SDA LOAD CONFIGURATION
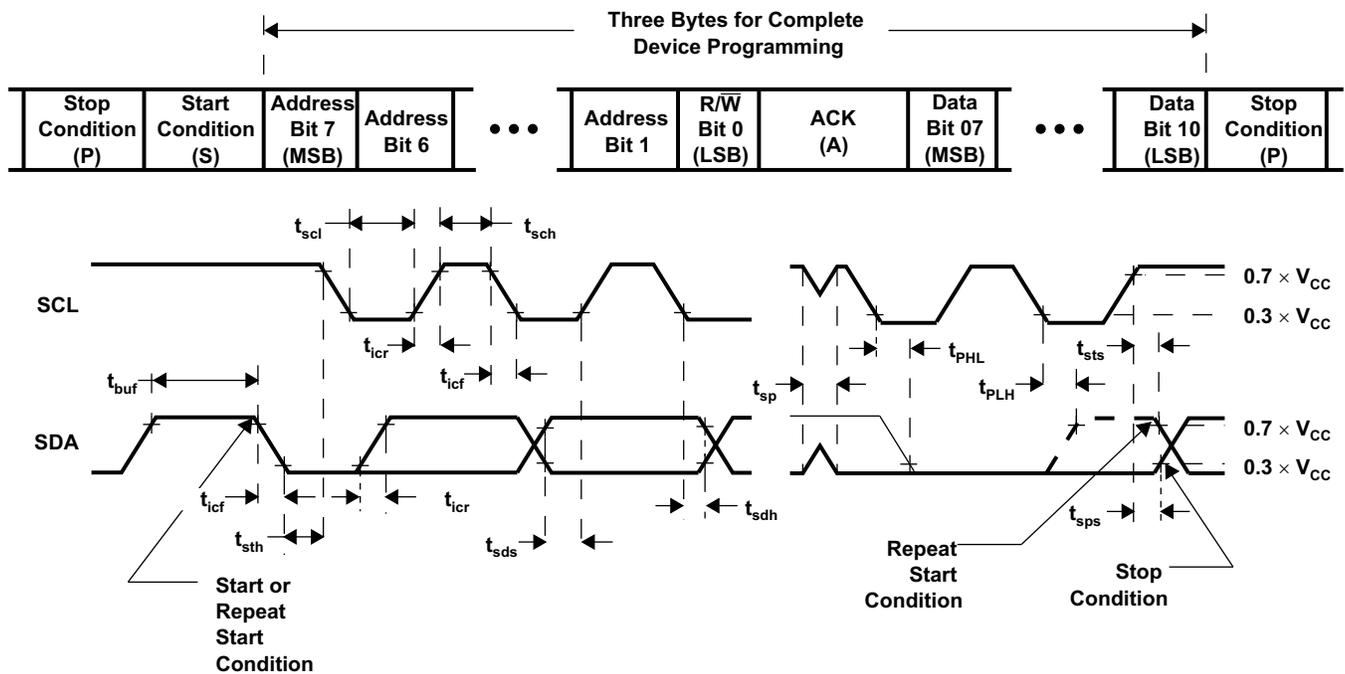
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 10. I²C Interface Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)

V_{CC}

$R_L = 4.7$ kΩ

DUT $\overline{INT}$

$C_L = 100$ pF
(see Note A)
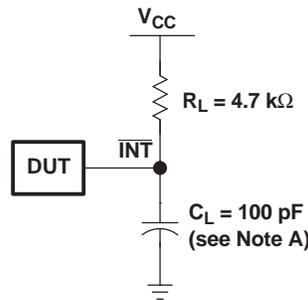
INTERRUPT LOAD CONFIGURATION
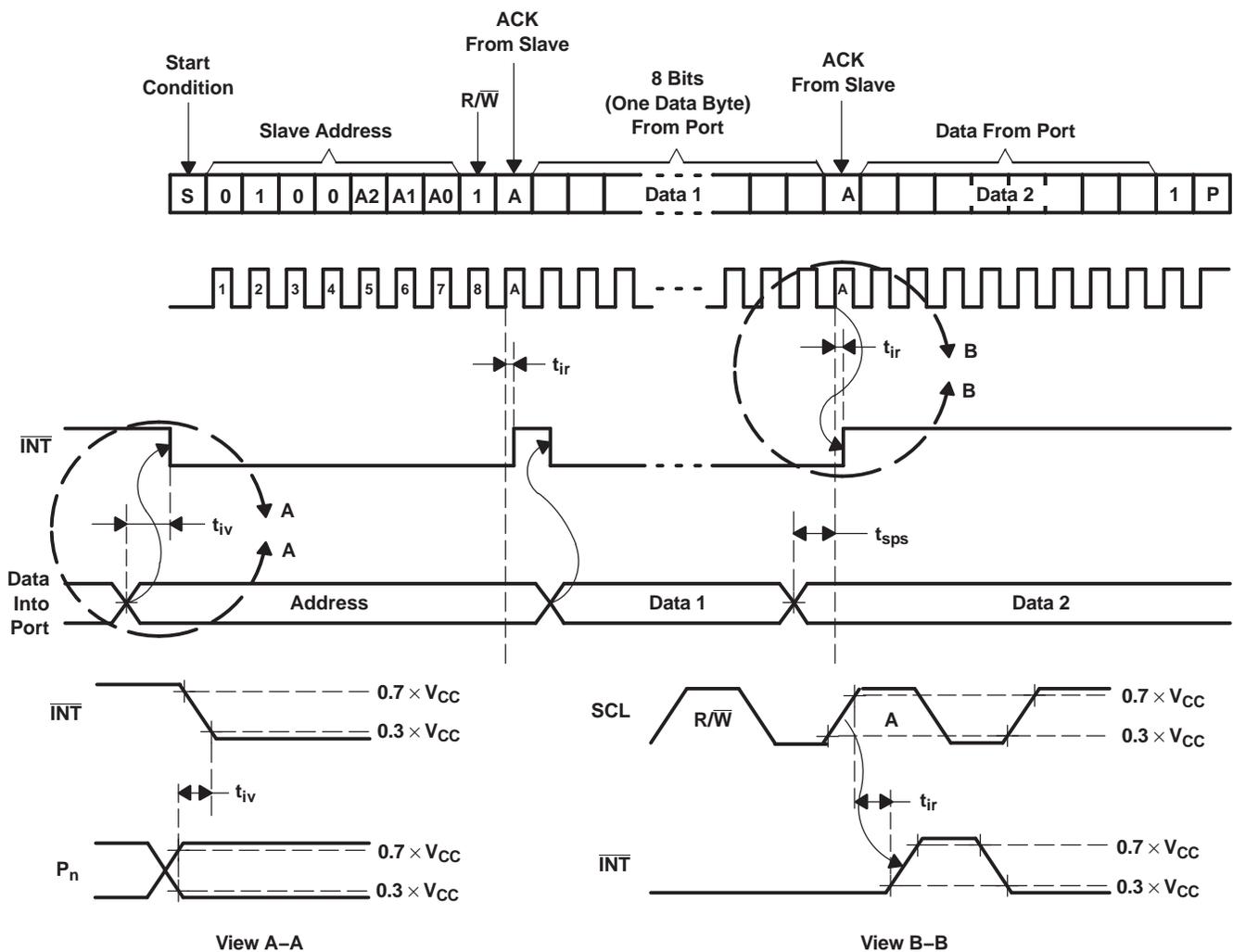
Start Condition

Slave Address

ACK From Slave

R/$\overline{W}$

8 Bits (One Data Byte) From Port

ACK From Slave

Data From Port

| S | 0 | 1 | 0 | 0 | A2 | A1 | A0 | 1 | A | | | | Data 1 | | | | A | | | | Data 2 | | | | 1 | P |

1 2 3 4 5 6 7 8 A

t_{ir}

B
B

$\overline{INT}$

t_{iv} A
A

t_{sps}

Data Into Port

Address   Data 1   Data 2

View A–A

$\overline{INT}$ $0.7 \times V_{CC}$ $0.3 \times V_{CC}$

t_{iv}

P_n $0.7 \times V_{CC}$ $0.3 \times V_{CC}$

View B–B

SCL   R/$\overline{W}$ A $0.7 \times V_{CC}$ $0.3 \times V_{CC}$

t_{ir}

$\overline{INT}$ $0.7 \times V_{CC}$ $0.3 \times V_{CC}$

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, $t_r/t_f ≤ 30$ ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 11. Interrupt Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)
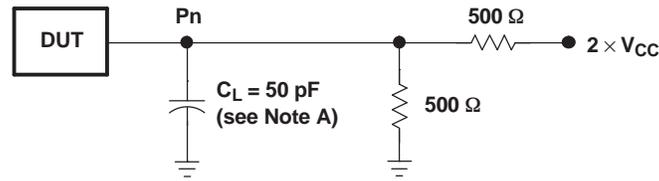
P-PORT LOAD CONFIGURATION
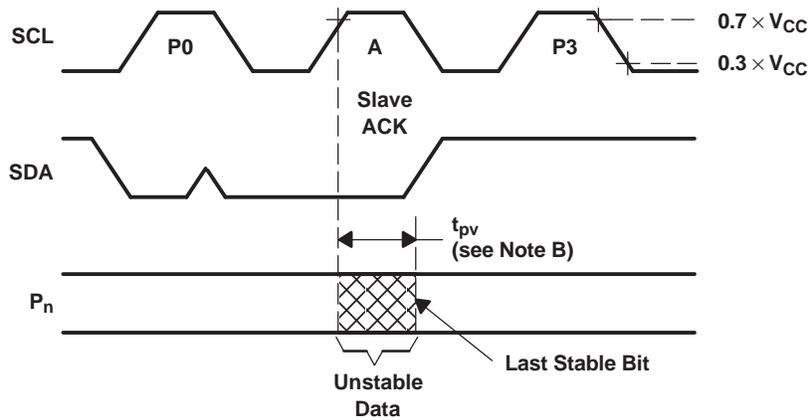
WRITE MODE (R/$\overline{\text{W}}$ = 0)
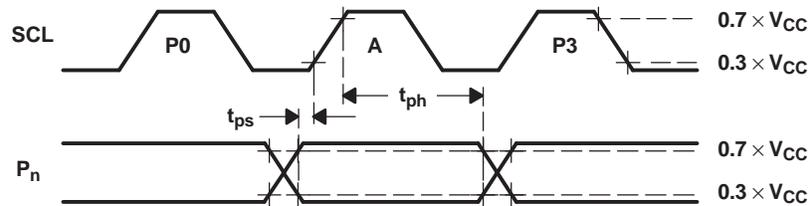
READ MODE (R/$\overline{\text{W}}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 12. P-Port Load Circuit and Voltage Waveforms
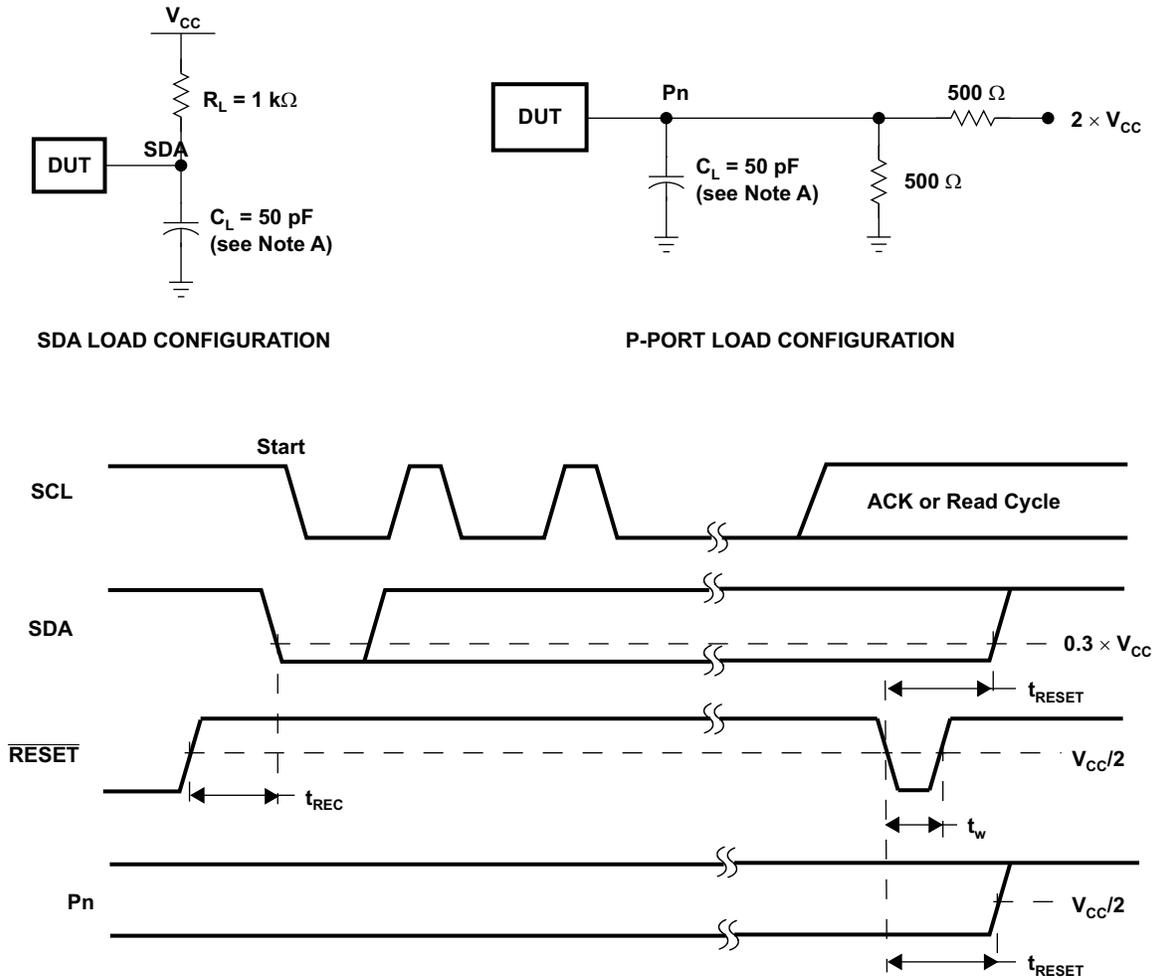
Product Folder Link(s): *PCA9534*

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PARAMETER MEASUREMENT INFORMATION (continued)

SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION

A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   I/Os are configured as inputs.

D.   All parameters and waveforms are not applicable to all devices.

Figure 13. Reset Load Circuits and Voltage Waveforms

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APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9534 can be used.
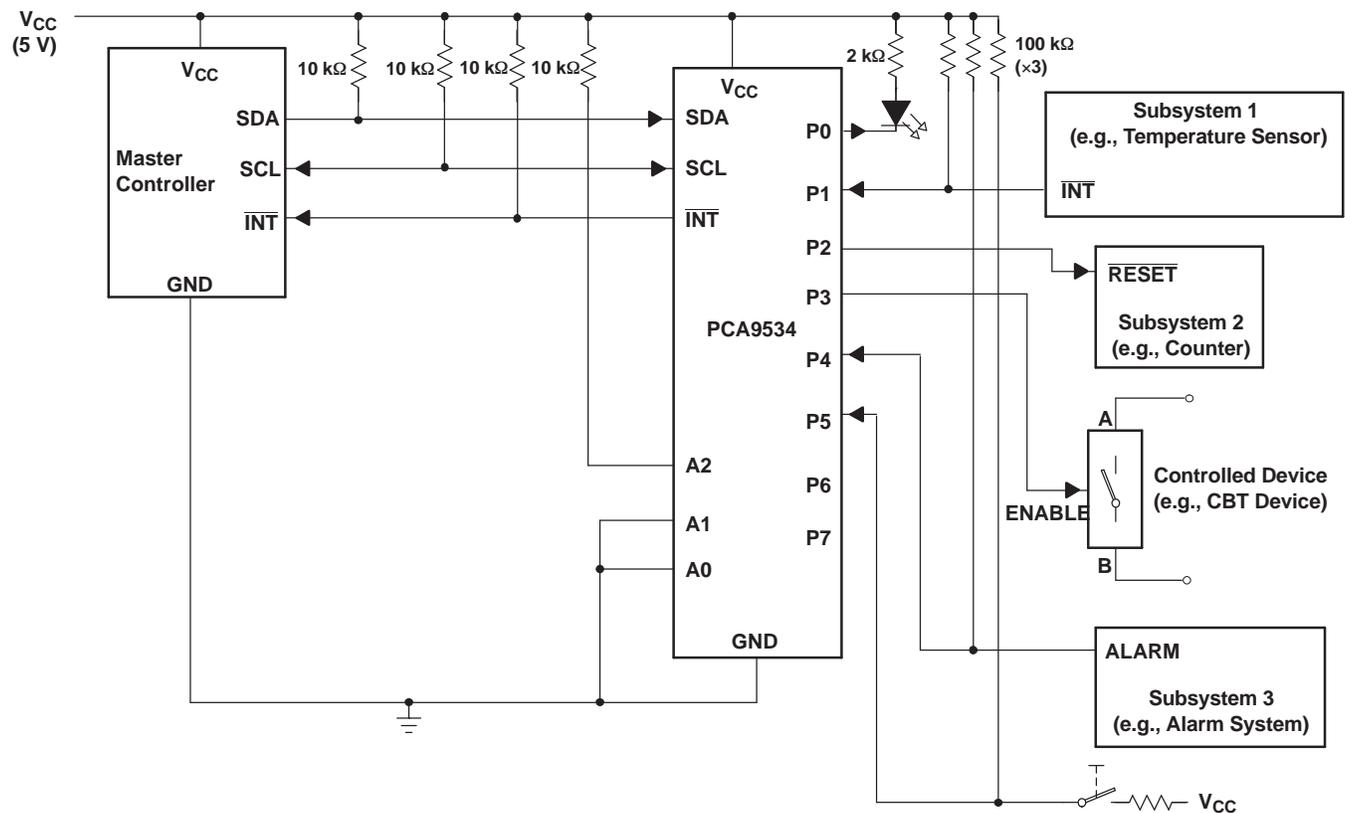
A. Device address is configured as 0100100 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and must be configured as outputs.

Figure 14. Typical Application

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Minimizing I_{CC} When the I/O Controls LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor, as shown in Figure 14. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of the I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.
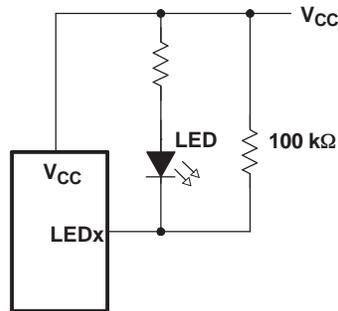
Figure 15. High-Value Resistor in Parallel With the LED
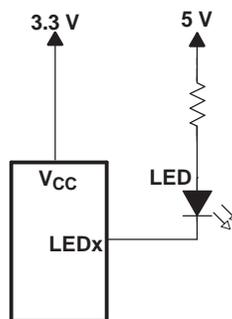
Figure 16. Device Supplied by a Lower Voltage

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCA9534DB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DBQR	PREVIEW	SSOP/QSOP	DBQ	16	2500	TBD	Call TI	Call TI
PCA9534DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9534RGTR	PREVIEW	QFN	RGT	16	3000	TBD	Call TI	Call TI
PCA9534RGVR	ACTIVE	QFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9534RGVRG4	ACTIVE	QFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS
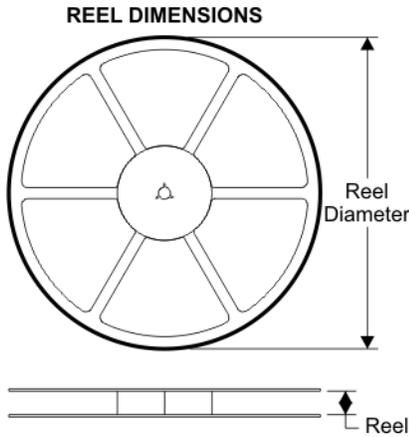
compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL BOX DIMENSIONS
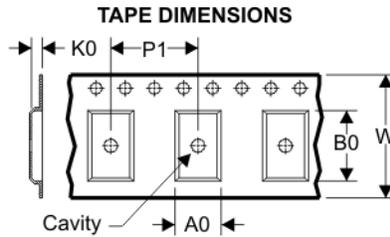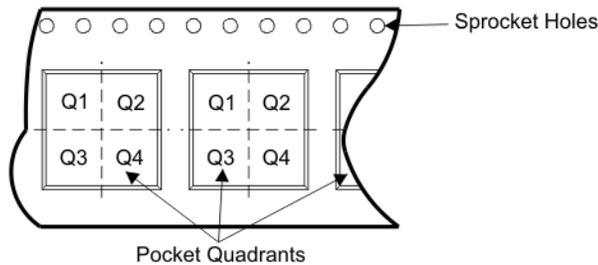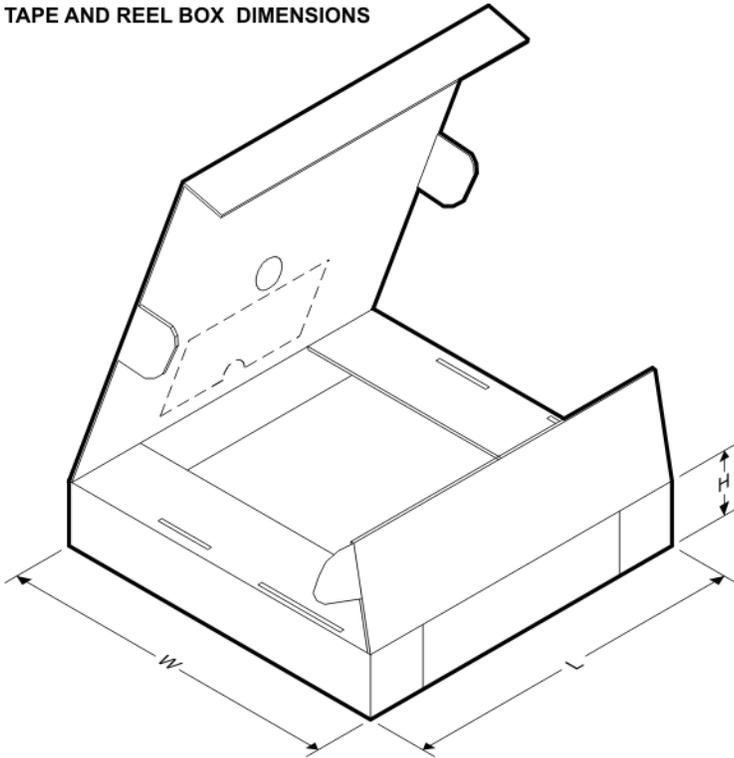
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
PCA9534DBR	DB	16	SITE 41	346.0	346.0	33.0
PCA9534DGVR	DGV	16	SITE 41	346.0	346.0	29.0
PCA9534DWR	DW	16	SITE 60	346.0	346.0	33.0
PCA9534PWR	PW	16	SITE 41	346.0	346.0	29.0
PCA9534RGVR	RGV	16	SITE 41	346.0	346.0	29.0

DGV (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20
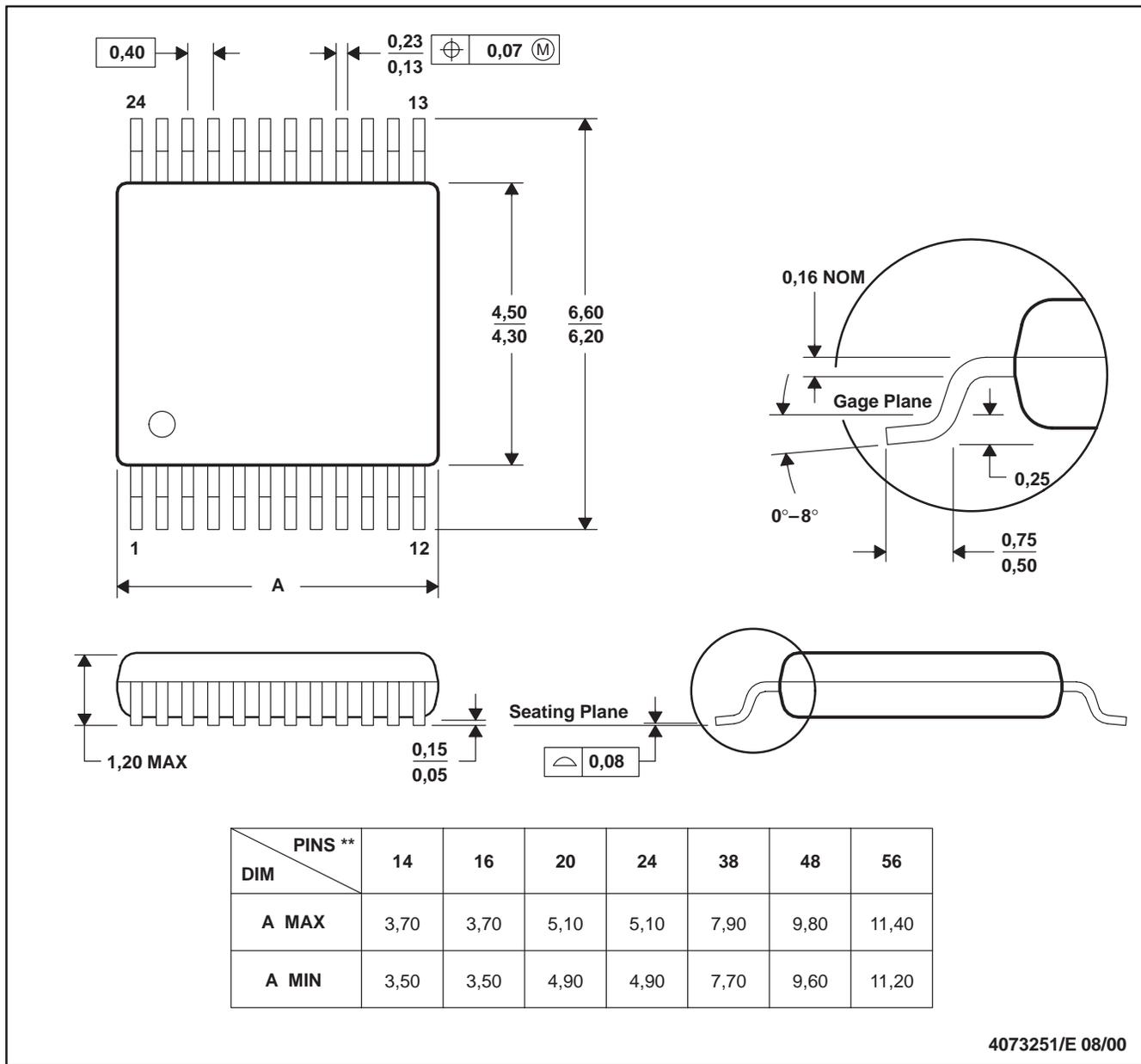
4073251/E 08/00
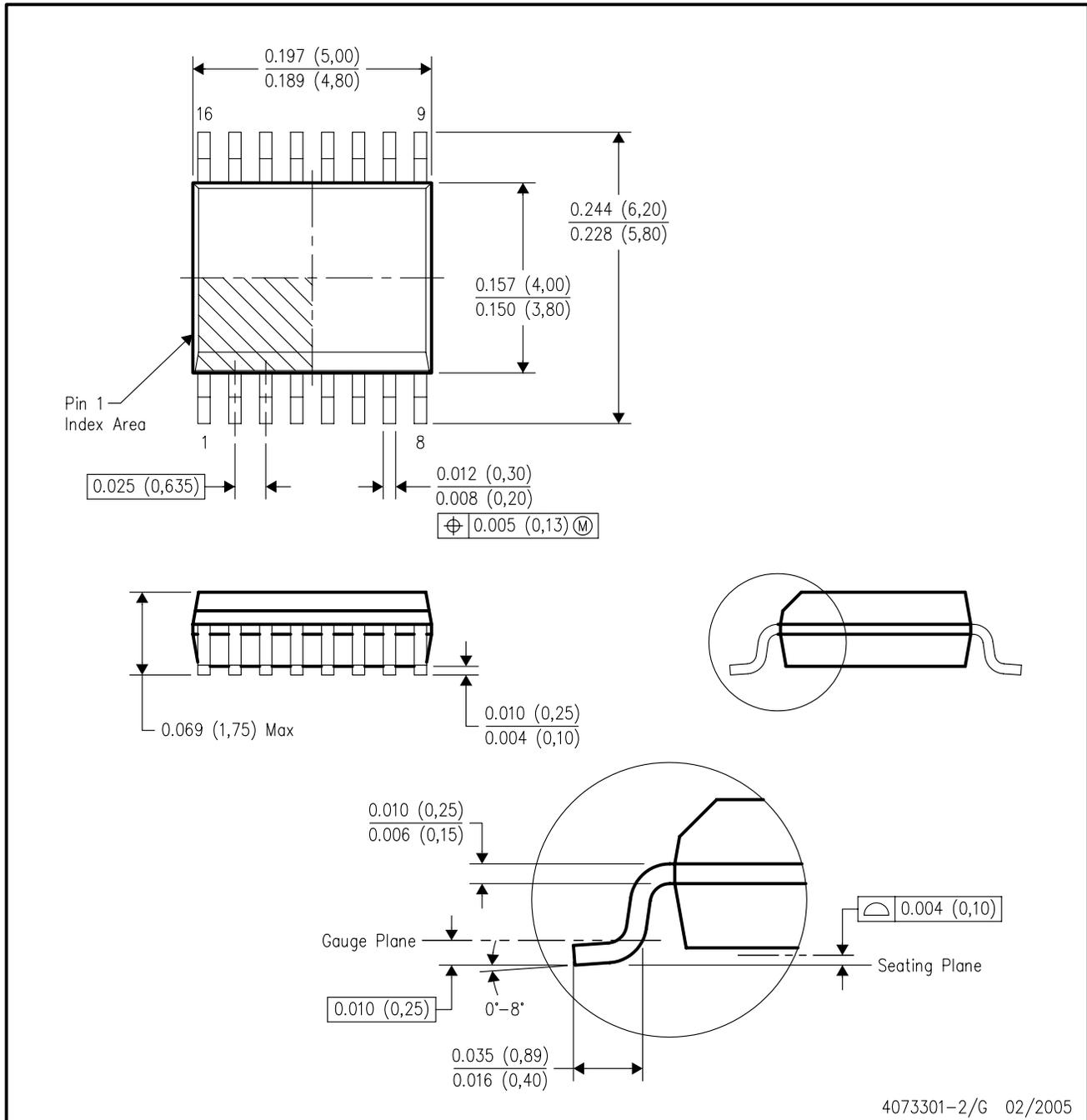
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

RGT (S−PQFP−N16) PLASTIC QUAD FLATPACK

$\frac{3,15}{2,85}$

$\frac{3,15}{2,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

⌴ 0,08

$\frac{0,05}{0,00}$

16X $\frac{0,50}{0,30}$

1   4

16   5

13   8

12   9

EXPOSED THERMAL PAD

/D\

16X $\frac{0,30}{0,18}$ ⊕ 0,10 Ⓜ

0,50

1,50
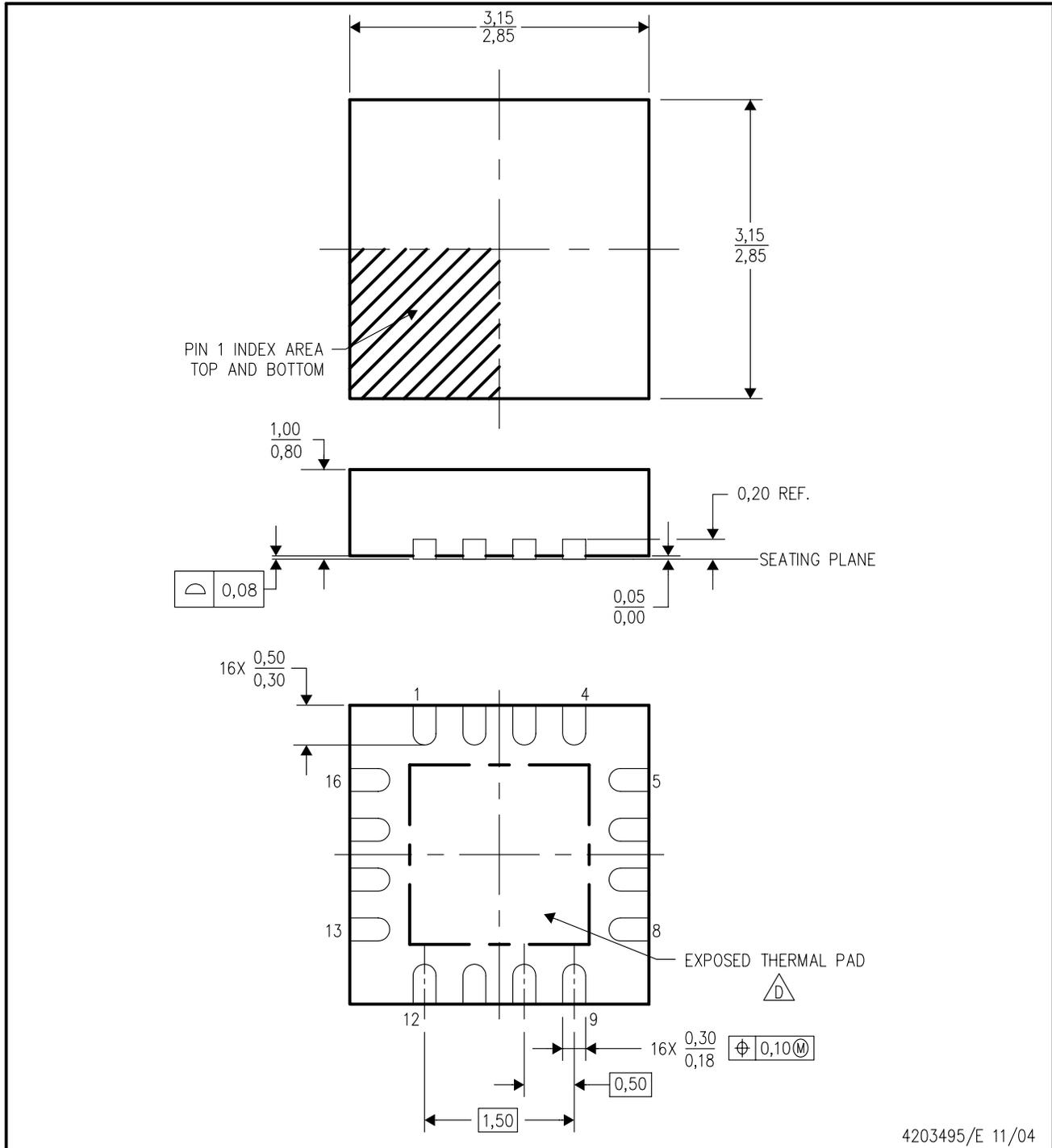
4203495/E 11/04

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
   /D\   The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−220.

RGV (S−PQFP−N16)   PLASTIC QUAD FLATPACK

4,15
3,85

4,15
3,85

PIN 1 INDEX AREA
TOP AND BOTTOM

1,00
0,80

0,20 REF.

SEATING PLANE

△ 0,08

0,05
0,00

16X 0,65
0,45

0,65

1   4

16   5

13   8

EXPOSED THERMAL PAD
⚠ D

12   9

16X 0,38
0,23

1,95

⊕ ⌀ 0,10 Ⓜ
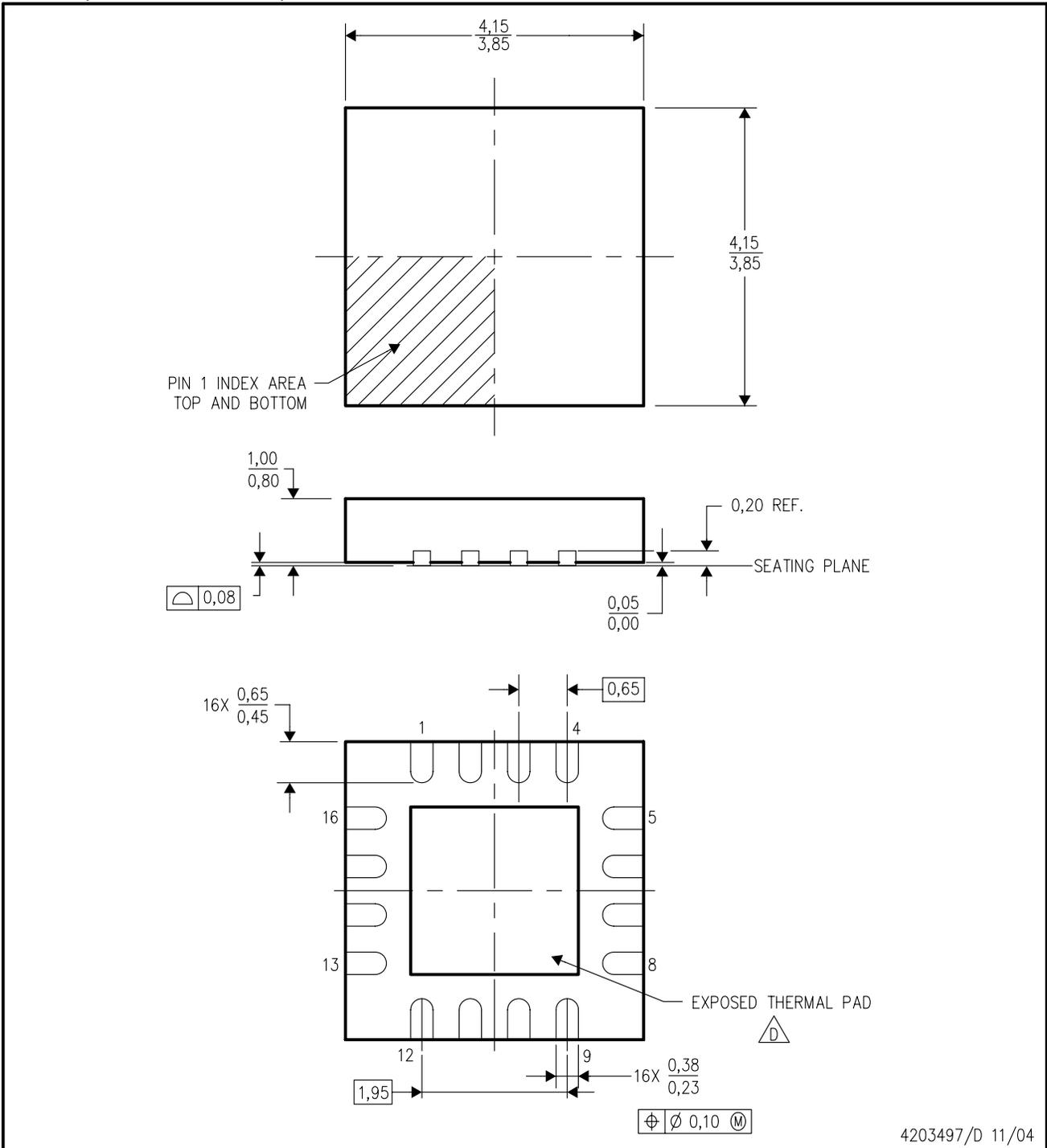
4203497/D 11/04

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
      ⚠   The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Pin 1 indicator is electrically tied
to the exposed thermal pad
Pin 1 indicator metal feature may
not be present on some devices

0,18±0,05 (2 Places)

0,35±0,05 (2 Places)

Exposed Thermal Pad

2,16±0,10

2,16±0,10
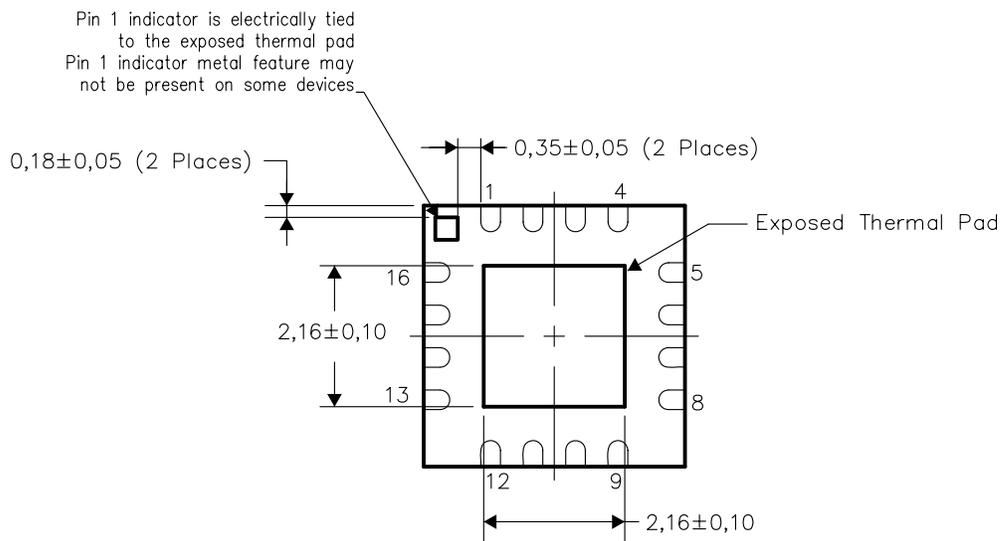
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGV (S−PQFP−N16)
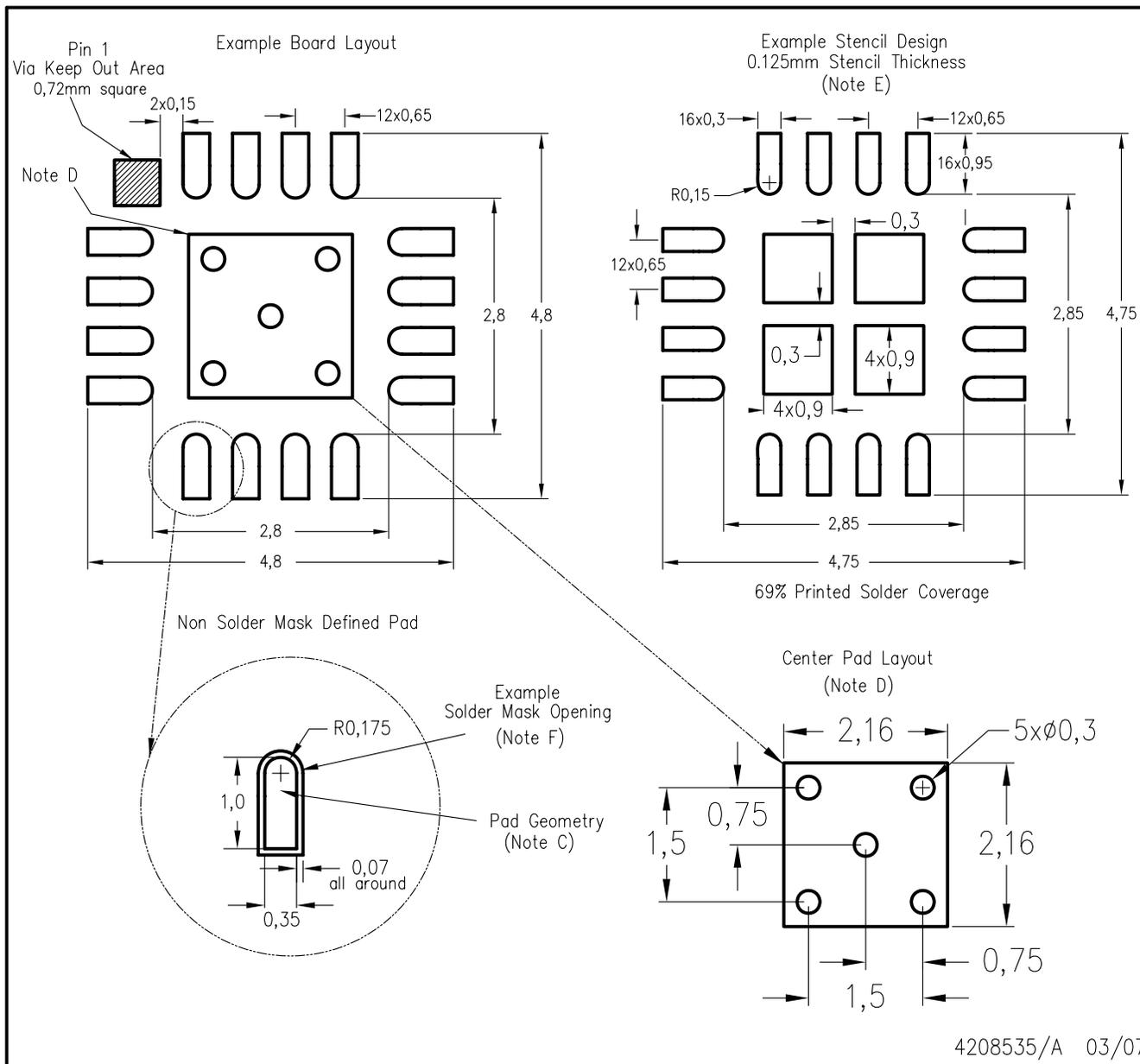
Example Board Layout

Pin 1
Via Keep Out Area
0,72mm square

2x0,15

12x0,65

Note D

2,8

4,8

2,8

4,8

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

R0,175

1,0

Pad Geometry
(Note C)

0,07
all around

0,35

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

16x0,3

12x0,65

16x0,95

R0,15

0,3

12x0,65

2,85   4,75

0,3   4x0,9

4x0,9

2,85

4,75

69% Printed Solder Coverage

Center Pad Layout
(Note D)

2,16

5xØ0,3

0,75

1,5

2,16

0,75

1,5

4208535/A   03/07

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN
            Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for solder mask tolerances.

DW (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
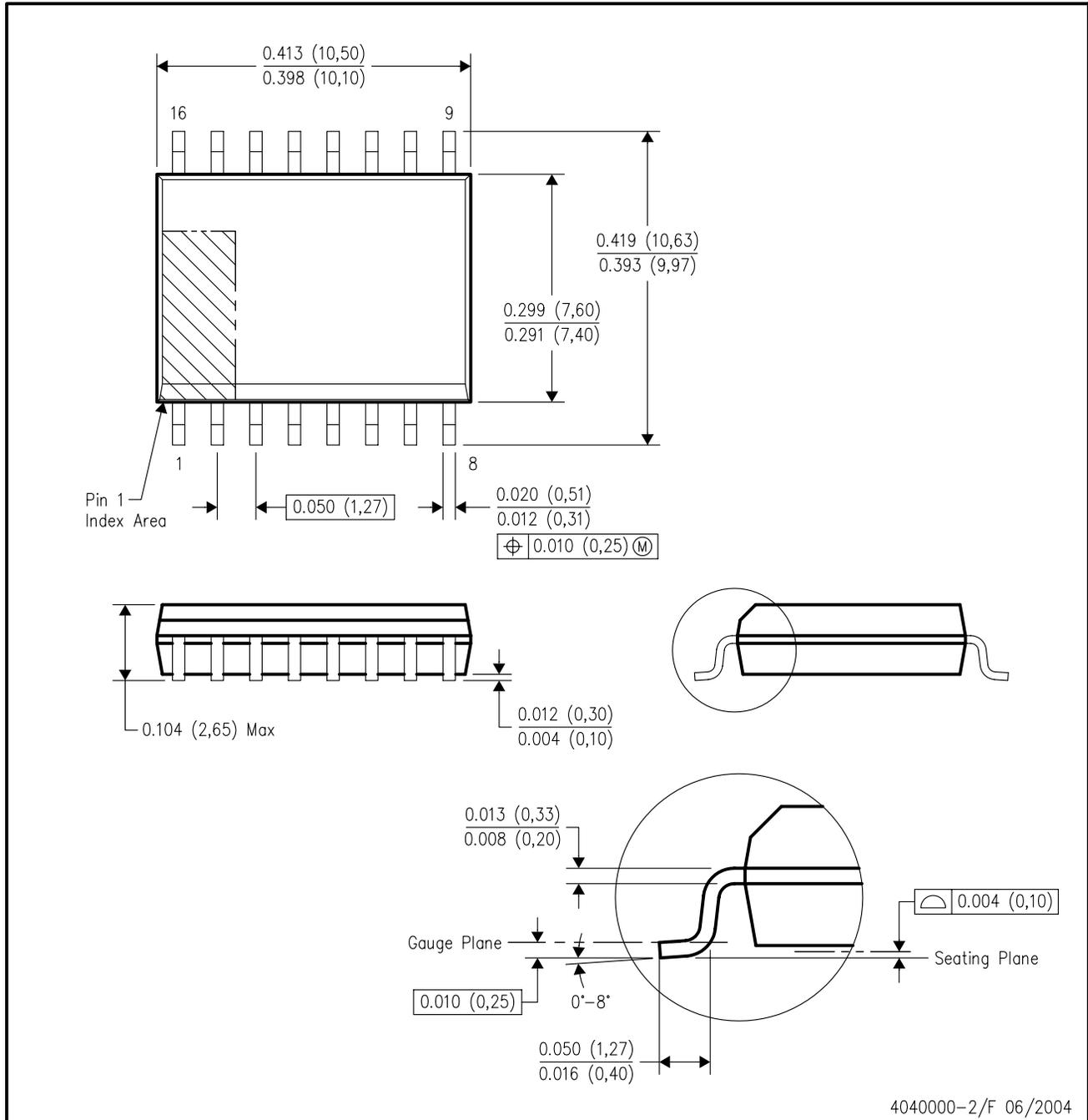
4040000−2/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AA.

DBQ (R−PDSO−G16)　　　　　PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)

16　　　　　　9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1　　　　　　8

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.006 (0,15)

⌒ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−2/G　02/2005

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
　　　　　D.　Falls within JEDEC MO−137 variation AB.

MECHANICAL DATA

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
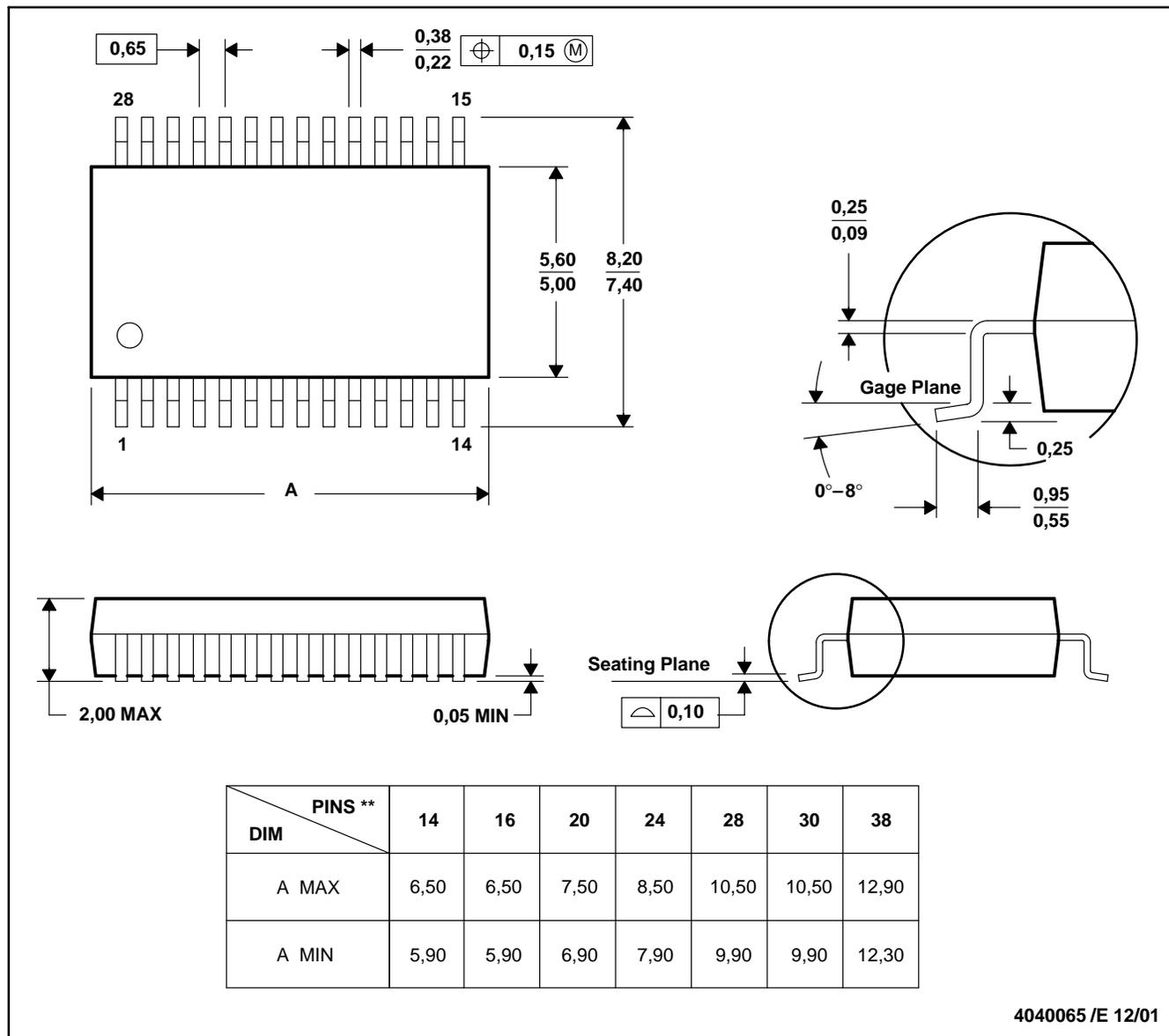
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

MECHANICAL DATA

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
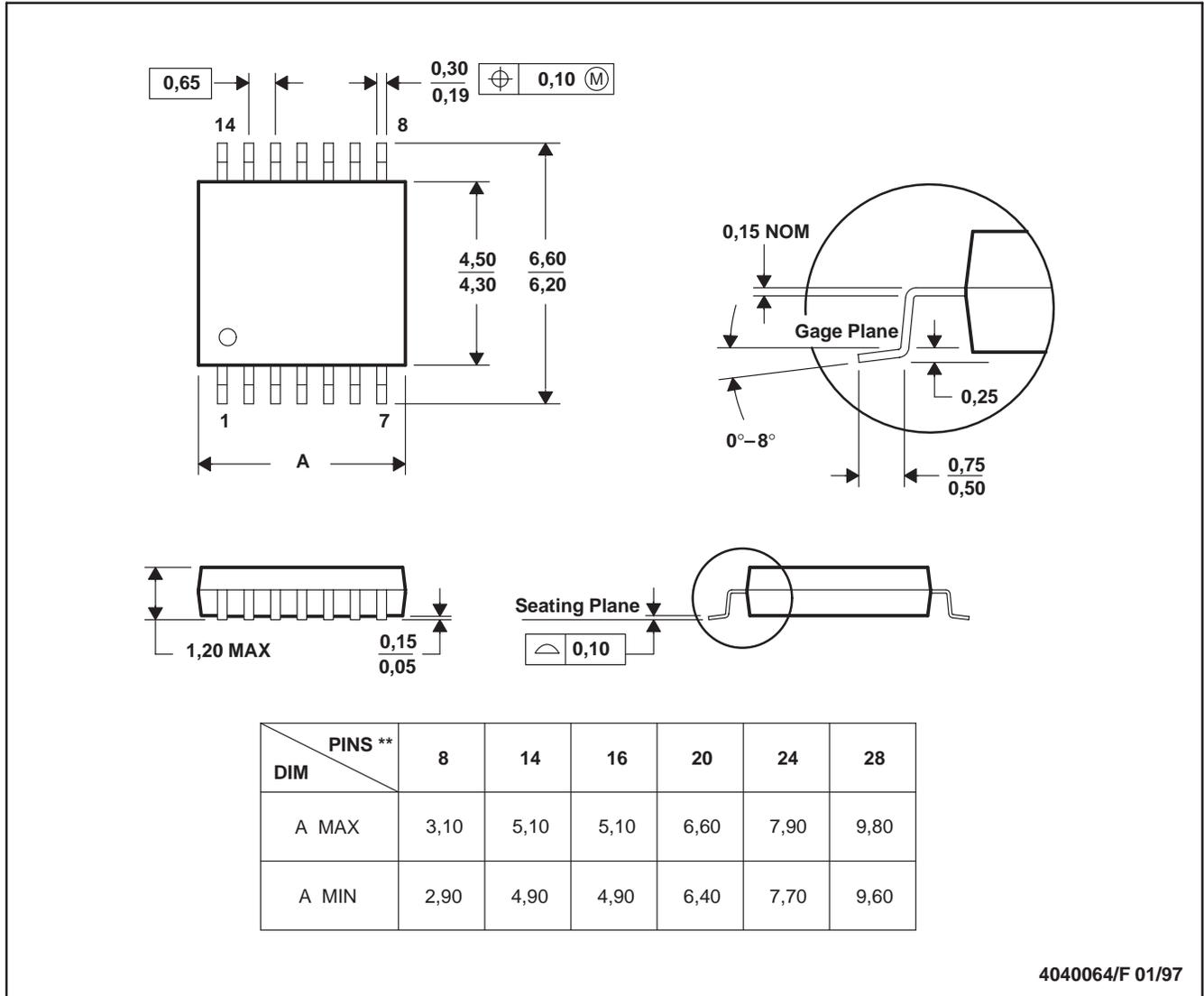
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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