



HM-65262

T-46-23-05

16K x 1 Asynchronous
CMOS Static RAM

January 1992

Features

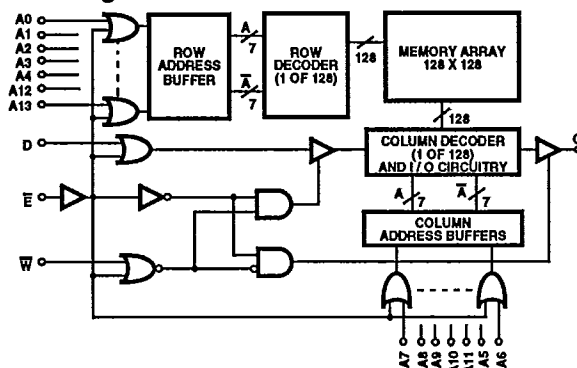
- Fast Access Time70/85ns Max
- Low Standby Current50µA Max
- Low Operating Current50mA Max
- Data Retention at 2.0 Volts20µA Max
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout
- No Clocks or Strobes Required
- Temperature Range+55°C to +125°C
- Equal Cycle and Access Time
- Single 5 Volt Supply
- Gated Inputs-No Pull-Up or Pull-Down Resistors Required

Description

The HM-65262 is a CMOS 16384 x 1 bit Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262 is available in both JEDEC standard 20 pin, 0.300 inch wide DIP and 20 pad LCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

The HM-65262, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Functional Diagram



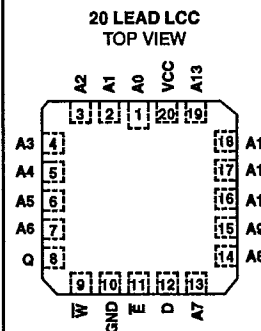
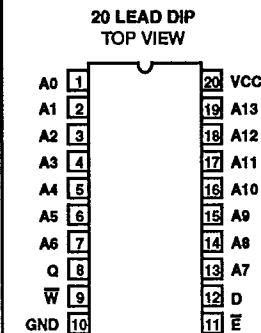
Ordering Information

PACKAGE	TEMP. RANGE	70ns/20µA*	*85ns/20µA*	*85ns/400µA*	
Ceramic DIP /883**	-40°C to +85°C	HM1-65262B-9	HM1-65262-9	HM1-65262C-9	
	-55°C to +125°C	HM1-65262B/883	HM1-65262/883	-	
		JAN #	29109BRA	29103BRA	-
		SMD#	8413203RA	8413201RA	-
LCC	-40°C to +85°C	HM4-65262B-9	HM4-65262-9	HM4-65262C-9	
	-55°C to +125°C	HM4-65262B/883	HM4-65262/883	-	
		JAN #	29109BYA	29103BYA	-
		SMD#	8413203YA	8413201YA	-

* Access Time/Data Retention Supply Current

** Respective /883 specifications are included at the end of this data sheet.

Pinouts



A0 - A13	Address Input
\bar{E}	Chip Enable/ Power Down
Q	Data Out
D	Data In
VSS/ GND	Ground
VCC	Power (+5)
\bar{W}	Write Enable

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CMOS MEMORY

Specifications HM-65262

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Absolute Maximum Ratings

Supply Voltage	+7.0V
Input or Output Voltage Applied for all grades	-0.3V to VCC+0.3V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	+300°C
Typical Derating Factor	.5mA/MHz Increase in ICCOP
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	66°C/W	13°C/W
Ceramic LCC Package	85°C/W	40°C/W
Maximum Package Power Dissipation at +125°C		
Ceramic DIP Package	0.75W	
Gate Count	26256 Gates	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V	Operating Temperature Range	HM-65262B-9, HM-65262-9, HM-65262C-9 -40°C to +85°C
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DC Electrical Specifications VCC = 5V ± 10%; T_A = -40°C to +85°C (HM-65262B-9, HM-65262-9, HM-65262C-9)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
ICCSB1	Standby Supply Current	-	50	μA	HM-65262B-9, HM-65262-9, IO = 0mA, \bar{E} = VCC - 0.3V, VCC = 5.5V
		-	900	μA	HM-65262C-9, IO = 0mA, \bar{E} = VCC - 0.3V, VCC = 5.5V
ICCSB	Standby Supply Current	-	5	mA	\bar{E} = 2.2V, IO = 0mA, VCC = 5.5V
ICCEN	Enabled Supply Current	-	50	mA	\bar{E} = 0.8V, IO = 0mA, VCC = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	50	mA	\bar{E} = 0.8V, IO = 0mA, f = 1MHz, VCC = 5.5V
ICCDR	Data Retention Supply Current	-	20	μA	HM-65262B-9, HM-65262-9, VCC = 2.0V, \bar{E} = VCC
		-	400	μA	HM-65262C-9, VCC = 2.0V, \bar{E} = VCC
ICCDR1	Data Retention Supply Current	-	30	μA	HM-65262B-9, HM-65262-9, VCC = 3.0V, \bar{E} = VCC
		-	550	μA	HM-65262C-9, VCC = 3.0V, \bar{E} = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND, VCC = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND, VCC = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 4.5V
VIH	Input High Voltage	2.2	VCC+0.3	V	VCC = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 8.0mA, VCC = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -4.0mA, VCC = 4.5V
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100μA, VCC = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	12	pF	

- NOTES: 1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

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AC Electrical Specifications VCC = 5V 10%, TA = -40°C to +85°C (HM-65262B-9, HM-65262-9, HM-65262C-9)

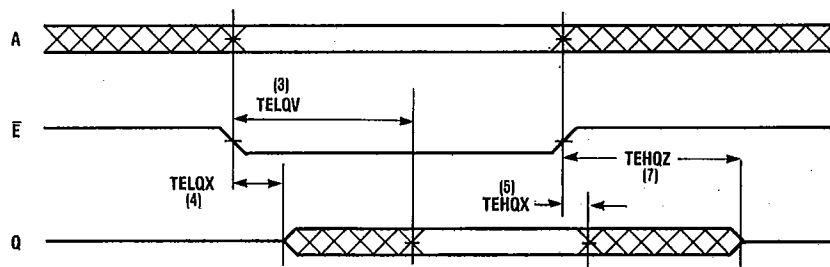
SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		HM-65262B-9		HM-65262-9		HM-65262C-9			
		MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE									
(1) TAVAX	Read/Cycle Time	70	-	85	-	85	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	70	-	85	-	85	ns	(Notes 1, 3)
(3) TELQV	Chip Enable Access Time	-	70	-	85	-	85	ns	(Notes 1, 3)
(4) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(5) TEHQX	Chip Disable Output Hold Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(6) TAXQX	Address Invalid Output Hold Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(7) TEHQZ	Chip Enable Output Disable Time	-	30	-	30	-	30	ns	(Notes 2, 3)
WRITE CYCLE									
(8) TAVAX	Write Cycle Time	70	-	85	-	85	-	ns	(Notes 1, 3)
(9) TELWH	Chip Selection to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(10) TWLWH	Write Enable Pulse Width	40	-	45	-	45	-	ns	(Notes 1, 3)
(11) TAVWL	Address Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(12) TWHAX	Address Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(13) TDVWH	Data Setup Time	30	-	35	-	35	-	ns	(Notes 1, 3)
(14) TWHDX	Data Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(15) TWLQZ	Write Enable Output Disable Time	-	30	-	30	-	30	ns	(Notes 2, 3)
(16) TWHQX	Write Disable Output Enable Time	0	-	0	-	0	-	ns	(Notes 2, 3)
(17) TAVWH	Address Valid to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(18) TAVEL	Address Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(19) TEHAX	Address Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(20) TAVEH	Address Valid to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(21) TELEH	Enable Pulse Width	55	-	65	-	65	-	ns	(Notes 1, 3)
(22) TWLEH	Write Enable Pulse Setup Time	40	-	45	-	45	-	ns	(Notes 1, 3)
(23) TDVEH	Chip Setup Time	30	-	35	-	35	0	ns	(Notes 1, 3)
(24) TEHDX	Data Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. VCC = 4.5 and 5.5V.

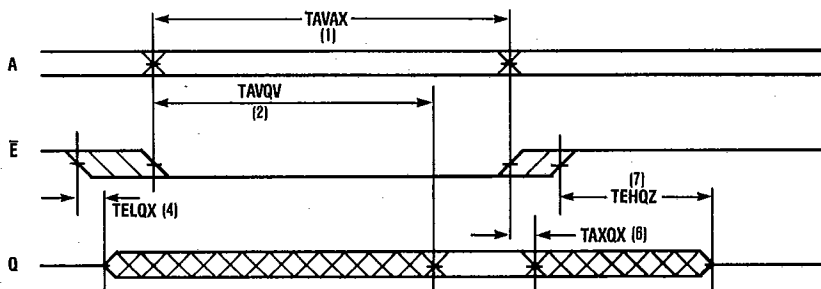
Timing Waveforms

READ CYCLE 1: CONTROLLED BY \bar{E}



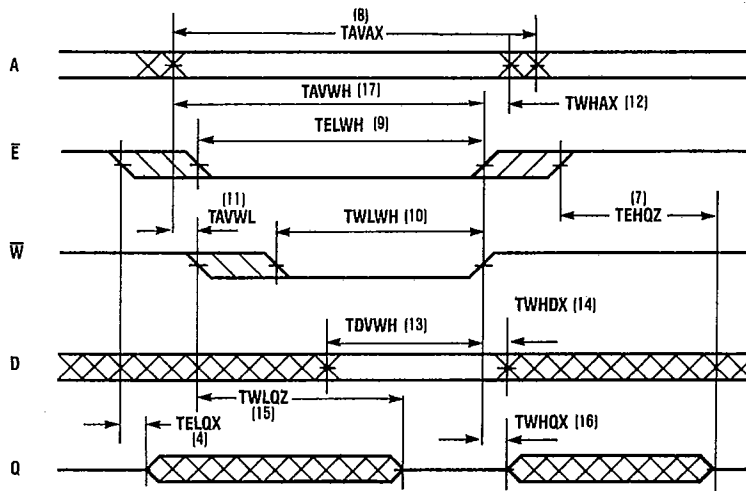
NOTE: \bar{W} is high for entire cycle and D is ignored. Address is stable by the time \bar{E} goes low and remains valid until \bar{E} goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS

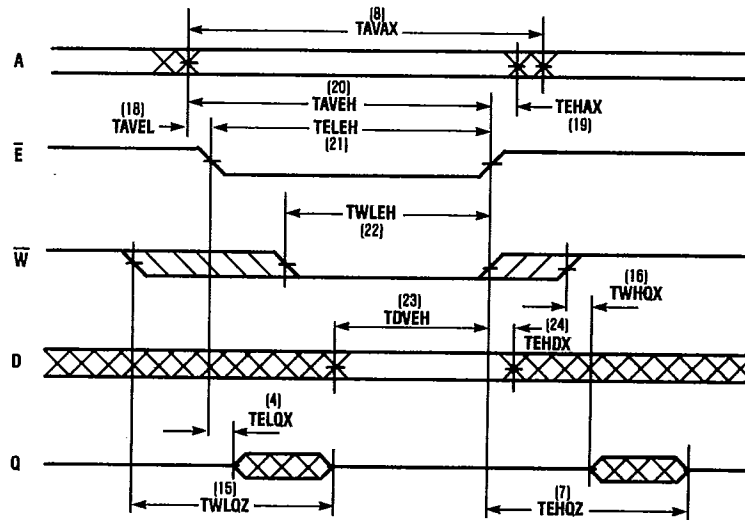


NOTE: \bar{W} is high for the entire cycle and D is ignored. \bar{E} is stable prior to A becoming valid and after A becomes invalid.

WRITE CYCLE 1: CONTROLLED BY \bar{W} (LATE WRITE)



NOTE: In this mode, \bar{E} rises after \bar{W} . The address must remain stable when- ever both \bar{E} and \bar{W} are low.

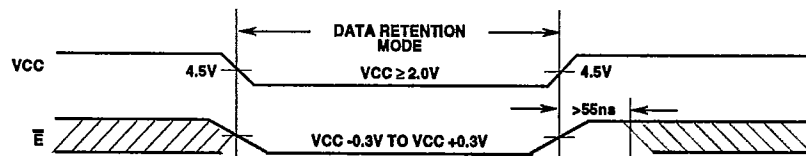
Timing Waveforms (Continued)WRITE CYCLE 2: CONTROLLED BY \bar{E} (EARLY WRITE)

NOTE: In this mode, \bar{W} rises after \bar{E} . If \bar{W} falls before \bar{E} by a time exceeding $TWLQZ$ (Max) $TELOX$ (Min), and rises after \bar{E} by a time exceeding $TEHQZ$ (Max)- $TWHQZ$ (Min), then Q will remain in the high impedance state throughout the cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable (\bar{E}) must be held high during data retention; within VCC to $VCC + 0.3V$.
2. On RAMs which have selects or output enables (e.g., S , \bar{G}), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., \bar{E}) must be kept between $VCC + 0.3V$ and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation $> 55ns$ after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING

Performance Curve

TYPICAL ICCDR vs T_A

