

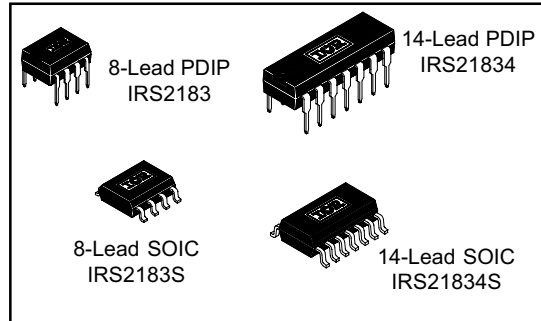
IRS2183(4)(S)PbF

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A
- Also available LEAD-FREE (PbF)

Packages



Description

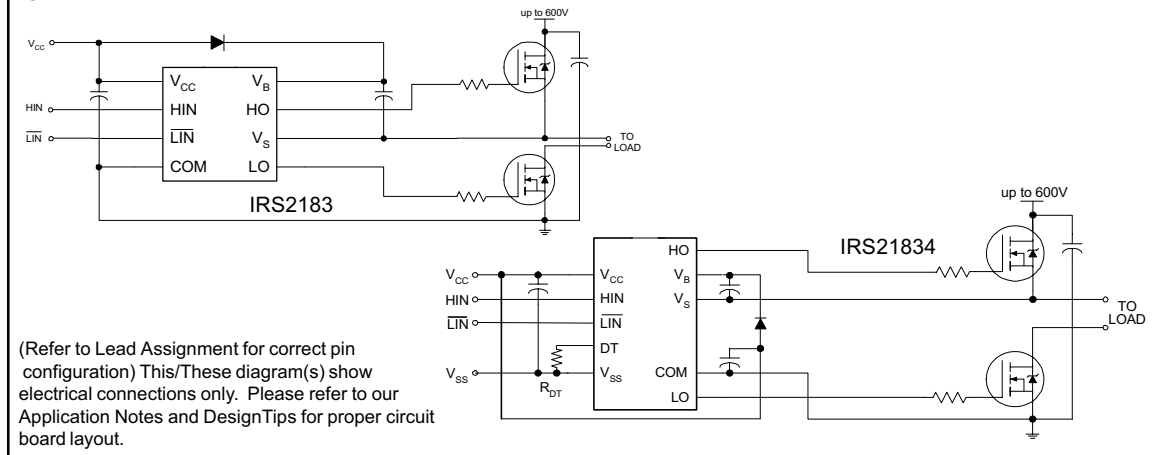
The IRS2183(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V

logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IRS2181/IRS2183/IRS2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/LIN	yes	Internal 500ns Program 0.4 ~ 5 us	COM	180/220 ns
21834				VSS/COM	
2184	IN/SD	yes	Internal 500ns Program 0.4 ~ 5 us	COM	680/270 ns
21844				VSS/COM	

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	620	(Note 1a)	
V _S	High side floating supply offset voltage	V _B - 20	V _B + 0.3	V	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	20		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
DT	Programmable dead-time pin voltage (IR21834 only)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & $\overline{\text{LIN}}$)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{SS}	Logic ground (IR21834 only)	V _{CC} - 20	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Note 1a: All supplies are fully tested at 25V and an internal 20V clamp exists for each supply.

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN & $\overline{\text{LIN}}$)	V _{SS}	V _{CC}	
DT	Programmable dead-time pin voltage (IR21834 only)	V _{SS}	V _{CC}	
V _{SS}	Logic ground (IR21834 only)	-5	5	°C
T _A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

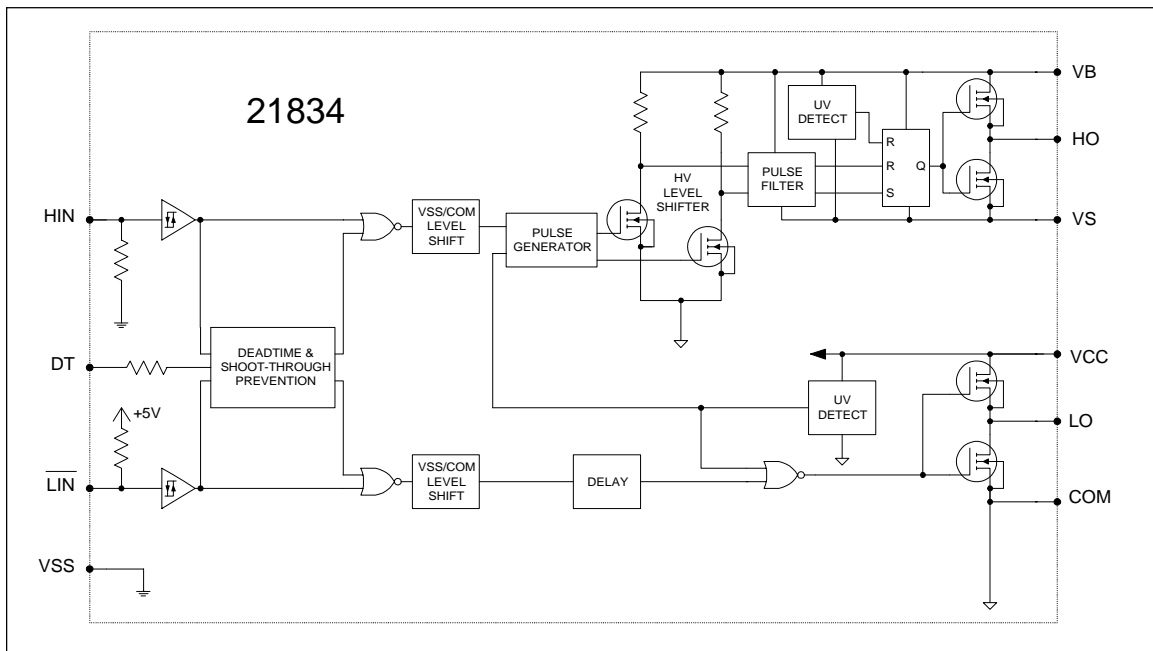
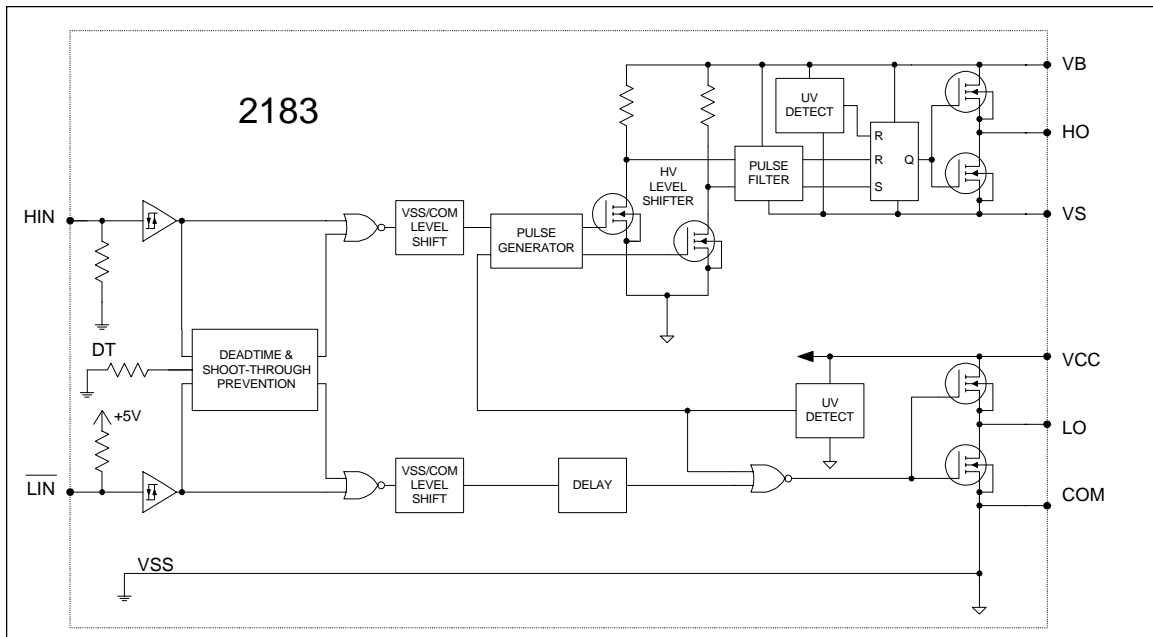
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	220	330		$V_S = 0V$ or 600V
MT	Delay matching $t_{on} - t_{off}$	—	0	35		
t_r	Turn-on rise time	—	40	60		$V_S = 0V$
t_f	Turn-off fall time	—	20	35		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO})	280	400	520		μsec
		4	5	6	RDT = 200k (IR21834)	
MDT	Deadtime matching = DT _{LO-HO} - DT _{HO-LO}	—	0	50	nsec	RDT=0
		—	0	600		RDT = 200k (IR21834)

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, DT = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HIN & logic "0" for \overline{LIN}	2.5	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage for HIN & logic "1" for \overline{LIN}	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150	μA	$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" input bias current	—	25	60	μA	$HIN = 5V, \overline{LIN} = 0V$
I_{IN-}	Logic "0" input bias current	—	—	1.0		$HIN = 0V, \overline{LIN} = 5V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	$V_O = 0V,$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		$V_O = 15V,$ $PW \leq 10 \mu s$

Functional Block Diagrams



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IRS2183 and VSS for IRS21834)
LIN	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IRS2183 and VSS for IRS21834)
DT	Programmable dead-time lead, referenced to VSS. (IRS21834 only)
VSS	Logic Ground (IRS21834 only)
V _B	High side floating supply
HO	High side gate driver output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments

<p>8-Lead PDIP</p>	<p>8-Lead SOIC</p>
IRS2183PbF	IRS2183SPbF
<p>14-Lead PDIP</p>	<p>14-Lead SOIC</p>
IRS21834PbF	IRS21834SPbF

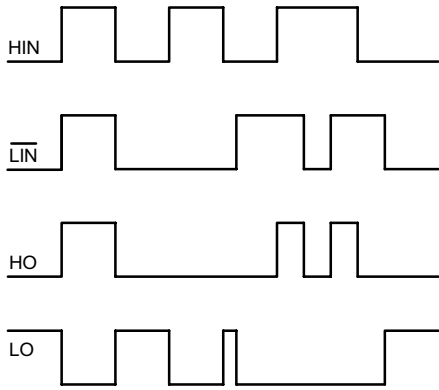


Figure 1. Input/Output Timing Diagram

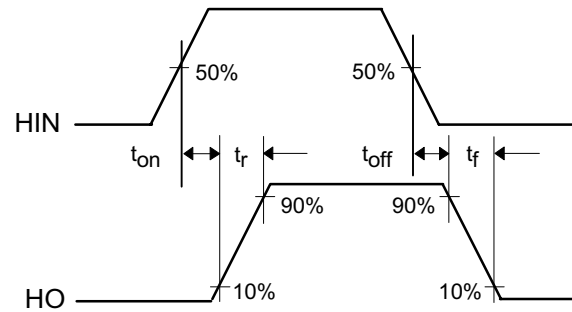
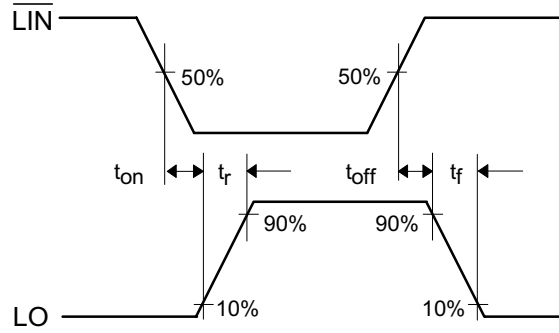


Figure 2. Switching Time Waveform Definitions

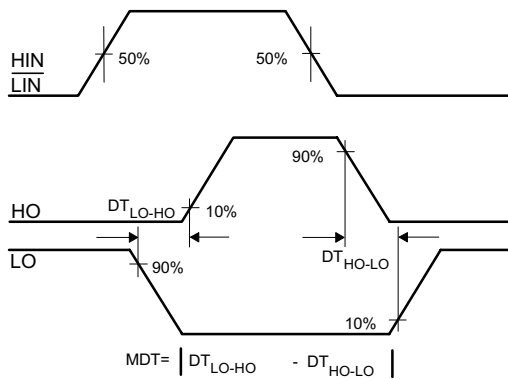
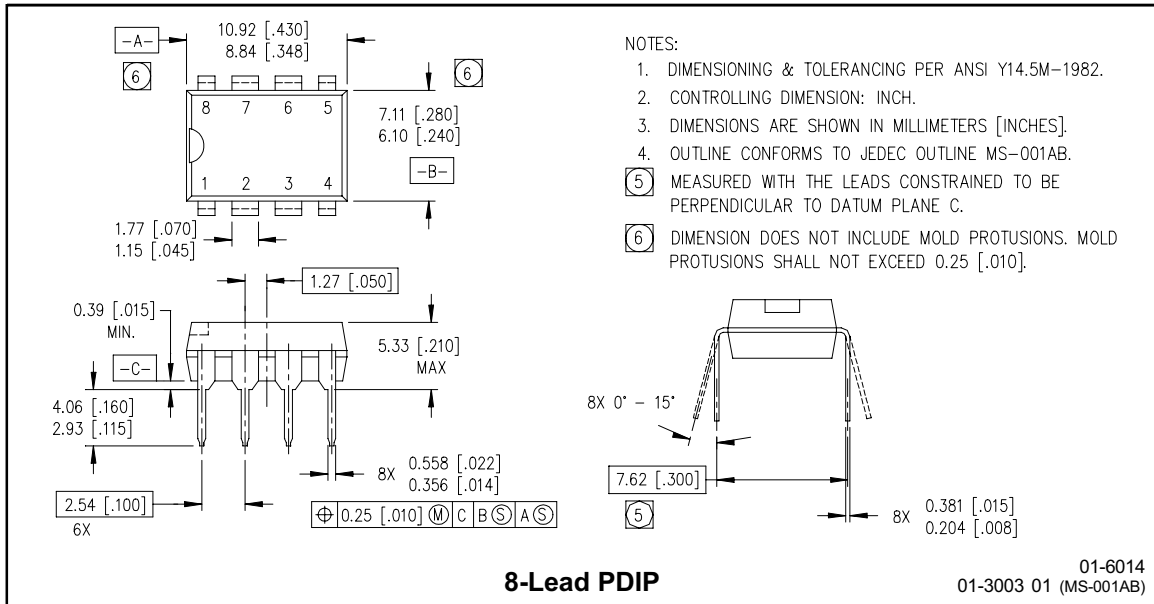
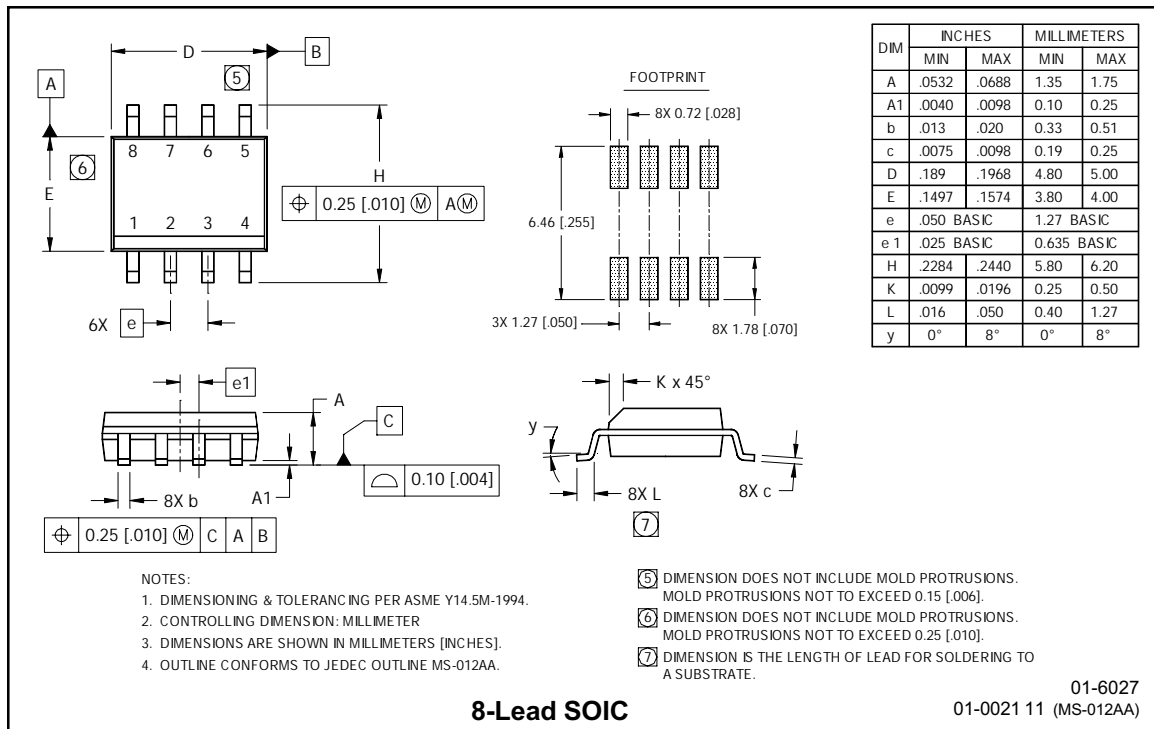


Figure 3. Deadtime Waveform Definitions

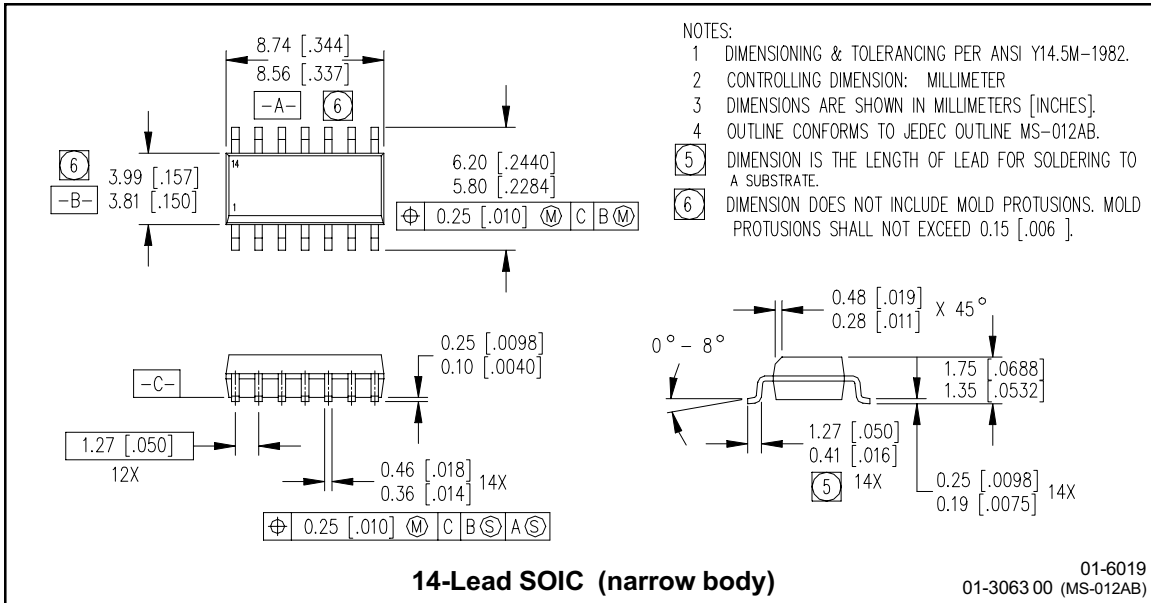
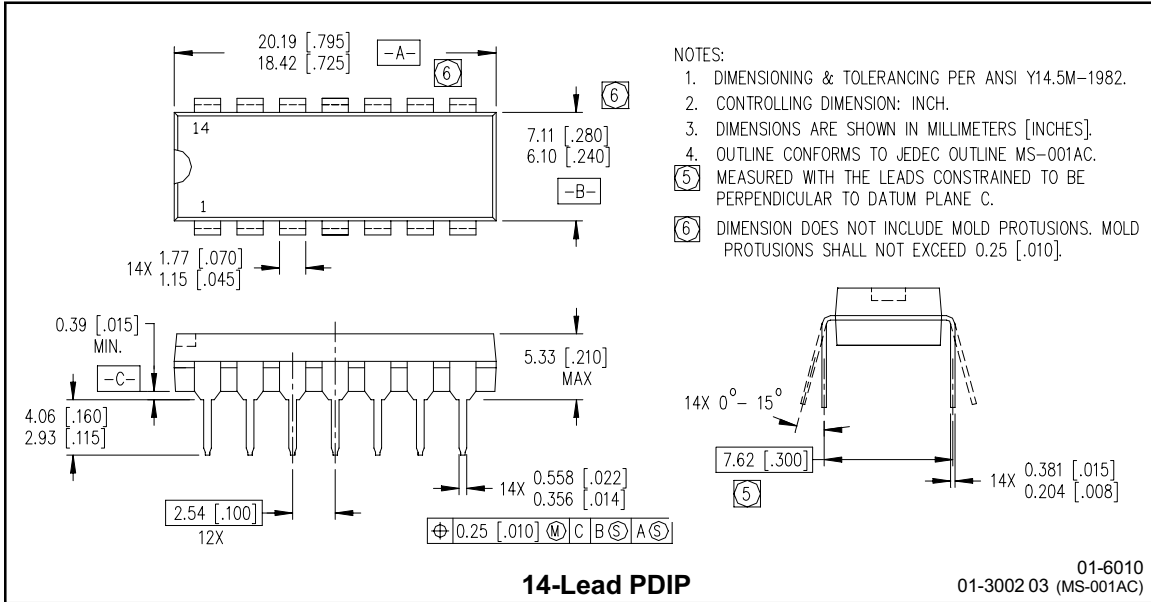
Case outlines



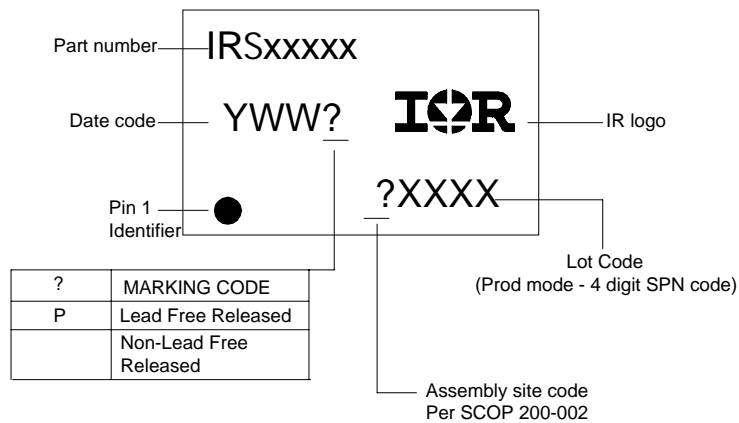
8-Lead PDIP



8-Lead SOIC



LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

8-Lead PDIP order IRS2183PbF
 8-Lead SOIC order IRS2183SPbF

14-Lead PDIP order IRS21834PbF
 14-Lead SOIC order IRS21834SPbF